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The Increasing Importance of the Thermal Management for Modern Electronic Packages

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Abstract:
This paper deals with the significance of the thermal management for some modern types of electronic packages. The main part is focused on the Quad-Flat No-leads (QFN) package and its mounting ways and means, which depends significantly on their thermal characteristic. Apart from that, thermal properties of the Ball Grid Array (BGA) package were also calculated as well as thermal resistances for each structure. All results were gained through the computer simulations, which were done in ANSYS program.

INTRODUCTION

The design of the electronic package is very complicated process that includes many steps. One of the most important specifications is a thermal management of such package. The main issue for thermal management is cooling of the chip that is secured by heat distribution from the die to the ambient. This can be done by many ways, but we also need to consider other aspects, like electric insulation, thermo-mechanical stress etc. The former packages haven´t basically dealt with cooling, because of their low power and low temperature. The situation has changed with increasing performance and reducing area for cooling, that's the reason why thermal management is playing such a big role in up to date designs.

In modern types of the package, for example QFN, is thermal design closely related to the mounting possibilities on the board. This is given by direct contact between the board and thermal pad of the QFN, see Fig. 1. The problem is detailed described in this article. Moreover we also have to consider influence on the components near the package, because higher temperature could cause many issues, like bad signal interpretation, value change or reliability failures.

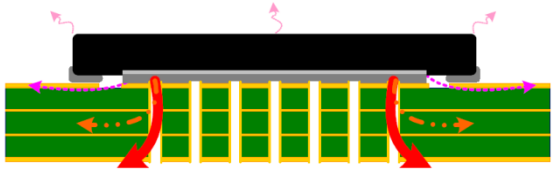

Fig. 1: Heat paths away from the QFN package [2]

Ball Grid Array package is also very popular package type. This is mainly because of high number of the leads, lower thermal resistance between the package and the PCB and low-inductance leads. Thermal design is slightly different than for QFN package, but it could serve as a good sample for comparison.

The modern approach for thermal solution of electronic packages is done through the simulation tools, which one of the most affordable and the most common is ANSYS software. In this article is shown the application of this program to deal with thermal conditions of modern packages determining real temperatures distribution, specify the heat flux and redirect it by using thermal improvement. Generally increased temperature of packages causes thermal stress, which in a result can eventually evoke their failure.

THE BASICS OF THERMAL MANAGEMENT

Thermal management focuses on the thermal solution based on the heat transfer. This can take place through conduction, convection or radiation. In this case, carry the importance the first two, respectively.

Conduction

The description of the whole package thermal properties is based on fundamental thermal theory. There are three thermal transport mechanisms: conduction, convection and radiation. Every mechanism is ensuring heat dissipation from the die. The conduction is very often presented by heat flow or the heat flux, as the rate of a heat, transferred through a given surface. For the heat flux Q (W m^{-1}) we can write the following:

$$Q = \lambda . A . \frac{\Delta T}{d} \qquad (1)$$

, where λ [W m^{-1} °C^{-1}] is thermal conductivity, A is the given area (m^2), ΔT is the temperature gradient (°C) and d is the distance of the thermal gradient [7].

If we consider thermal properties of the package, we have to focus on thermal gradient between the die and the ambient near the package, or the board. Apart from that we also need to know heat flux, which flows through the system. These variables and their behavior are very similar to the electric ones. For example heat flux is similar to the current, temperature gradient to the voltage, etc. Therefore, we could assume that the basic equations are also similar. With this assumption, we could state the "Ohm´s Law" for the thermal domain. That is derived from the Fourier´s Law and describes temperature change across the material. By this consideration, we can write the following equation for a junction to ambient thermal resistance [3]:

$$R_{\theta JA} = \frac{\Delta T_{JA}}{P_D} = \frac{(T_J - T_A)}{P_D} \qquad (2)$$

This value is most commonly used for thermal specification of the package by manufactures. Generally it's defined for the worst case, but it could also serves as a good indicator of how well is heat dissipated from the die. Junction to ambient thermal resistance differs with options of package mounting and it also changes considering given configuration.

Convection

Another thermal transport mechanism is convection, which occurs when the solid surface is in contact with fluid or gas. Though the thermal transport is more complicated than with conduction, the basic equation is quite simple:

$$q = k.A.\Delta T \qquad (3)$$

, where q is heat transferred per unit time (W), k is heat transfer coefficient of the process (W m^{-2} °C^{-1}), A is heat transfer area of the surface (m^2), ΔT is temperature difference between the surface and the bulk fluid (°C) [3].

From the list of variables above, it's most complicated to define heat transfer coefficient. There are two ways how to reach it**,** first is the experimental way, where we have to measure heat transferred through the system and consequently determine the coefficient value. Other way how to usually define this coefficient is its calculation according to the type of convection, (natural or forced) and its direction.

For vertical direction we can assume the heat transfer coefficient as:

$$k = \frac{Nu.\lambda}{H} \qquad (4)$$

and for horizontal direction we can write:

$$k = \frac{\frac{Nu.\lambda}{W.L}}{2W + 2L} \qquad (5)$$

where λ is thermal conductivity (W m^{-1} °C^{-1}), H, W and L are dimensions of the considered body and Nu is the Nusselt Number, which is a function of Reynolds Number and the Prandtl number [4]. In following simulations, we have calculated heat transfer coefficients for each material and also for vertical and horizontal orientation. The temperature of ambient surrounding the system was 50°C.

THERMAL MANAGEMENT OF ELECTRONIC PACKAGES

The solution of the thermal dissipation from the chip is the main question in the package design. The need of the heat distraction is growing as the power of the chip rises. There are many ways how to distract heat, nevertheless we need to use material with great thermal conduction, such as copper. The problem is that mounted package is the heterogeneous system, which includes materials with different coefficient of thermal expansion and this is causing reliability issues through thermomechanical stress. Therefore, we need to be very cautious about final design of the package. Thermal properties for used materials in packaging are summarized in Table 1.

Table 1: Thermal properties for used material

Material	**Density [kg.m^{-3}]**	**Thermal Conductivity [W.m^{-1}.K^{-1}]**
Adhesives	2400	3,8
Copper	8940	401
Die	2330	108
Mold Compound	2088	0,67
Solder	8400	50
Substrate	1900	X/20,62; Y/0,366; Z/20,62

Thermal simulations of modern packages

Computer simulations have recently become an integral part of the package design. We can spare a lot of time and money by creating a virtual model of the structure. This model we can use for different types of simulation: thermal, electric, structural, etc. Therefore, we are able to calculate necessary values and we can apply this knowledge into our package design.

The decisive factor for the simulations is the time at which we are able to obtain the results. That depends on the quality of the hardware, which we have available for calculation. It's simpler and also common to simulate only one fourth of the virtual model, by this we have less equation to solve and lower result time, but this simplification we can use only for symmetric models.

Thermal simulations are based on the heat transfer through the system. In the package is heat generated by the die and it goes through the easiest way to the ambient. Generally it goes through the shortest distance, with regard to the material, but it's often the inappropriate solution and we need to create different path for the heat. The designer's task is to ensure that path and hence avoid reliability and functional issues.

QFN (Quad Flat No-leads) package

The simulation model of QFN package is shown on Fig. 2. The die is attached to the thermal pad through the adhesive. Leads are connected with the die by wirebonds, which weren't modeled because of insignificant effect on thermal characteristic. Whole system is packaged in the mold compound. The connection with the copper pads on the printed circuit board (PCB) is ensured by standard lead solder.

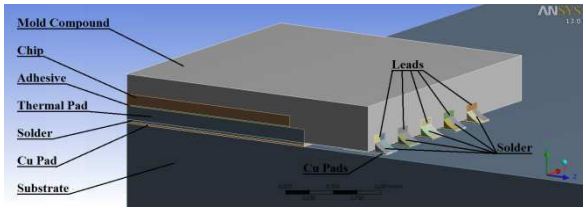

Fig. 2: Model of QFN package

As we have mentioned above, thermal parameters for structure with QFN package are very much reliant on mounting technique. This is caused by thermal pad, which is attached directly to the die and it provide the main cooling of the chip. In the basic version of mounting (Fig. 3.) is the pad soldered to the PCB, therefore we assume that the heat is conducted through the pad into the board. The problem is that PCB has low thermal conductivity and the heat is cumulating under the chip. Different transition way for the heat is through the leads of QFN package and subsequently further to the conductive net. This can cause problems such as signal interpretation, parameter change, thermo-mechanical stress, etc. In followed simulations we have determined how given style of assembly changes thermal parameters of the package.

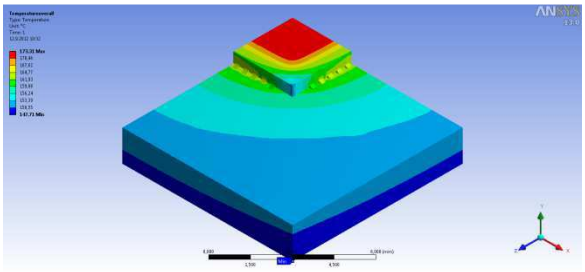

Fig. 3: Temperature distribution in QFN package

In the first case we have connected the thermal pad with the copper layer on the PCB surface, Fig. 4. By this we have ensured the heat dissipation from thermal pad to the copper layer and at same power the chip temperature have consequently fallen by almost 7%. In addition we have used another copper layers in the middle, in the bottom of PCB and then both. The temperature drop wasn´t that substantial, but additional copper layers have secured much better temperature distribution in the PCB, thus there are no such large deformations of the board. From two mentioned cases, the bottom copper layer comes out as better solution. The middle layer also improves thermal characteristics and its usage depends on the application, because of the value of such PCB.

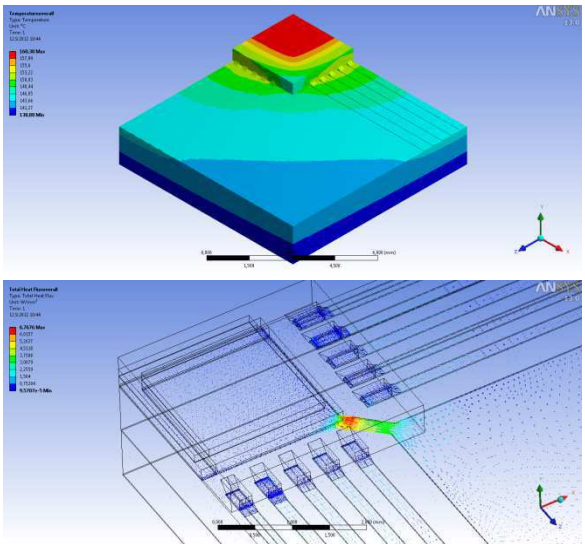

Fig. 4: Temperature and heat flux for PCB with copper layer

Other way how to cope with heat dissipation from the thermal pad, or die, is implementation of thermal vias in the substrate. This will create new way for heat to flow through the PCB and then we can conduct heat furthermore to the copper on the bottom side of the PCB. The vias will enhance the thermal properties of the package even without additional copper plate, but

the heat will remain nearby the package. The heat flux of the system with the thermal vias and copper plate on the bottom side is shown in Fig. 5.

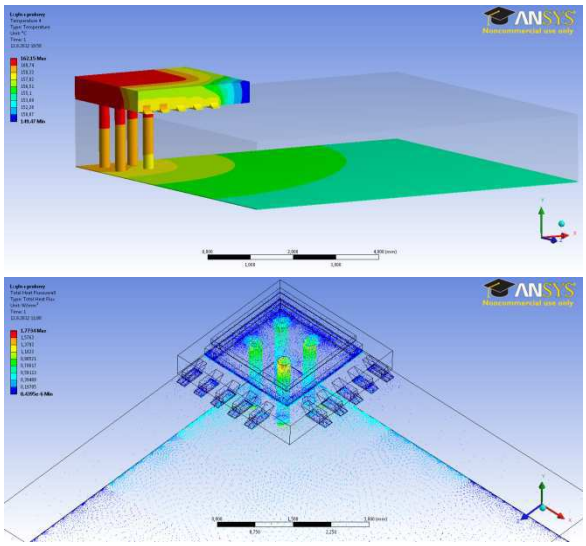

Fig. 5: Temperature and heat flux distribution for PCB with thermal vias

Thermal properties of the package are improving with number of thermal vias, but there are some rules, which we have to respect, like minimal (maximal) diameter of the via, distance from the edge of thermal pad, distances between the vias, etc. [5]

BGA (Ball Grid Array) package

The same simulation as for QFN was modeled for BGA to compare its thermal properties; shown on Fig. 6. The maximum temperature of the system was almost the same as for basic structure with QFN, but the heat distribution is for BGA much worse.

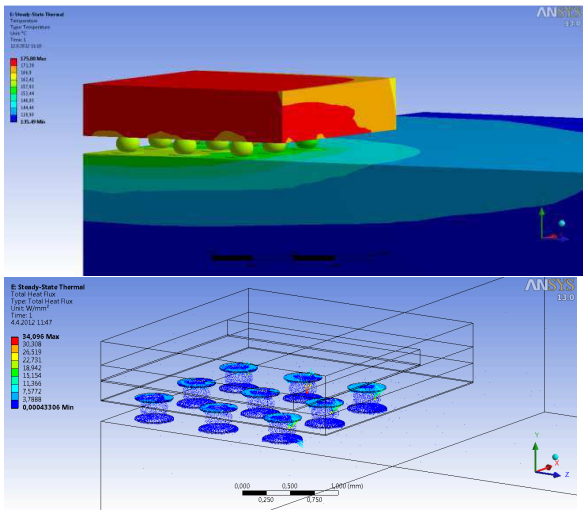

Fig. 6: Temperature and heat flux distribution for BGA package

As we can see, the all amount of heat is conducted through the solder bumps. This could cause big troubles, like mechanical stress of bumps and their consequent deformation or cracks. We can also use thermal pad as in the QFN case, but we will face problems during soldering process and also reliability issues, which are very specific for BGA package. The usage of thermal vias could also improve thermal dissipation of the package, but correct mounting of such structure will be very complicated. The copper layer is not very useful in this case, unless we use thermal pad. Very good solution is provided by passive heat sink, which is attached on the top of the package and then the heat is conducted to the heat sink directly and dissipated to the ambient. This structure is also known as the EBGA package (Enhanced Ball Grid Array), because it is improving thermal as well as electric characteristics. The basic principle of enhanced BGA package structure is shown on Fig. 7.

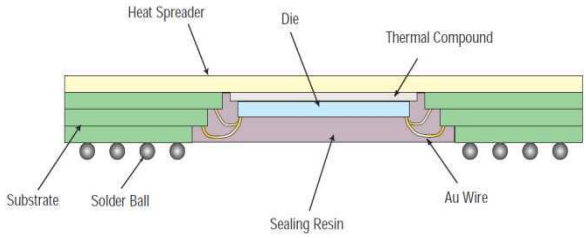

Fig. 7: Enhanced BGA package; structure [6]

From the thermal point of view EBGA main idea lays on conducting heat not through the solder balls, but to the heat sink on the top and consequently to the ambient. As shown in Fig. 8. the temperature of the solder balls is much lower in EBGA structure.

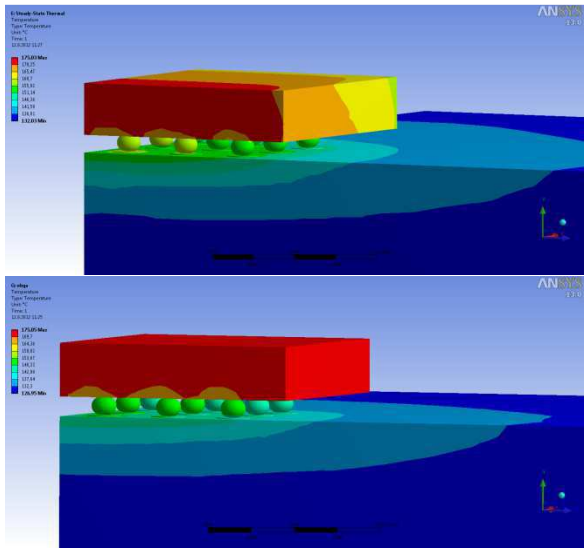

Fig. 8: Temperature distribution of the BGA (top) and EBGA (bottom) package

Calculation of junction to ambient thermal resistance

The rate of thermal improvement could be gained from the simulations by calculation of the coefficient called junction to ambient thermal resistance ($R_{\theta JA}$), according to equation (2). The results are summarized in Table 2.

Table 2: Thermal resistance of QFN and BGA packages

Package	$R_{\theta JA}$ (°C/W)		
	General mounting	Copper plate	Thermal vias
QFN	94,32	80,08	12,41
-	PCB		Top side
BGA	155,68		3,56
EBGA	207,4		0,2

The thermal resistances for the QFN package were calculated from the temperature of the die and of the bottom side of the PCB. The same calculations were done for BGA and EBGA (values in the column PCB). The values for BGA and EBGA (Table 2.) are displayed in the column "Top side" were gained from the chip temperature and the top side of the package.

We can see that the QFN package generally secures better heat distraction than the BGA and the best solution for the QFN package are thermal vias. Even though the lowest values of thermal resistance are for the BGA/EBGA structure in the last column, we have to know that these values were calculated differently than the others. However, we can state that the EBGA version ensures much better heat transfer to the top side (to the heat sink) than the regular one.

Conclusions

Every single type of the electronics package has specific thermal characteristics. There is an important fact that we need to solve not just thermal management for the package itself, but for the whole interconnection structure. As we have shown in this article, mounting technique is very crucial for final thermal properties of the modern packages, like QFN, which has increasing number of leads by small dimensions. Thermal vias have proved to be the best thermal improvement of those that are the most used in today's PCB. However, this solution is also the most expensive one. Therefore, we need to adapt thermal solution to given application and find the compromise between the price and desired temperature rate.

The best way how to find this solution is the use of computer simulation. By doing this we are able to determine final temperatures for the whole structure; specify the heat flux and redirect it by using thermal improvement, etc. The simulations are also much cheaper than creation of the testing prototype for every thermal option.

Acknowledgments

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REFERENCES

[1] Psota, B.: *The Increasing Importance of the Thermal Management for Modern Electronic Packages,* Electronic Devices and Systems Conference Proceedings, Brno, 2012

[2] Thermal Considerations for QFN Packaged Integrated Circuits. In: *Analog and Digital Processing ICs, Semiconductor Company, Cirrus Logic:* [online]. [cit. 2012-04-28]. Web: http://www.cirrus.com/en/pubs/appNote/AN315REV1.pdf

[3] FREESCALE SEMICONDUCTOR, Inc. *Thermal Analysis of Semiconductor Systems* [online]. 2008 [cit. 2012-04-04]. Web: http://www.freescale.com/files/analog/doc/white_paper/BasicThermalWP.pdf

[4] Jamia A.: *Practical Guide to the Packaging of Electronics-Thermal and Mechanical Design and Analysis*. New York: Marcel Dekker, Inc., 2003. ISBN 0-8247-0865-2.

[5] CIRRUS LOGIC. *Thermal Considerations for QFN Packaged Integrated Circuits* [online]. 2008 [cit. 2012-04-04]. Web: http://www.cirrus.com/en/pubs/appNote/AN315REV1.pdf

[6] Enhanced BGA. In: Fujitsu Global [online]. [cit. 2012-04-28].Web: http://192.240.0.102/downloads /MICRO/fma/pdf/enchancedpkg.pdf

[7] Szendiuch,I.: *Základy technologie mikroelektronických obvodů a systémů*. Brno: VUTIUM, 2006. 377 s. ISBN 80-214-3292-6