UNIVERSITY OF WEST BOHEMIA

Faculty of Electrical Engineering

Department of Applied Electronics and Telecommunications

DOCTORAL THESIS

Development of the TOTEM trigger system

Pilsen, 2014 **Ing. Josef Kopal**

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Candidate: Ing. Josef Kopal
Supervisor: prof. Ing. Jiří Pinker, CSc.
Supervisor specialist: RNDr. Vojtěch Kundrát, DrSc.

Pilsen
2014

in loving memory of my mother Jana
věnováno památce mojí maminky Jany

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Název práce:	Vývoj triggrovacího systému projektu TOTEM
Kandidát:	Josef Kopal
Katedra:	Aplikované elektroniky a telekomunikací
Vedoucí doktorské práce:	prof. Ing. Jiří Pinker CSc. Fakulta Elektrotechnická, ZČU, Plzeň
Vedoucí specialista:	RNDr. Vojtěch Kundrát DrSc. Fyzikální ústav, AV ČR v.v.i, Praha
Abstrakt:	Spouštěcí (triggerovací) systém je první krok při analýze dat a je nepostradatelnou součástí moderních detektorů. Vyhodnocuje a posuzuje všechny události v reálném čase a pokud jsou splněné stanovené podmínky, spouští vyčítání dat z detektoru. Z tohoto důvodu je kritický pro následnou analýzu dat. Tato práce se zaměřuje na implementaci a optimalizaci triggerovacího systému pro experiment TOTEM. Dále popisuje integraci triggerovacích systémů experimentů CMS a TOTEM pro společný fyzikální program.
Klíčová slova:	CERN, CMS, FPGA, LHC, TOTEM, TRIGGER

Title:	Development of the TOTEM trigger system
Candidate:	Ing. Josef Kopal
Department:	Department of Applied Electronics and Telecommunications
Supervisor of the thesis:	prof. Ing. Jiří Pinker CSc. Faculty of Electrical Engineering, UWB, Pilsen
Supervisor specialist:	RNDr. Vojtěch Kundrát DrSc. Institute of Physics, AS CR v.v.i, Prague
Abstract:	A trigger system is the first part of a data analysis and it is an essential part of modern detectors. It processes and overviews all events in real time and activates an consecutive data acquisition, when defined criteria are satisfied. Thus the trigger system is critical for an consecutive offline data analysis. This work is focused on implementation and optimization of the trigger system of the TOTEM experiment. An integration of the CMS and TOTEM trigger systems for common physics program is also discussed.
Key Words:	CERN, CMS, FPGA, LHC, TOTEM, TRIGGER,

I hereby submit this work (written during my studies at UWB Pilsen) for review and advanced defense. I declare that all work has been done independently. All used literature and sources are cited and listed in this document.Only legal and licenced software was used.

In Geneva, Switzerland .....

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Contents

Introduction

CERN (Organisation européenne pour la recherche nucléaire) is the largest center for particle-physics research in the world. It is located on the French-Swiss border close to Geneva. This facility provides physicists with an excellent environment for fundamental research. At CERN, the Large Hadron Collider (the world largest hadronic particle collider) has been built. Inside the LHC machine, the particles (protons and ions) are accelerated in clock-wise and counter-clock-wise directions. The machine perimeter is about 27 km. Each particle could reach an energy up to 4 TeV per nucleus; from 2015 on a maximum energy of 6.5 TeV is foreseen. During the operation, the particles are orbiting in well defined groups - the so-called "bunches". Since the particles reach almost the speed of light, the orbiting frequency of a single bunch is about 11 kHz. Up to 2808 bunches can be present in each ring. There are four beam intersection points, the so-called "interaction points" 1, 2, 5 and 8, where those bunches pass through each other (the so-called "bunch collision"). While bunches collide, only few particles interact with each other, thus the probability of detectable interactions is small. However, due to the high orbiting frequency and the number of bunches, the volume of generated data is enormous.

When particles interact with each other, the following scenarios (or their combinations) may occur: their trajectories are changed, they are destroyed or new particles are created. For physics studies, observables of the particles leaving the interaction have to be measured (e.g. trajectory, energy, charge, time of flight etc.). To do so, various detectors of several experiments are surrounding the LHC interaction points. The experiments are: ATLAS, ALICE, CMS, TOTEM, LHCb, LHCf, MoEDAL and ALICE. For individual experiments, only a small subset of interactions is interesting, depending on the physics studies to be performed. The measurement data flow has to be monitored and controlled to optimize the usage of available resources (such as the data storage space, transmission line bandwidth, etc.). One way is a continuous monitoring of the measuring equipment (detectors) and activating (triggering) the data read-out and storage only if the predefined criteria are met.

In large systems, the data monitoring is very demanding from the data-transfer and data-analysis point of view. It is not possible to deliver all the measured data to a single center and to perform complex data analyses in real time. Therefore at least three different processes (systems) are needed. The Trigger System is responsible for the real-time detector monitoring, data evaluation and triggering the system responsible for the data read out called "data acquisition system (DAQ)". The last important system is the so-called "offline data analysis" that is responsible for consecutive data analyses and physics studies. Each system has different requirements from the engineering point of view. The Trigger System evaluates in real time a subset (trigger data) of the data stored in local short-time buffers (possible physics data) and performs a raw analysis of the physics observables in order to select events of physics interest. Data fulfilling the selected criteria are tagged in the local buffers and DAQ executes the readout procedure. The local buffers are usually limited in size, thus the trigger decision has to be taken

in a very short time (for TOTEM of the order of two or three micro-seconds). The trigger and DAQ systems are usually implemented by dedicated ASIC electronics and programmable logic devices like FPGA. To operate both systems correctly, a hand-shake ("busy" signal) has to be implemented between them. Once the tracking data are stored, the offline data processing can begin. Typically, also two additional systems are required: a monitoring system that is responsible for operation parameters monitoring and a slow control system that is responsible for configuration and the system commands distribution.

This thesis describes the work done on the trigger system for the TOTEM experiment. This experiment and its physics program is briefly over viewed in Chapter 1. The TOTEM experiment detectors are situated around the interaction point 5, sharing the location with detectors of the CMS experiment. The possibility to combine the physics data from both experiments provides a better physics coverage (this requires the cooperation of the TOTEM and CMS trigger systems), thus Chapter 1 also contains a brief description of the CMS experiment.

Chapter 2 describes, in general, the topology and functionality of the TOTEM trigger system. The related hardware is described.

The third chapter is devoted to the author's work related to the TOTEM trigger system. The trigger data from all the TOTEM detectors are transmitted via optical fibers, over up-to 300 m distance, to the so-called "counting room" where all events, based on these trigger data, are evaluated according to the selected physics program. When the predefined criteria are met, the final tracking data read out request signal has to be generated to activate the consecutive DAQ readout during experiment measurements. To achieve this, the author has written the corresponding firmware for the FPGA-based trigger electronics in the counting room. For the Roman Pot detectors, the latency of the optical fiber path is too long for the common operation of the TOTEM and CMS experiments. To reduce the trigger system latency, the optical links were replaced by an LVDS parallel bus - the so-called "electrical trigger". The author designed signal repeating devices and cards for a galvanic isolation. The author was also responsible for the manufacturing and consecutive installation in the LHC environment. The author has also developed FPGA firmware for the receiving part of the electrical trigger.

The author's work on the trigger system calibration and commissioning is described in Chapter 4. Once all the components were installed, the system needed to be tested and calibrated. This chapter describes the methods used for the system optimization and examples of trigger system performance. This includes the transmission line performance calibration, detector local clock distribution optimization and detector re-synchronization. Also the trigger performances studies are mentioned. During the system commissioning, the author's work required cooperation with other members of his group. For example, the timing and clock calibration required the system to be fully running and configured. The trigger efficiency studies required extensive work of the offline analysis group.

Chapter 1

The TOTEM experiment and the LHC environment

When two protons collide at high energy their partons (quarks and gluons) exchange momentum and new particles can be created. The angle of out-going particles is related to the momentum transfer. When the momentum transfer is high, out-coming particle trajectories are likely to be found at large angles to the axis of the beam. This is the so-called "central region" (Figure 1.1).

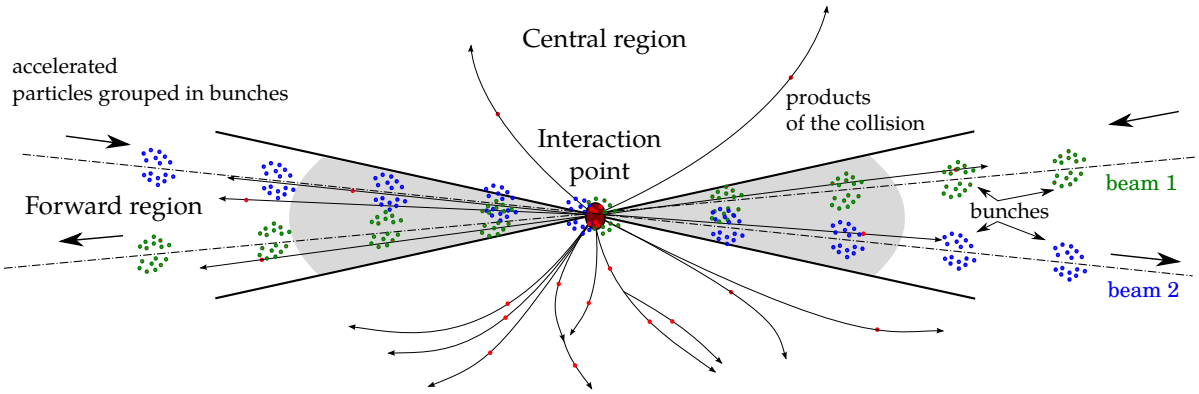


Figure 1.1: At the picture, there are two particle beams (where particles are clustered in bunches) colliding at the interaction point. Depending on the amount of the momentum loss of two interacting particles in the collider, the high energy physics is divided in two main categories: forward region and central region physics.

On the other hand, there is a complementary area: the so-called "forward region" covers collisions with low momentum transfer. All final particles are collimated in the directions of the incoming beams, moreover, it can be that at least one of two colliding protons is preserved and can be detected at a large distance from the interaction point.

The application of modern physics on the forward region processes is not straight forward and certain phenomena are still not well understood. The TOTEM experiment provides unique data for further physics studies.

1.1 CERN accelerator cascade

Currently, the Large Hadron Collider (LHC [4]) LHC is the largest hadronic particle collider in the world and it allows to reach highest energies (per particle) and collide them, in a controlled environment.

Before protons are injected into LHC at the energy of 450 GeV, there is a long way to go. In fact, the cascade of several accelerators is used to reach the injecting energy (Figure 1.2).

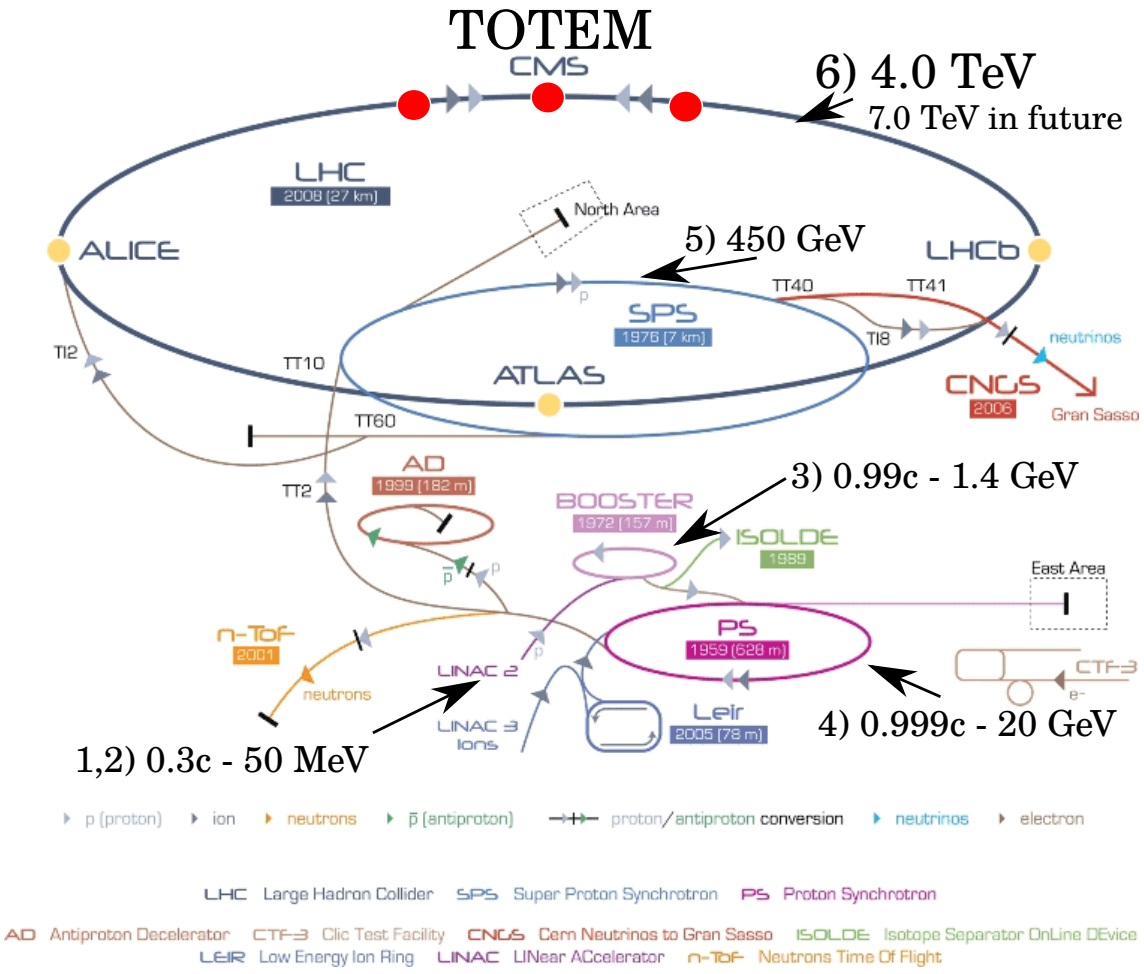


Figure 1.2: CERN accelerator cascade. Before the particles are injected into LHC they pass through a cascade of smaller accelerators to reach the desired parameters [1].

The whole CERN accelerate complex is also used for a number of different, non-LHC, experiments. One example is the so-called “North area”. In the past, this place was used for number of experiments. Currently, it is used as a test beam area providing environment for detector studies and concept verification. Another example is the CERN Neutrinos to Grand Sasso (CNGS) experiment where the beam is directed to special targets where a neutrino beam is created, pointing towards the Grand Sasso laboratory in Italy.

The injection procedure is as follows:

1. Hydrogen atoms are pumped into the Source Chamber on the linear accelerator LINAC 2 and a strong electromagnetic field is used to separate protons and electrons.
2. The protons are accelerated by LINAC 2 to one third of the speed of light (corresponding to proton energy 50 MeV).
3. The protons enter the Proton Synchrotron Booster (PSB) and are accelerated to the 95% of the speed of light. (1.4 GeV).
4. Then the protons are injected to the Proton Synchrotron (PS) and accelerated to the 99.9% of the speed of light (25 GeV).
5. Super Proton Synchrotron (SPS) is the last stage before entering LHC. The protons are accelerated to the energy of 450 GeV.
6. The protons are injected to LHC.

Not all those protons are injected at once. This procedure is repeated and the whole process of injection takes up to one hour (depending on desired bunch parameters). Once all the protons are injected into LHC, they can be accelerated up to the energy of 7 TeV.

1.2 LHC beam structure and configuration

For LHC operation and related physics measurements, LHC beams have very well defined structure and parameters. This is also very useful for detector calibration and fine-timing-optimization (including clock phases and latency verification). In LHC, there are two circulating beams: one clock-wise – Beam 1 (B1) and one counter-clock-wise – Beam 2 (B2). Each beam is composed of particle clusters called bunches (Figure 1.3). Each bunch is divided into 10 sub-segments so-called "buckets". The buckets and bunches are determined by the radio frequency (RF) cavity's resonance frequency of 400 MHz[1] [5] and an LHC clock of 40 MHz. Buckets correspond to period of 2.5 ns. Thus the bunch is 25 ns long. Since the particles travel with a speed that is close to the speed of light:

- one bucket corresponds to 0.749 m distance and
- one bunch corresponds to 7.495 m distance.

The charged particles are injected in a way that they occupy the bucket 1 (Figure 1.3) and the rest of buckets is empty. That means that all particles are located in small fraction of the bunch[2]. This configuration can be used for a precise detector clock phase optimization. When a certain phase shift is programmed into the detectors PLL then we can see aliasing effect and the signal from a single bunch can be seen in two different time slots. Unfortunately, a small amount of particles is migrating between the buckets. This also makes a difference in the beam quality at the beginning and the end of measurements. Thus any system calibration should be done as soon as possible after the injection.

[1] RF cavity in LHC is a metallic chamber. Its electromagnetic field accelerates charged particles.

[2] Only clock of 40 MHz is propagated to experiments. This limits their time resolution and it would be difficult to analyze more colliding bunches in one clock cycle.

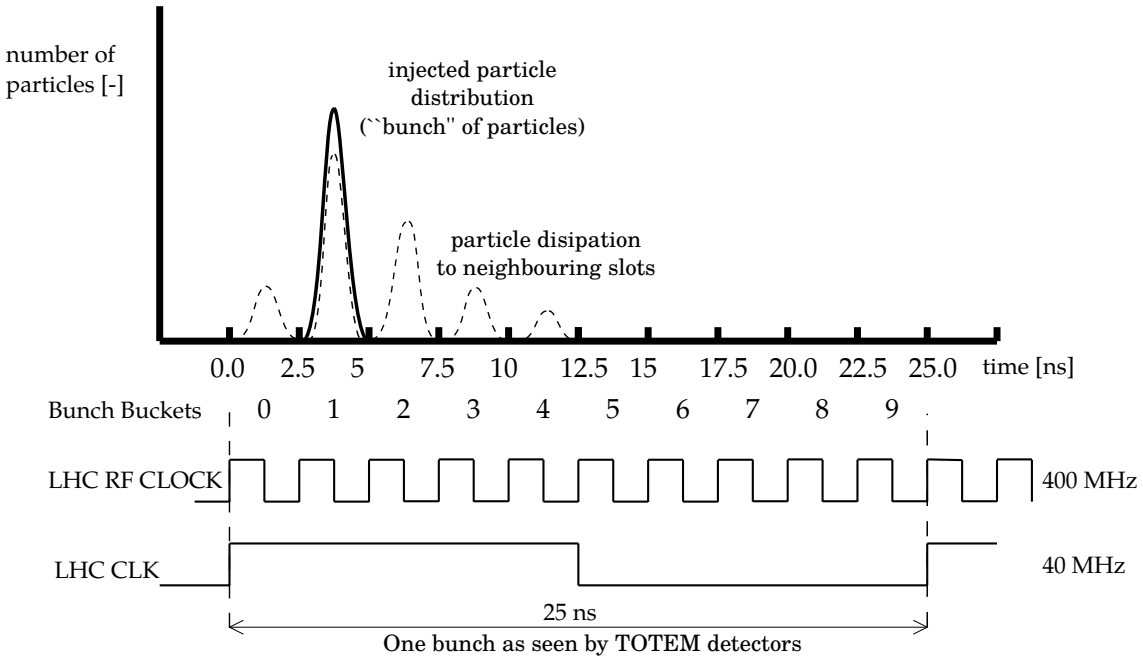


Figure 1.3: Each bunch is segmented to so-called "buckets" 2.5 ns wide (related to RF cavities). In LHC, the particles are injected into the bucket one. This is important for the local detector clock phase tuning. However this structure is invisible for TOTEM detectors.

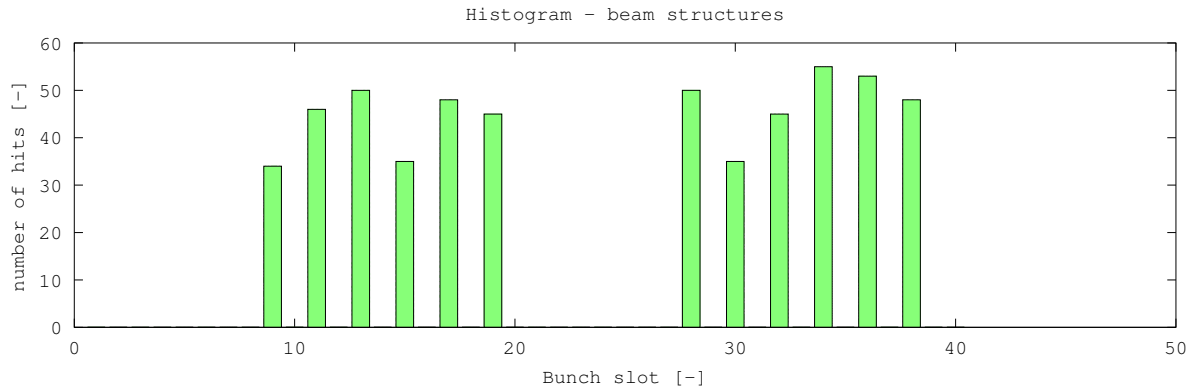


Figure 1.4: The histogram of trigger bits from detectors reveals indirectly the beam structure and trains can be observed (an illustrative image). Bunch slot corresponds to a position in a beam that can be populated by particles.

Considering the circumference of the LHC and the bunch length then 3550 bunches can fit in the LHC beam. This position is called "bunch slot". In reality, charged particles cannot be injected in every bunch slot due to properties of the injecting cascade. The maximum of populated bunches 2808. The beams are injected with a certain number of populated bunches on desired positions. Also, the numbers and location of populated bunches can be different in each beam for different measurement. Such a beam configuration is called a "filling scheme" and is specified before injection.

There are many important attributes related to the filling scheme. Let us mention only the technical ones related to this thesis. The bunches are injected in small numbers (not all at once). They can be injected in consecutive bunch slots with well defined increments. This is the so-called "bunch spacing". Such series of bunches are called "trains". Normally, the beam contains many trains and they are identified by wider gaps (in comparison to the bunch spacing) between populated bunch slots. This is very often used for system calibrations. By creating and analyzing histograms of trigger bits, we can determine the system latencies, identify the instabilities in the clock distribution, etc. An example of the beam histogram is shown in Figure 1.4. In this case there are two trains with six bunches and 50 ns spacing. The number of detected particles (hits) in the detectors is proportional to the bunch intensity.

To determine the first bunch (bunch 0), also a synchronization strobe signal the so-called "Bunch 0 crossing" is physically provided by LHC (together with the clock signal) via LVDS cables. This allows TOTEM electronics and LHC synchronization.

The 40 MHz synchronous clock (one tenth of the RF clock corresponding to the Bunches) is distributed to the rest of relevant electronics (LHC experiments) via Trigger Timing Control (TTC) [11]. This means that TOTEM detectors have their clock perfectly synchronous with LHC. However correct clock phase of local detector clock for each detector have to be determined and fine-tuned to achieve the optimal system performance. The clock frequency also determines the time resolution of TOTEM detectors to 25 ns.

1.3 CMS experiment overview

Together with ATLAS [7], CMS [8] is a general purpose experiment focused on central-region collisions. It was conceived to detect and study a wide range of particles and phenomena created by the interactions of high-energy particles during the operation of the LHC machine.

The CMS detector is located one hundred meters deep inside the CMS experimental cavern around IP5. To fulfill its physics program, various types of sub-detectors are installed. To provide the sufficient information about collisions, the CMS detector has an onion-like structure (Figure 1.5).

In the middle of the apparatus, there is the Tracker detector which can reconstruct the trajectory of charged high-energy particles such as electrons, muons, hadrons and see tracks of a decay of short-lived particles. Inside the detector, there is a strong magnetic field (4 T). As charged particles travel trough the magnetic field their trajectory is bend by the Lorenz force. This gives us the information about the particle momentum and charge. The spacial resolution of the CMS tracker is extremely important. Also the amount of material in this region has to be limited to minimize effects of the multiple-scattering on the measurement. For this reason the Tracker is made of silicon strip and pixel detectors with a resolution down-to 10 μm. Due to the fact that it is also the closest detector to the interaction point, it has to be carefully designed from the radiation-hardness point of view.

The second layer is the Electromagnetic Calorimeter (ECAL). It is used to measure of the energy of the exiting proton and electrons.

The next layer is the Hadron Calorimeter (HCAL) which measures energy of hadronic particles. It also provides indirect measurements of a presence of non-interacting (uncharged) particles such as neutrinos. During particle decays, new particles can be created. For this reason the HCAL is made such that no known particle (except muons and neutrinos) can escape it

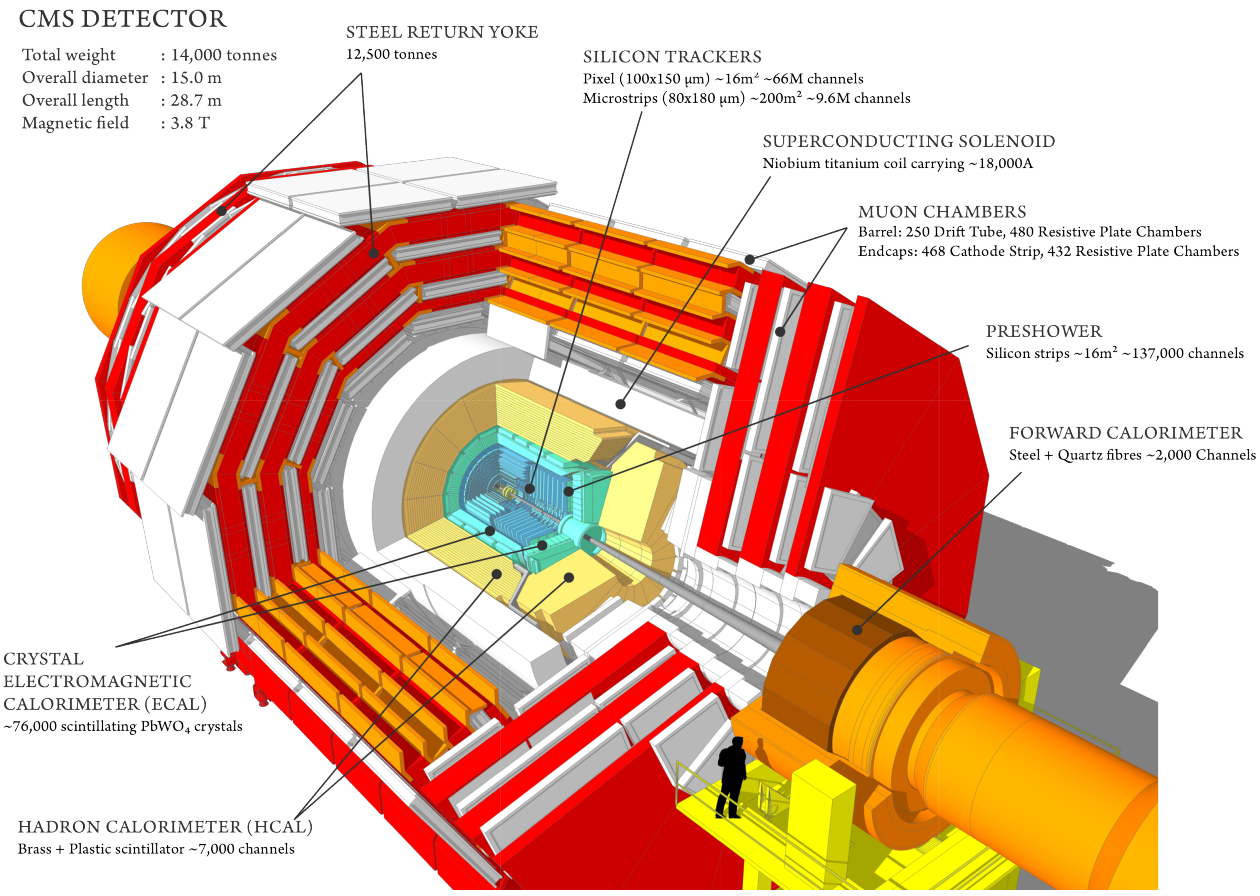


Figure 1.5: Onion-like structure of the CMS detector. The detector encapsulates IP5 to measure observables of the out-coming particles [8].

without being detected. If there is a discrepancy in the measured energies and momenta of particles, it can be a clue that a new-unknown particle has been created.

As it was mentioned before, a strong magnetic field is present inside the CMS detector. It is created by a super-conductive solenoid magnet. Its core is the fourth layer of the CMS detector.

The last layer is a sandwich of muons detectors and steel return yokes for the magnetic field. Unlike most other particles, muons can penetrate a few meters thick layer of material without any interaction. This means they are not stopped by the inner calorimeters and solenoid magnet. For this reason, the muon detectors are placed as the outer layer of the CMS detector.

Figure 1.6 shows the CMS flight-through of several particle types.

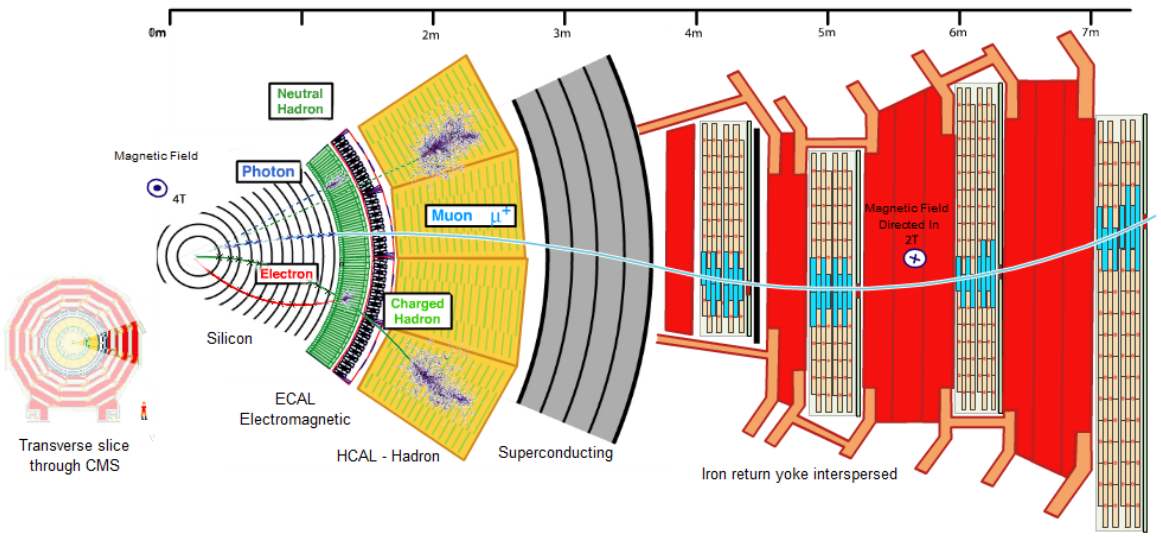


Figure 1.6: This image shows how various types of particles interact with the components of the CMS detector. The different types of particles are absorbed in the corresponding layers [8].

1.4 TOTEM Experiment

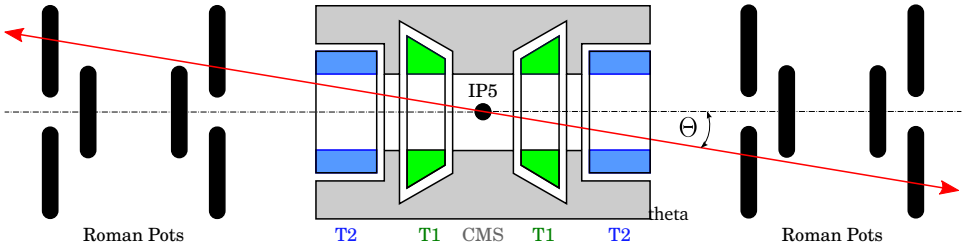
The TOTEM experiment [3] shares IP5 with CMS. Since the TOTEM physics program explores the forward-region physics, the configuration is radically different from the large general-purpose experiments such as CMS. The TOTEM detectors (the telescope 1, telescope 2 and Roman Pots described in Subsections 1.4.3-1.4.5) are small in size, but are very close to the beam and are situated up to 220 m from IP5 (in both directions) following the beam pipe. Special demands for the detectors also imply requirements and challenges for the mechanical construction and detectors design (e.g. precise movable parts, almost edge-less silicon detectors).

The TOTEM physics program covers the following phenomena and measurements: total cross section, elastic scattering, single diffraction, double diffraction, central diffraction and hard diffraction (alone and with CMS). In Figure 1.7, three of these measurements are illustrated and they show the role of individual detectors. The first example is the elastic scattering. If there is no energy transfer between the particles during a collision, but only momentum transfer, then the event is elastic (Figure 1.7(a)). Both protons are preserved and they scatter to small angles (microradians) and may be detected by dedicated detectors (Roman Pots) 220 m far from IP5.

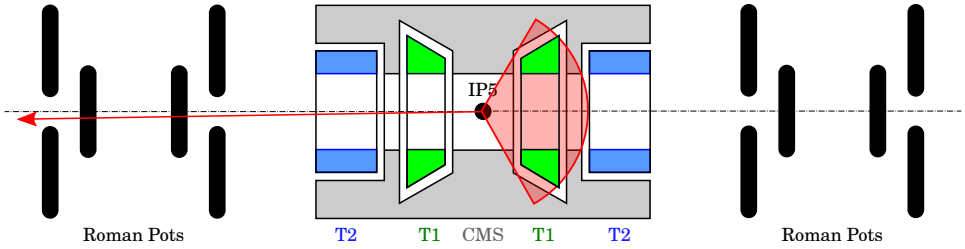
If not only momentum but also an energy is transferred then protons can be destroyed . The process when only one proton survives the collision is called single diffraction (Figure 1.7(b)). In such a case, new particles are created and may be detected by dedicated inelastic detectors T1 and T2.

Directions of those new particles are related to the amount of momentum loss of the surviving proton. In some events, the tracks can reach also the central region. This means that for TOTEM and CMS it is very important to integrate the data from both experiments. This requires to combine their trigger systems.

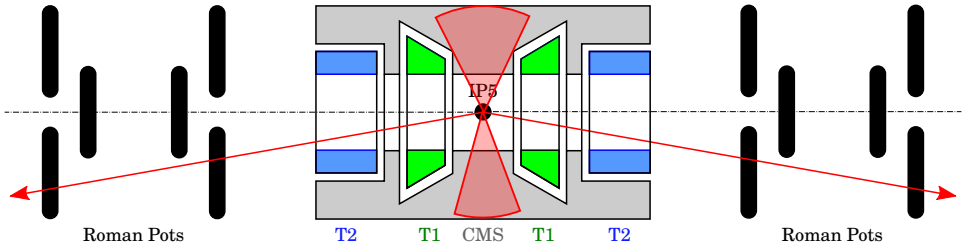
In central diffraction (Figure 1.7(c)), both protons are preserved and detected by the Roman Pots but new particles are also created and detected by the CMS. For this type of measurement,



(a) Elastic scattering.



(b) Single diffraction.



(c) Central diffraction

Figure 1.7: Measurement principles. Various types of processes can be created. This figure shows some of the important ones for the TOTEM experiment: elastic scattering, single diffraction and central diffraction. Surviving protons are represented by red arrow. The red wedge represents area where new particles can be detected.

the joint operations of the TOTEM and CMS experiments gives the maximum physics coverage.

Pseudorapidity

Since measurements of very small scattering angles are needed, it is not very convenient to use the standard linear scale in degrees. The pseudorapidity η provides a useful logarithmic alternative:

$$\eta = -\ln\left[\tan\left(\frac{\Theta}{2}\right)\right], \tag{1.1}$$

where Θ is the scattering angle between the particle and a beam axis. The relation is illustrated in Table 1.4. Using pseudorapidity allows us to display extremely small angles in a simpler way and will be used in the following text.

$Theta, [°]$	$\eta\,[-]$	$\Theta\,[°]$	$\eta\,[-]$	$\Theta\,[°]$	$\eta\,[-]$	$\Theta\,[°]$	$\eta\,[-]$
0	∞	10	2.44	90	0	170	-2.44
0.1	7.04	20	1.74	100	-0.175	175	-3.13
0.5	5.43	30	1.32	120	-0.55	178	-4.05
1	4.74	40	0.88	135	-0.88	179	-4.74
2	4.04	60	0.55	150	-1.32	179.9	-7.04
5	3.13	80	0.175	160	-1.74	180	$-\infty$

Table 1.1: This table shows conversion values between the scattering angle Θ in degrees and the pseudorapidity η [21].

1.4.1 Electronics overview

In TOTEM, all three detectors vary in size and in types of sensors. On the other hand, all detectors share components and technologies for the read out, the data transmission and their control. Figure 1.8 represents a general block diagram of the electronics. This diagram is

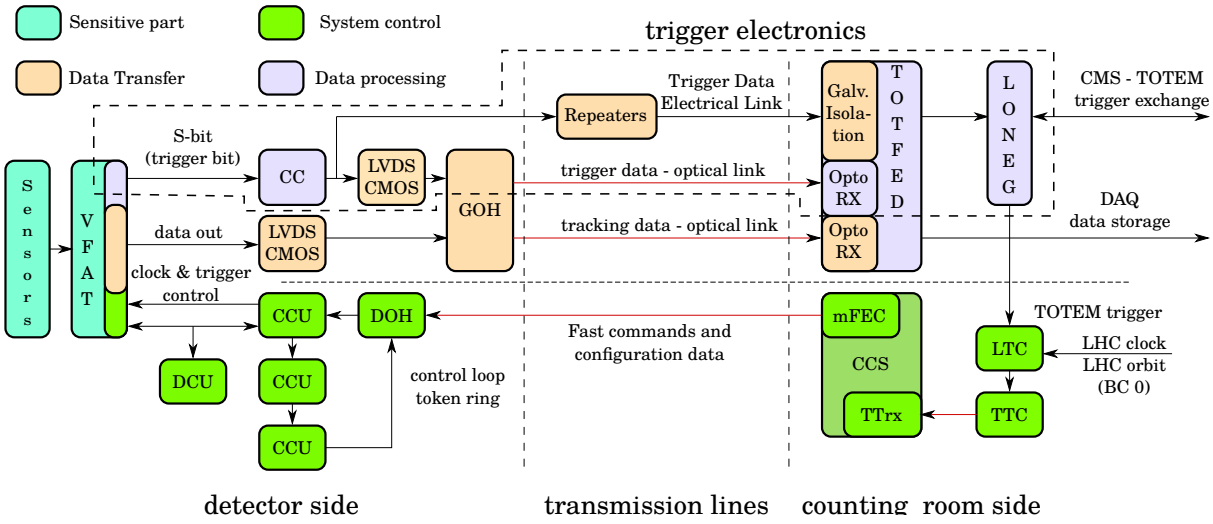


Figure 1.8: Block diagram of the TOTEM electronics. There are four main tasks to be performed by the electronics: data has to be measured, transferred from individual detectors to a single place and processed.

common for all detectors with small variations. In general, there are the following main parts.

- **Detecting (sensitive) part** – sensors and the read out electronics.
- **System control** – configuration of registers, activation of the readout, distribution of the final trigger signal, clock and synchronization signals.
- **Data transfer** – transmission of the tracking and trigger data.
- **Data processing** – storage of the tracking data, analysis of the trigger data and providing the final trigger signal in real time.

Based on its location, the TOTEM electronics can be divided to:

- **Detector side** – ASIC chip based electronics located at detectors exposed to high radiation levels.
- **Counting room side** – Mainly FPGA based electronics located in the CMS counting room.

These two parts are interconnected by up to 300 m long line. The trigger related electronics is also marked in Figure 1.8.

1.4.2 Topology of the TOTEM experiment and the physics coverage of the TOTEM and CMS detectors

The position and the configuration of each detector is crucial for the experiment. Thus many simulations were performed to determine the optimal position of each detector accordingly to the TOTEM physics program. Based on the simulations, three different types of detectors have been designed for the optimal physics coverage:

- Telescope 1 (T1),
- Telescope 2 and (T2)
- Roman Pots (RP).

These detectors vary in the size, location, used sensor and technology. The most important parameters of the detectors are the covered area and resolution. For the TOTEM experiment, it is important to measure very small angles. The particle of interest often leave IP5 almost parallel to the beam. To detect such particles, the Roman Pot detectors are located 220 m from IP5.

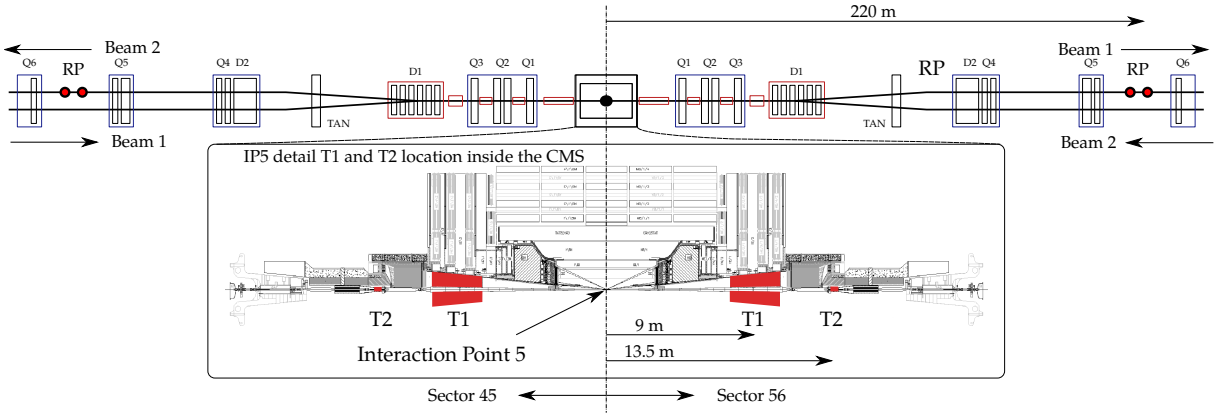
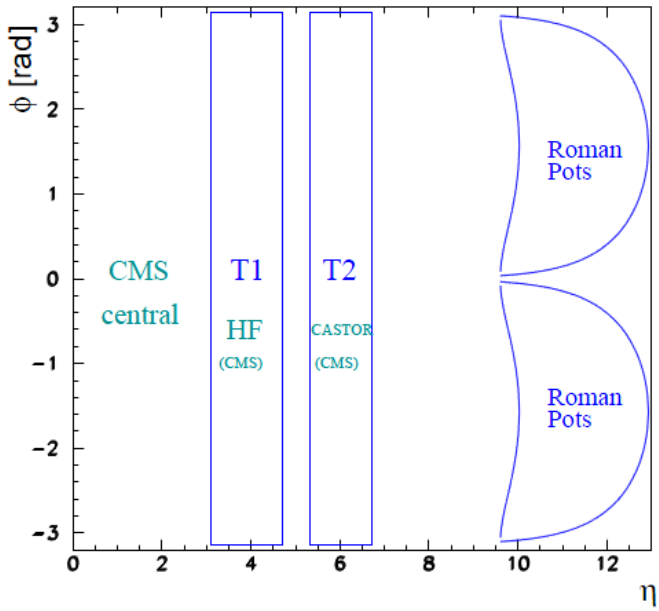


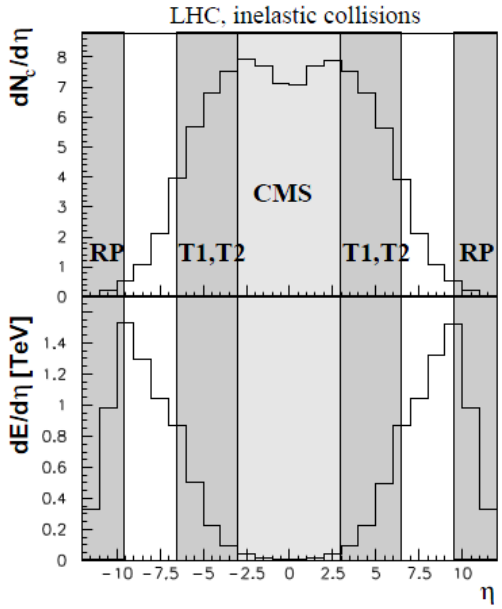
Figure 1.9: There are beams passing IP5 at the top of the image with the Roman Pots positions at 220 m. The bottom part of the image enlarges the middle section around IP5 and it shows the T1 and T2 positions inside the CMS detector. The Q and D labeled boxes indicate quadrupole and dipole magnets positions [14].

The placement of each detector is shown in Figure 1.9. The detectors are placed symmetrically in both directions. The closest to the interaction point is T1 (it has one arm on each side

– Figure 1.11) and is located inside the CMS detector 9 m from IP5 along the beam axis. The second detector is T2 (it has two arms too). It is located at the end-caps of the CMS detector 13.5 m far from IP5 along the beam. The most distant detectors are the Roman pots located 220 m from IP5.



(a) Coverage of the individual detectors in the pseudorapidity (η) and azimuthal angle (ϕ) plane. The area covered by T1 and T2 is fixed. The area covered by RP can vary accordingly to RP position and LHC optics [6].



(b) Charged particle multiplicity and energy flow as a function of pseudorapidity of inelastic events at $\sqrt{s} = 14$ TeV.

Figure 1.10: TOTEM detector physics coverage. The graphs show the expected spacious distribution of the particles and the corresponding coverage of the TOTEM detectors (Source of the graphs: [14]).

Figure 1.10, right, contains simulated (expected) charged particle multiplicity and energy flow. In Figure 1.10, left, there is the designed coverage of the TOTEM and CMS detectors. Those figures show that the TOTEM and CMS experiments cover complementary areas of particle distribution and support the idea of TOTEM/CMS data integration.

1.4.3 Telescope 1

The T1 detector is the largest TOTEM detector. Two so-called "arms" of T1 (one on each side of IP5) fit in the space between two conical surfaces of the beam pipe and the inner envelope of the flux return yoke of the CMS end-cap, at a distance between 7.5 m and 10.5 m from IP5 (Figure 1.9 and 1.12). Each telescope arm is further segmented in two so-called "quarters" (Figure 1.11). The Telescope 1 covers the pseudo-rapidity region $3.1 < \eta < 4.7$. The two quarters are shown in Figure 1.12(b). Figure 1.12(a) shows the installation procedure of the Telescope 1. Each quarter has five planes equally spaced in along the beam pipe.

Each detector plane consist of three individual CSC (Cathode Strip Chamber) detectors. The CSC detector is a type of a multi-wire proportional chamber gas detector.

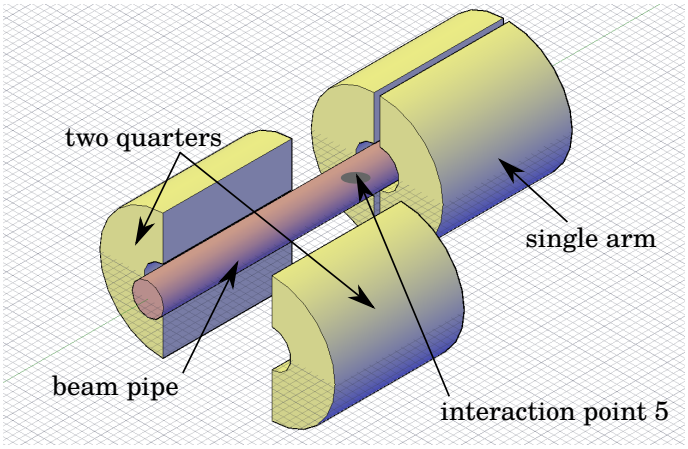
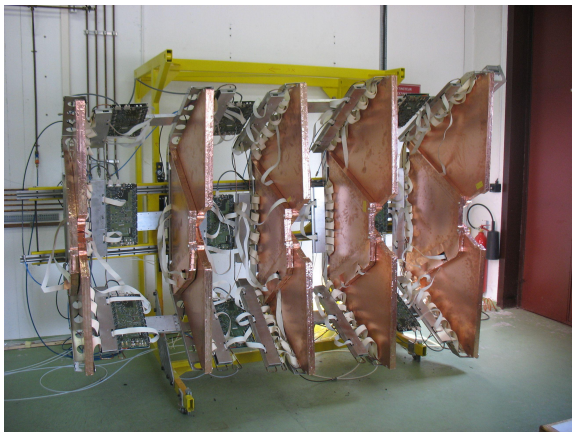
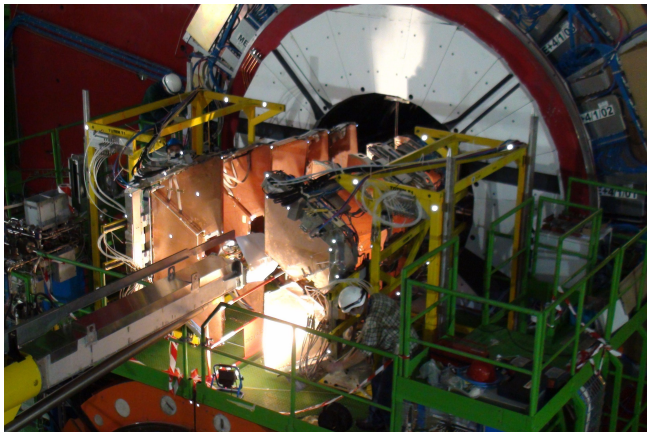


Figure 1.11: Physical segmentation of the TOTEM telescope detectors T1 and T2. Each telescope has one arm on each side of the IP5. Those arms are further segmented in two so-called "quarters".



(a) One quarter of the T1 detector stored in the laboratory waiting for its installation. You can see 5 detectors planes surrounded by the read out electronics. All five planes are made of three individual Cathode Strip Chamber (CSC) detectors.



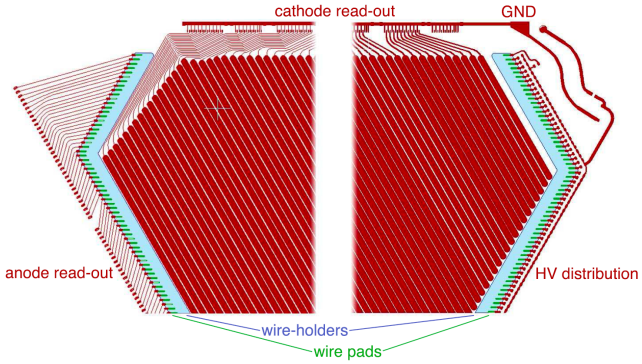
(b) The Telescope 1 during its installation to the end-cap of CMS. The two quarters of the telescope are opened. The beam pipe is visible in the middle.

Figure 1.12: Telescope 1 detector [14].

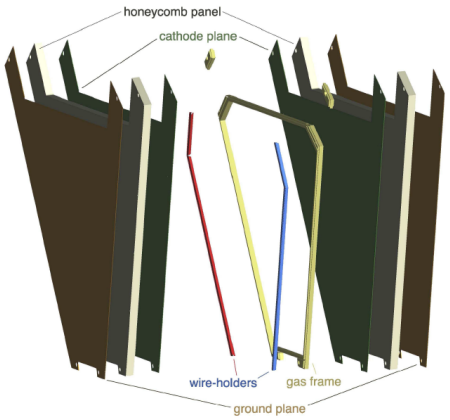
The cathode panels are composite structures, sandwich panels of a standard glass-epoxy laminate with a core of honeycomb that provides the necessary stiffness.

In TOTEM CSC detector, both cathode planes are segmented into strips. These strips and the anode wires are rotated by 60° with respect to each other.

These detectors, in which a single gas gap with segmented cathode planes allows a two-dimensional measurement of the particle position, are well understood. Unfortunately, the gas detectors of this kind are slow. The signal developing time can be up to 100 ns which corresponds to four machine clock cycles (four bunch crossings). Also the ions generated by the crossing particles, start to flood the detectors volume when the luminosity of the LHC accelerator gets too high. This means that T1 can only be used during low-luminosity TOTEM special runs when a small number of bunches is injected.



(a) Cathode strips and wire-holder printed circuit boards.

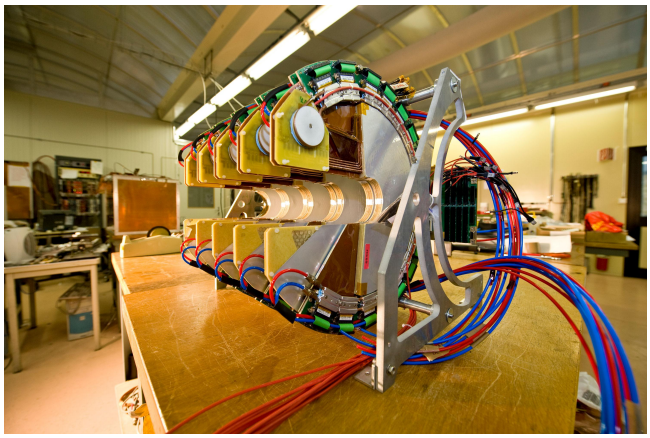


(b) Explode view shows the internal structure of the CSC detector.

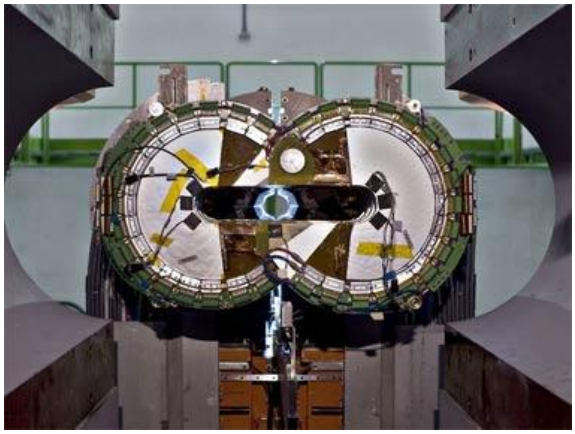
Figure 1.13: Telescope 1 - Cathode Strip Chamber detector overview [14].

1.4.4 Telescope 2

T2 is located at 13.5 m far from IP5 inside the end-caps at the very end of the CMS detector between the vacuum chamber and the inner shielding of the HF calorimeter (Figure 1.9 and 1.14). T2 covers the pseudo-rapidity range of $5.3 < \eta < 6.5$.



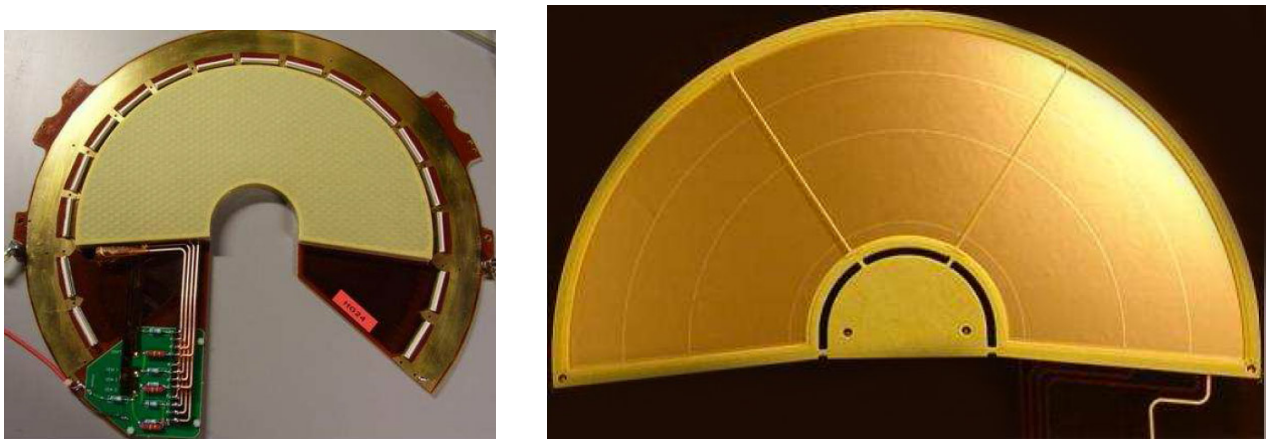
(a) One quarter of the T2 detector on a laboratory table. All five planes are made of a single piece of Gas Electron Multiplier (GEM) detector.



(b) Two quarters of one arm of T2 before closing at the end-cap of CMS. In the middle, there is the beam pipe.

Figure 1.14: Telescope 2 detector [14].

The T2 detector was designed for a good coverage of interesting forward-physics processes taking into account various beam conditions. This includes low-luminosity (total cross-section and soft diffractive scattering) measurements and moderate-luminosity (semi-hard diffractive scattering, low-x physics) measurements. As well as for T1, it is not possible to operate T2 during high-luminosity measurements. In comparison to T1, T2 is smaller in size but it has a better resolution. It also uses a gaseous detector type sensor but with different technology - Gas Electron Multiplier (GEM) (Figure 1.15).



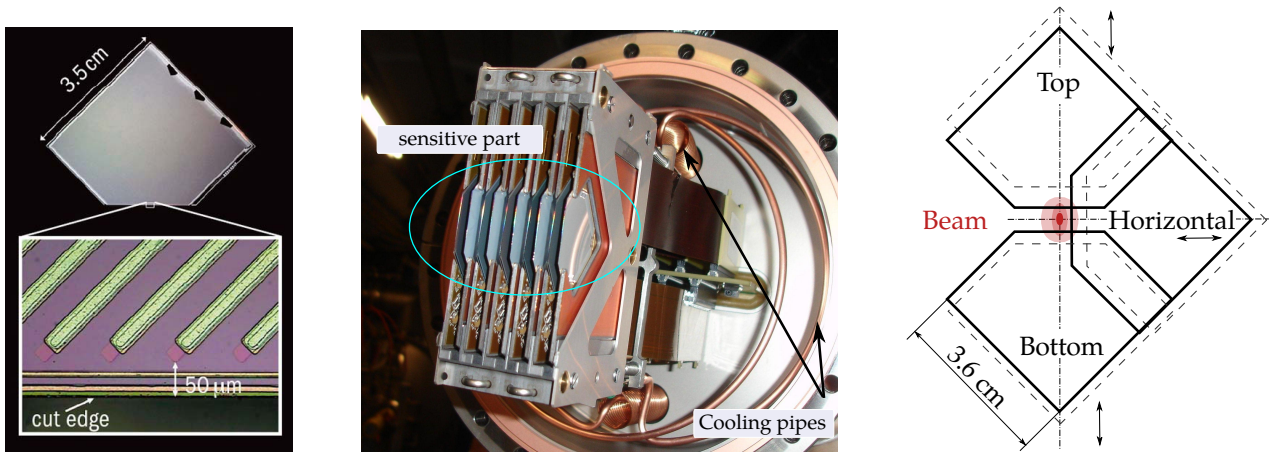
(a) T2 Gas Electron Multiplier With the high voltage divider without frond-end electronics

(b) The T2 GEM foil glued to the support.

Figure 1.15: Telescope 2 GEM detector plane [14].

Those detectors have been selected for their high rate capability, good spatial resolution, robust mechanical structure and excellent ageing characteristics.

1.4.5 Roman Pots



(a) Each edge-less silicon strip detector contains 512 reverse-biased diodes as a particle sensitive area.

(b) Detector planes of a single Roman Pot detector are grouped by five in two orthogonal projections u and v. Compared to pixel detectors, strip configuration reduces amount of measured data, but allows only single track reconstruction.

(c) Once inserted, the silicon detectors surround the beam. Movable configuration allows detectors to optimize their position accordingly to different beam configurations

Figure 1.16: Silicon sensors of the Roman Pot detectors allow a detection of collision surviving particles [14].

The Roman Pot detectors purpose is to detect collision-surviving-protons that come from IP5. Such protons leave the collision under a very small angle and follow to the beam. To

detect these particles, the Roman Pot detectors are located at 220 m from IP5 symmetrically on sides (Figure 1.9).

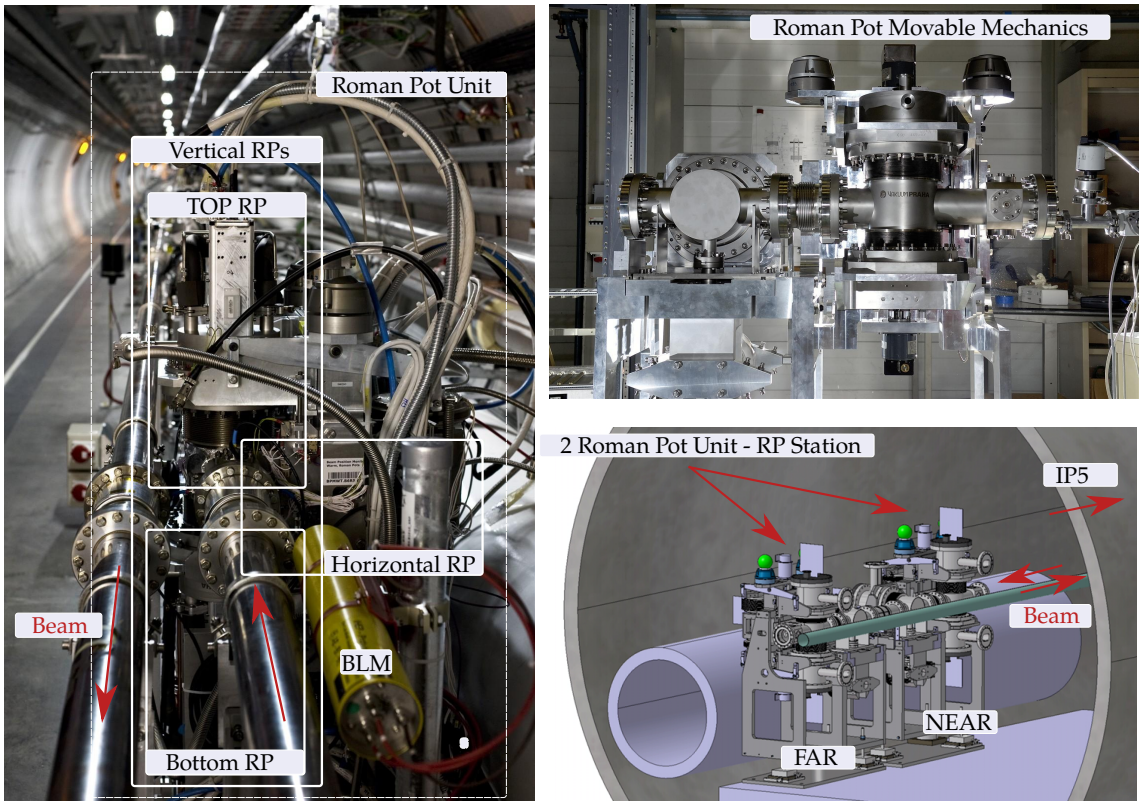


Figure 1.17: Mechanical construction of the Roman Pots. Detectors are grouped in a unit by three (two verticals – the top and bottom – and one horizontal). On each side of IP5, there are two units called near and far) [14].

To achieve the optimal performance and the minimal distance from the beam, specially designed almost edge-less silicon strip detectors are used (1.16(a)). The beam cross-section and orbiting trajectory position varies during the beam injection phase. Beam parameters are also affected by the LHC magnets optics. This all together means that it is not possible to install Roman Pot detectors to a fixed position. For this reason a special construction, the so-called "Roman Pot", has been developed (this mechanical construction gives the Roman Pot detectors their name). Its main function is to allow detectors to move close to the beam once the beam desired parameters are achieved. The movement can be executed with a micrometer precision. Roman Pots also provide a vacuum chamber for the silicon detectors (remaining electronics is under the atmospheric pressure) and separates the primary vacuum of the LHC accelerator and the secondary vacuum of detectors (this allows detector replacements without breaking the primary vacuum, and it protects the primary vacuum in case of device failure). The Roman Pot construction also provides cooling for all the silicon chips in the secondary vacuum.

The Roman Pot detectors are grouped in the so-called "units". Figure 1.17, left, shows one unit which contains three Roman Pots (two verticals – the top and bottom – and one horizontal). At each side, there are two units called a near and far unit (based on their location towards IP5), together forming one Roman Pot Station.

Chapter 2

TOTEM trigger system

All TOTEM detectors generate large amount of tracking data every single clock cycle and a continuous read out of all data is not technically possible and even not desired. Dedicated electronics is continuously buffering all the data locally, monitoring and analyzing all events and executing the consecutive buffer data read out when certain criteria are met. In real time, in parallel, all detectors are generating simplified information about their states the so-called "trigger information". The dedicated electronics, the so-called "trigger system" (or just the trigger), is evaluating every collision and executing the data acquisition (DAQ) that reads the corresponding buffered tracking data.

During the development of the Totem trigger system, the following assumptions had to be taken into account that trigger system:

- is a mechanism that evaluates all events and selects a subsample to be acquired by DAQ,
- is the first step in the data analysis and is critical for the consecutive offline data analysis (the data that are not triggered on and stored by DAQ are lost),
- is significantly affecting/reducing the transmitted and stored data volume,
- optimizes usage of the available data bandwidth and
- requires precise and extensive timing studies and calibrations.

The TOTEM trigger system uses a tree structure (Figure 2.1) which is important for the step-by-step data volume reduction. This structure has two main parts which are based on the physical location and surrounding environment.

Detector side

This part of electronics is physically located at or in a short distance from individual detectors in a proximity to the LHC beams. This means that this electronics is exposed to high radiation levels. For this reason, special radiation hard ASIC chips have been developed by the CERN Electronics Group. This part is also designed to significantly reduce the amount of the trigger information generated and transmitted to minimize requirements for a data-transfer over a long distance.

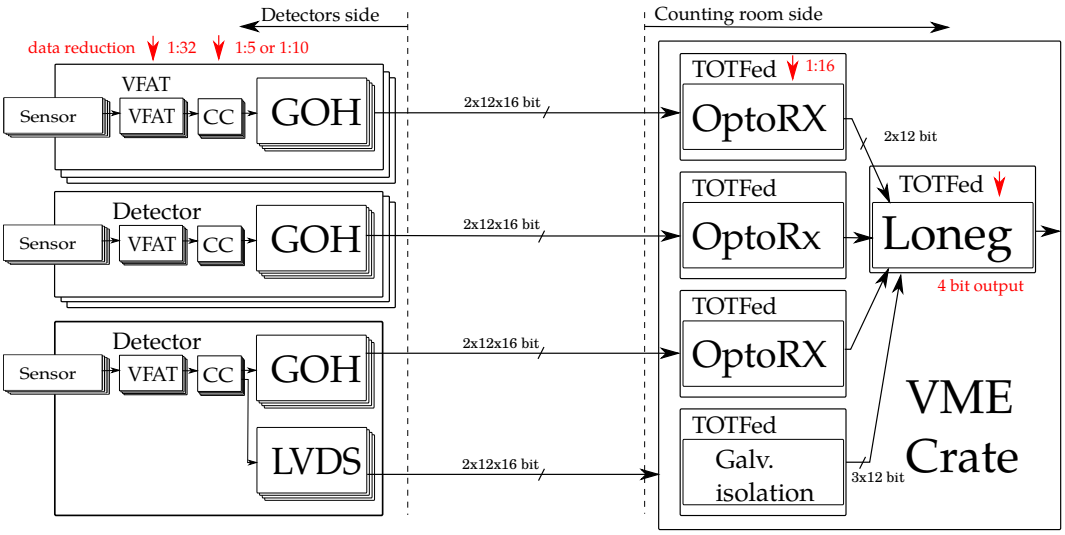


Figure 2.1: TOTEM trigger tree structure. The reduced sub-sample of data measured by individual detectors is send continuously to one central place located in the CMS service cavern. Once the data are received from each detector, each event is evaluated and the tracking data read out is requested if predefined criteria are met.

Counting room side

The counting room is located in the CMS service cavern (USC-S2) and it is shielded from radiation. This means that complex-memory-based components such as FPGA chips allow to develop the complex final stage of the trigger logic. Using FPGA, the trigger system can be easily updated accordingly to the TOTEM physics program needs.

2.1 TOTEM trigger menu

During each measurement, the TOTEM experiment can study various types of interactions. The trigger system has to be able to analyze and process different events accordingly. To do this, the trigger information enters individual logic blocks in parallel. The logic Blocks generate a bit-vector of individual triggers for each physics scenario separately. In the final step, these trigger bits are used to generate the final trigger signal and they are also stored by DAQ together with tracking data to allow trigger efficiency studies (described later in this section).

Each type of interaction has a different probability to occur and the trigger rates of the individual scenarios can vary by orders of magnitude. This is an issue when DAQ starts to fill its band-width and rejects trigger requests (random events are lost). To avoid this, the trigger system has to be able to “prescale” the triggers for individual scenarios. In such case, during the offline analysis, the event loss can be compensated. This set of individual trigger schemes is called “trigger menu”.

The TOTEM trigger menu typically consists of several important physics event types:

- **bunch crossing event** signal is generated when any populated bunch passes IP5.
- **minimum bias event** refers to at least one trigger bit from any detector active.
- **elastic event** corresponds to coincidence of active roman pots on both sides of IP5.
- **single diffraction event** has the Roman Pot and Telescope 2 active etc.

The list of individual physics events [1] grows as the TOTEM physics program evolves.

Multiple collisions can (and they do) occur during a single bunch crossing. This is the so-called the "pile-up". Due to TOTEM instrumentation resolution in time and space, detectors receive a cluster of data containing information about multiple interactions. For a data analysis, it is a non-trivial task to correctly disentangle and reconstruct individual interactions. At the trigger level, the situation is even more complicated because a reduced set of data is analyzed.
.

2.1.1 Trigger system performance

To evaluate the trigger overall performance the following two parameters are important.

Trigger system purity

The trigger purity refers to the capability to filter out events that do not meet the requested physics criteria and is estimated during physics offline analyses using the bunch crossing sub-sample of stored data. Each event in the sub-sample is analyzed and two conditions are checked:

- trigger bit corresponding to the selected physics criteria is set (tagged) and
- the event meets the selected criteria.

Trigger system purity defined as follows:

$$\nu_{trigger} = \frac{\text{N(event of type T \& event tagged as type T)}}{\text{N(event tagged as type T)}}, \tag{2.1}$$

where ν is a trigger purity, N is a sum of events meeting criteria in the sub-sample and T corresponds to the selected physics criteria.

Trigger system efficiency

The trigger system efficiency is a complementary parameter of the trigger purity and refers to the capability to correctly identify events. It is estimated:

$$\mu_{trigger} = \frac{\text{N(event of type T \& event tagged as type T)}}{\text{N(event of type T)}}, \tag{2.2}$$

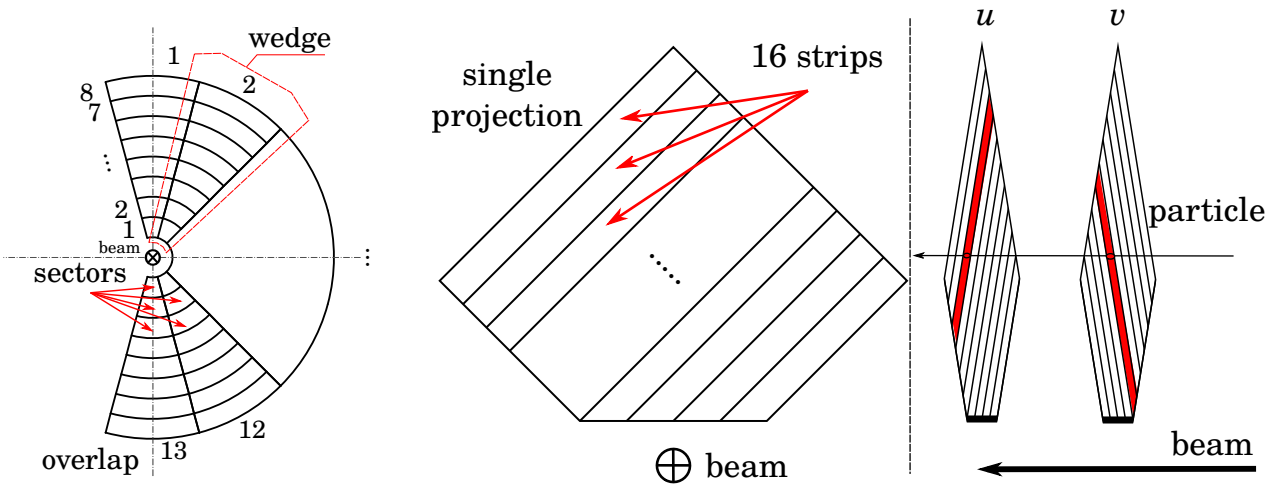
[1] When talking about events, it has to be distinguished between real physics events and events as seen by the detector. The second one is limited by apparatus properties like resolution etc.

where μ is the trigger efficiency, N is a sum of events meeting criteria in the sub-sample and T corresponds to the selected physics criteria.

It is very difficult to optimize trigger efficiency and trigger putity in the same time. To do so, a smart cut (an event rejecting condition) has to be applied by the trigger logic (e.g. a coincidence between specific detectors[2]). On the other hand, any cut creates a bias in stored data. If the bias is well understood then it can be corrected and data can be normalized. In case that number of generated triggers is such that DAQ starts to be overloaded and rejects trigger requests, then the bias in the stored data is unknown and cannot be easily compensated. This should never happen. In such case, the only acceptable solution is to prescale[3] the trigger signal.

2.2 Electronics related to the trigger system

Due to the very high complexity of the system, it is not possible to describe individual components in detail. However, it is important to briefly overview properties of the relevant electronics components to have an overall understanding of the system.



(a) T2 detector is segmented to 13 wedges. Each wedge contains 8 sectors.

(b) Roman Pot detectors uses two orthogonal projections u and v with strips segmntation. The trigger system can use different coincidence of those two projections.

Figure 2.2: Detector segmentation for the trigger system.

The most important parameter for the trigger system is the resolution of individual detectors on the trigger level. It defines and limits possible implementations of trigger algorithms. In the control room, each detector is monitored and trigger bits are processed in real-time. Each the 10 planes of a single T2 quarter are reduced to pixel matrix shown in Figure 2.2(a). Its area is divided to 13 wedges and each wedge contains 8 active sectors. This reduction is done using the VFAT chips (Sub-section 2.2.1) coincidence chips (Sub-section 2.2.2). In contrast to T2, individual Roman Pots are seen as two orthogonal planes divided to 16 strips each (Figure

[2]For example, a coincidence between the Roman Pot detectors on both sides of the interaction point reduces significantly trigger rates and preselects mostly elastics events.

[3]Prescaling means taking one event every N events. This reduces the mean rate by a factor N

2.2(b)). This representation leads to a significant reduction of detector resolution which is still sufficient for the trigger system.

2.2.1 The Very Forward Atlas and TOTEM chip

The Very Forward Atlas and TOTEM (VFAT) chip [9] is a tracking front-end ASIC chip. It was designed by the CERN Microelectronic Group as a read out chip of the sensors for the TOTEM and ATLAS experiments. It is one of the corner stones of TOTEM detectors. The main functionality of VFAT is:

- to receive analog signals from sensors (each VFAT has 128 inputs),
- to process, amplify, shape and compare the result with programmed threshold values to produce digital tracking and trigger data,
- to store the tracking data in the local buffer for the potential read out,
- to provide reduced information about the tracking data for the trigger system in real-time,
- to transmit the locally stored tracking data when requested and
- to reliably operate in high radiation environments.

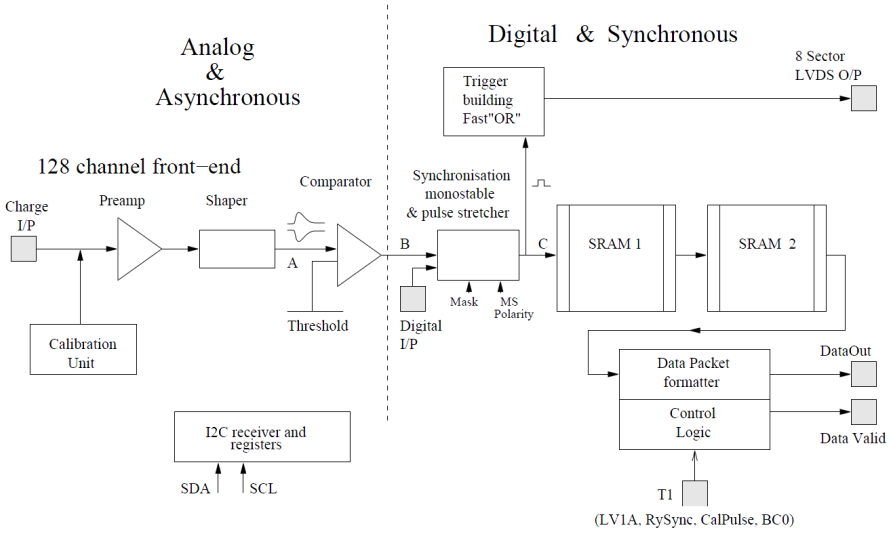


Figure 2.3: This VFAT block diagram shows its internal structure. The VFAT chip is responsible for the TOTEM detectors read out. It is divided in two parts. The analog part amplifies the collected charge from the detector, shapes the signal and compares it with desired threshold values. Accordingly, a digital pulse is generated. In the digital part, the trigger signal is generated and in parallel tracking data are stored in the local buffer SRAM1. Once the read out request is received, the corresponding data from SRAM1 are copied to the transmitter buffer SRAM2 and transmitted out (for more details see [9]).

The VFAT block diagram is in Figure 2.3. The internal part of the chip is divided into the analog and digital sections. The analog part amplifies the signal from the sensor and compares

it with the threshold value. The digital part propagates the tracking and the trigger information to the rest of the system. This part contains two memory blocks and the logic for the data read out and the fast OR logic block for the trigger computation. The tracking information is stored in the local buffer (SRAM 1) and in parallel the reduced trigger information is send. The tracking data are stored into the buffer continuously. Once the read out trigger request is received the data from the specific buffer slot are read and stored into the transmitter buffer (SRAM 2). The read out pointer for SRAM1 is programmable. This allows us to compensate different signal propagation delays (latency) for individual detectors. Once stored in SRAM2, those data are automatically sent out from the chip and collected by DAQ.

2.2.2 Coincidence Chip

Particles colliding in IP5 hit the detector under very small angles. In fact particles produced by showers inside the LHC beam pipe are incoming mostly under large angles and they are rejected by this mechanism. The Coincidence Chip (CC)[20] is designed specially for the trigger

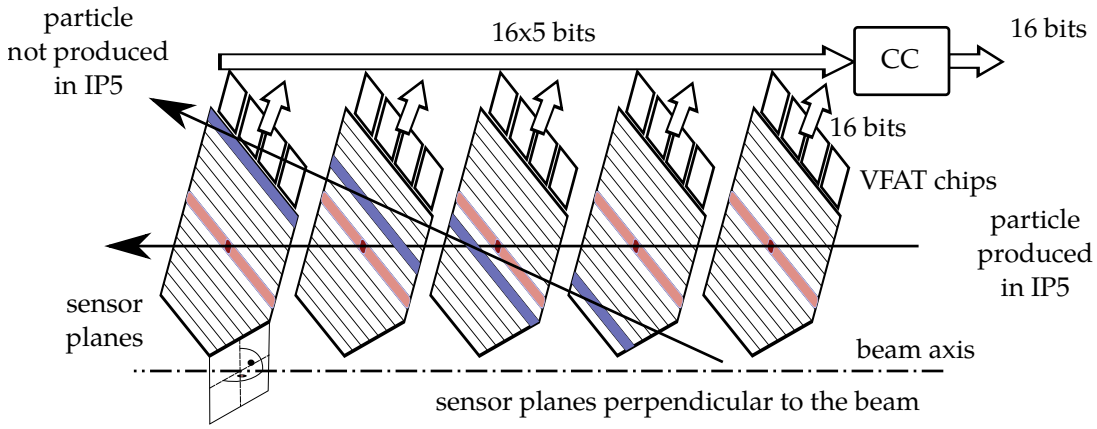


Figure 2.4: Function of the coincidence chip. The Coincidence Chip takes into account positions of activated areas in the set of planes. If a predefined number of active sectors corresponding to the same row in the plane set is found then the trigger signal is propagated.

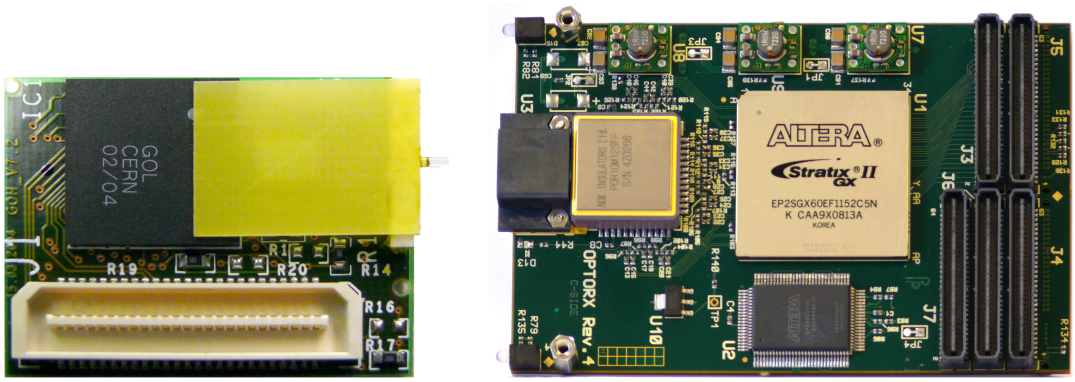
of the T2 and Roman Pot detectors. This chip is located in a proximity of VFAT chips. It checks the coincidence of the trigger bits in individual sensor planes to reduce the amount of the trigger bits and to eliminate the noise and particles not produced in IP5.

Figure 2.4 illustrates CC usage in the Roman Pot detectors (the principle is very similar for the T2 detector too). Five orthogonal silicon strip detector planes are aligned with the beam axis. For trigger purposes, each plane containing 512 sensitive strips, is segmented by the VFAT chips to the sixteen logical groups. Each group is represented by one trigger bit signal. CC makes an individual sum of the active trigger bits from groups in the same column and compares the sum with a threshold value. If the sum is greater or equal than the threshold value then the corresponding CC trigger bit is generated. There are two examples in Figure 2.4. If the particle trajectory is almost perpendicular to the planes (almost parallel to the beam axis), which is the case for physics tracks, then the same area is activated in each plane and the group of corresponding trigger bits reaches the threshold. Thus the trigger signal is propagated. If the angle between the beam axis and the particle trajectory is large enough then different

areas are activated (particles are produced close to RP). In such a case the trigger bit is not propagated. The number of planes in a row reduces amount of trigger bits: by factor five for the Roman Pots and by factor ten for T2.

2.2.3 GOH and OptoRX modules for the Optical trigger

The Gigabit Optical Hybrid (GOH, Figure 2.5(a)) is another module developed by the CERN Micro Electronic Group for optical data transmissions. GOH is based on an ASIC chip GOL [22] (Gigabit Optical Link) which is designed as a radiation hard circuit thus it can operate inside detectors while exposed to high radiation levels. This chip uses a 16 bit wide input bus at 40 MHz. It uses a 8 to 10 bit encoding to generate 800 Mbits^{-1} output bit stream.



(a) GOH module based on the ASIC GOL chip (the transmitter module).

(b) OptoRX mezzanine (the receiver module for up-to 12 GOH links).

Figure 2.5: Main components of the optical data transmission line used for the TOTEM trigger system.

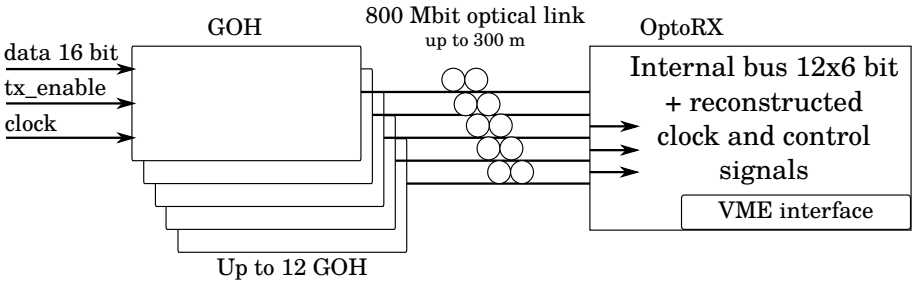


Figure 2.6: Block diagram of the optical link. Once the tx_enable signal is asserted, the GOH module converts the parallel bus into the optical data stream. The OptoRX module can receive those data-streams form up-to twelve GOH modules and convert it back to parallel buses. The data stream uses 8 to 10 bit coding and uses 800 MHz modulation frequency.

The OptoRX module (Figure 2.5(b)) was designed as a TOTFed card mezzanine (see Subsection 2.2.4). The main functionality is to receive optical data streams from up to twelve independent GOH modules that are transmitting at 800 Mbits^{-1}. The card holds a Stratix II GX FPGA for this purpose. This FPGA contains 12 dedicated hardware receivers (the link block diagram is in Figure 2.6). The OptoRX is used for DAQ and the trigger system as well. The

number of logic elements in FPGA also allows the complex trigger logic implementation. To reduce the development time, the DAQ VME interface and internal registers blocks are used. This part allows writing and reading register values via the VME interface thus those registers are used for the system configuration and the data readout.

2.2.4 TOTFed

The TOTFed board (the TOTEM Front EnD) is shown in Figure 2.7 (additional mezzanine cards are shown as well). It is a plug-in card developed for the standard VME 64x crate. It contains four Stratix I FPGA chips equipped with a USB interface and SRAM memory blocks. Three chips are dedicated to corresponding mezzanine slots. These chips are designated Main 1, Main 2 and Main 3. The fourth FPGA is called "Merger" and it is dedicated to combine three 64 bit wide buses from each Main FPGA. It also provides an S-link mezzanine connectivity. In the trigger system,the Merger and S-link slots are used for the LONEG mezzanine card and connector mezzanine cards (see Sub-section 2.2.5).

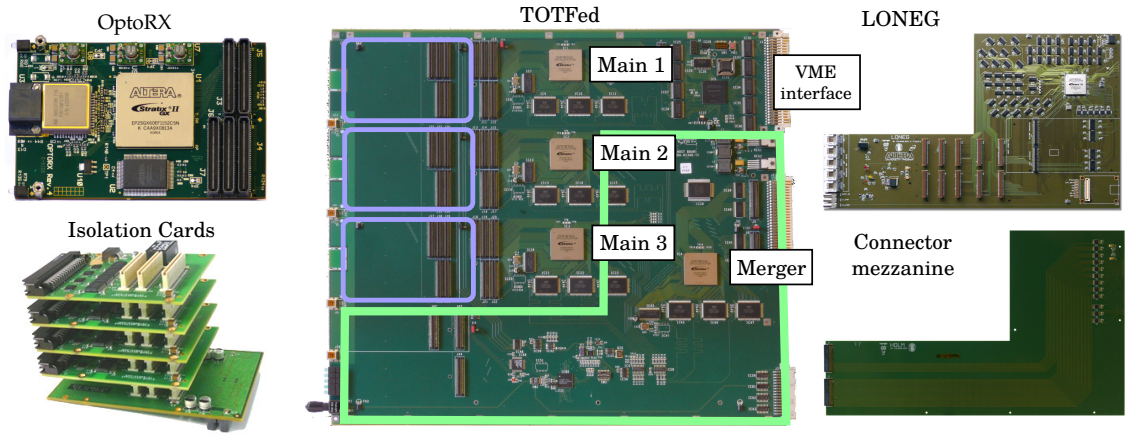


Figure 2.7: Overview of the mezzanine cards for TOTFed. Those cards extends the functionality and connectivity of the TOTFed. The mezzanine cards are described in Chapters 2 and 3.

The common VME interface is controlled by a dedicated VME interface Cyclone III FPGA. Another important part of the board is a TTC block which receives LHC machine signals and provides the board with the LHC synchronous clock and control signals. This precise timing is essential for the trigger system synchronization.

2.2.5 LONEG and Connector mezzanine card

The trigger signals from the individual TOTFeds are propagated via Mergers and Connector mezzanines to the LONEG card - Level ONe triggEr Generator (Figure 2.8). The LONEG card, together with Connector mezzanine cards (Figure2.7), was specially designed to provide sufficient amount of connectivity for individual trigger signals. There is a CMS interface connector set that allows the trigger exchange between the TOTEM and CMS experiments. Next to it, there is the Level One trigger output. Ten extra connectors allow up to five additional TOTFed to be connected. The on-board Stratix II FPGA chip also provides sufficient resources for the final trigger algorithms. The card also receives LHC clock from the parent TOTFed board. Thus it is fully synchronous with the rest of the trigger electronics.

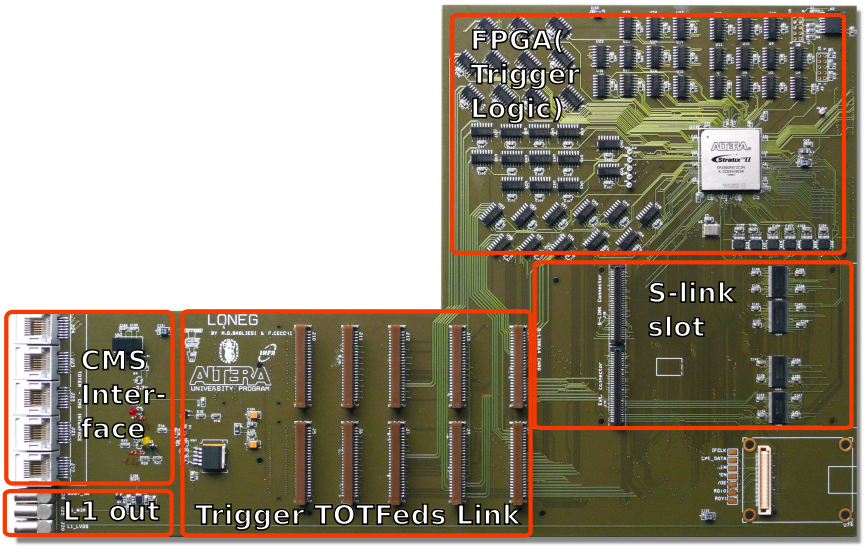


Figure 2.8: LONEG mezzanine contains the final stage of the TOTEM trigger logic.

2.2.6 VME crate and an usage of the VME interface for the system configuration

All the TOTEM FPGA based trigger electronics is installed in the VME trigger crate in the trigger rack located on floor -1 of the CMS Underground service cavern. This VME crate provides necessary power and configuration capabilities. The VME bus is connected to the computer (located in the same room) by the CAEN VME controller card (Figure 2.9). This computer is connected to the CMS technical network and allows the remote access from multiple machines in the TOTEM control coom. The CMS technical network is separated by a firewall from the rest of the CERN network but this can be bypassed using SSH tunneling (this allows completely remote access).

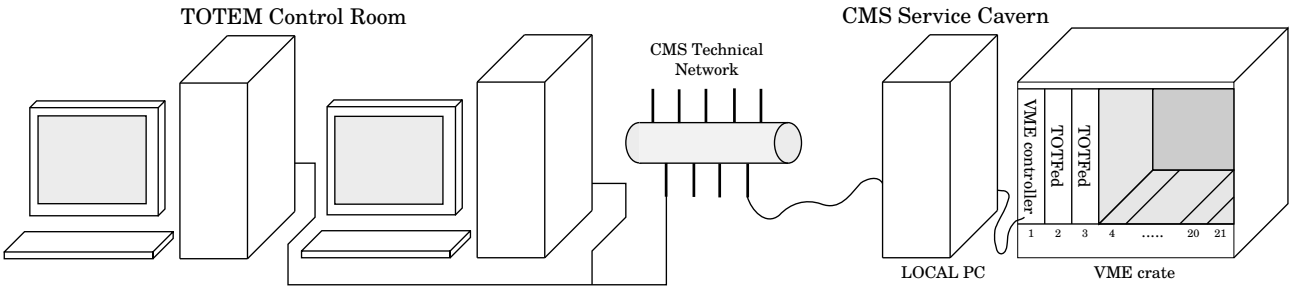


Figure 2.9: Interfacing the VME crate. The VME crate is connected to a locally installed computer via VME controller interface. A connection of the PC to the CMS technical network allows a remote access.

The Linux operating system is used for all machines interfacing the trigger system electronics and provides us with comfortable and stable development environment. In the moment, most of the trigger system configuration is done by bash scripts. These scripts give full control over the system and allow modify individual parameters during the physics measurement.

To configure trigger devices, a shared VME crate memory space with 32 bit addressing is used. According to Table 2.1, the most significant address bits correspond to the physical location in the VME crate slots. The following set of bits is used to determine local chips on the VME card (Table 2.2 contains a local chip addresses for TOTFed). The sub-address bits corresponds to possible mezzanine devices. Register select bits are used to access registers in corresponding devices.

VME crate address space																														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phys. address address					local device			sub address					register select																-	-

Table 2.1: VME crate address space. The VME space address space is defined by its 32-bit-wide address. It is shared between all twenty one physical slots for the cards and individual local devices.

The most problematic addressing and data access is related to the Main mezzanine cards VME access. The Main chip is capable to propagate limited number of addresses and data bits to its mezzanines. This is the bottleneck for OptoRx module access. Its directly addressed register space is limited and indirect addressing had to be used in most cases. Also the OptoRX data-bus is limited to 16 bits.

Local device address	Local device
0	VME
1	MAIN 1
2	MAIN 2
3	MAIN 3
4,7	reserved
5	mFec connector (used for LONEG)
6	Merger

Table 2.2: Local device address for the TOTFed devices.

card type	purpose	plugged in	occup. slot(s)	remark
VME contr.	PC/VME bus interface	1	1	-
Fiber splitter	TTC optical fiber splitter	-	2	-
TOTFed	RP147 45/56 trig. receiver	3	3 and 4	to be removed
TOTFed	RP220 45/56 trig. receiver	5	5 and 6	optical
TOTFed + LONEG	T2+ NR&FR Trig receiver	8	8 and 9	optical
TOTFed	T1 trigger receiver	10	10 ans 11	optical
TOTFed	T1 trigger receiver	12	12 and 13	optical
TOTFed	T2- NR&FR trig. receiver	14	14 and 15	optical
TOTFed	RP 220 trig. receiver	17	17 and 21	electrical

Table 2.3: Usage of the VME trigger crate

The VME register addressing firmware for individual FPGA devices is shared by TOTEM DAQ and TOTEM trigger system. The DAQ VME interface code was extended to provide

device	purpose	type	max. reg.	data-bus width [bits]	base address
Main	El. trigger	RO	2^{15}	32	0083 0000
Main	El. trigger	RW	2^{15}	32	0084 0000
LONEG	Final trigger	R0	2^{15}	32	0004 0000
LONEG	Final trigger	RW	2^{15}	32	0008 0000
OptoRX	DAQ / HW de-serializer	RW	2^{7}	16	0000 0000
OptoRX	Opt. trigger	RO	2^{7}	16	0018 0100
OptoRX	Opt. trigger	RW	2^{7}	16	0018 0200

Table 2.4: Base addresses of registers spaces used for the trigger system.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP 220 m opt.	0	0	1	0	1	⇐ physical location of the card																										
Main 2						0	1	0	⇐chip board address																							
BA RW	reg.base address⇒								0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
Reg. 5	register address⇒																											1	0	1		
result	0	0	1	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	final address in HEX: 0x2A180214																															

Table 2.5: Example how to obtain a register address. The example shows how to obtain the address of RP220 optical trigger board (slot 5), OptoRX 2 mezzanine firmware (space is shared with the Main 2), trigger read/write register 5.

additional control registers. For individual devices, different base addresses (register select part of the address) are used. The list of base addresses important for the trigger system is in Table 2.4. Table 2.3 shows an overview of the currently installed devices in the trigger VME crate.

To summarize, Table 2.5 shows an example how to determine the register address. In this case, the address corresponds to trigger Read/Write register number five of OptoRX two of Roman Pots 220 m optical trigger TOTFed.

Chapter 3

Implementation of the TOTEM trigger system

The author started to work on the TOTEM trigger system when most of its relevant hardware had been installed at IP5. However, there was basically no firmware written for the trigger system and it had to be developed from scratch.

In that time, LHC started its operation. This meant to develop and update the trigger system firmware continuously during its operation (this affected the entire firmware development). To reduce the necessary development time, the firmware inherited the registers blocks and VME interface made by our DAQ group. In the first step, the optical trigger path (described in Chapter 2) was used for all detectors. This required the OptoRx firmware to receive trigger signals from the individual detectors and provide the adequate trigger logic for them. The author's first work on the TOTEM trigger system is described in Section 3.1. He wrote the OptoRX trigger firmware for the T2 and Roman Pots detectors (the firmware for the T1 was developed in parallel by other members of the group, by modifying author's firmware). Finally, the Roman Pot Optical trigger had to be replaced due to its too high latency which prevented the trigger signal exchange between TOTEM and CMS. The Roman Pot detectors were designed with a possibility to propagate the trigger signal electrically in parallel with the optical one. The author's further task was to implement an electrical link called "Electrical trigger", between the Roman Pot detectors and the counting room. Thus Section 3.2 describes his work on the signal repeating devices, galvanic isolation devices, cabling and installation. This includes their prototyping, design (schematics, layout), production and installation. Section 3.3 describes the author's work on the Electrical trigger related firmware.

The author also participated in the LONEG card firmware. This work was shared among four people. However, the LONEG card is the core of the TOTEM trigger system thus it's firmware is briefly described in Section 3.4.

3.1 Optical trigger firmware

Located in the OptoRX mezzanine, the optical trigger firmware was developed to receive and process trigger information from the T2 and Roman Pots detectors. Figure 3.1 shows its block diagram.

In each OptoRX FPGA (Stratix II GX), there are twelve hardware transceiver blocks based on 8 to 10 bit encoding (Subsection 3.1.1), configured and used as receivers of the trigger bit streams transmitted by the individual detectors by their GOH modules. These receivers decode and is driven by the LHC synchronous clock which is encoded in the data streams. The trigger logic blocks use a locally distributed LHC clock. It means that the trigger data have to cross from the receiver clock domains to the FPGA one (the clock frequency is the same but with an unknown phase). Thus FIFO buffers and controlling FSM for each block had to be implemented. If detector's PLL is unlocked, then data skews are detected by FSM and an error signal is generated and counted by a control scaler. Also FIFO's underflow and overflow signals are monitored in real-time.

The total amount of bits received by single OptoRX is up to 192 (2x8 bits per receiver). A possibility to mask individual signals on a bit level is needed due to the noisy channels. Thus a set of masks is implemented in the firmware.

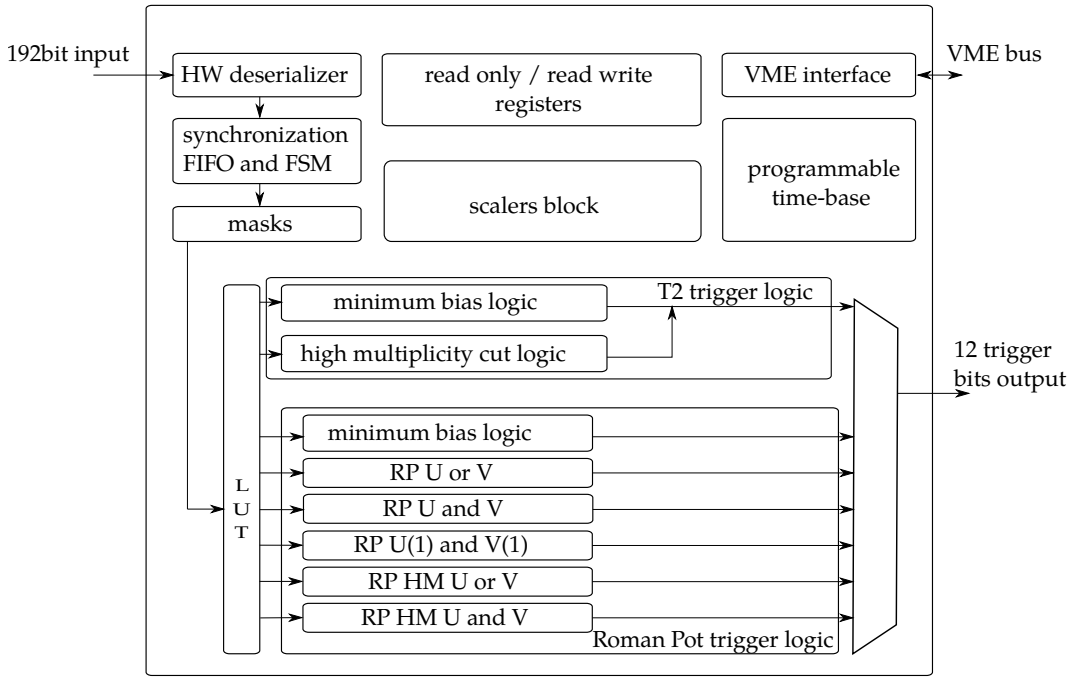


Figure 3.1: Block diagram of the OptoRX firmware. The firmware contains blocks responsible for a correct reception of the trigger optical data (synchronization, masking), blocks with the trigger logic for each T2 and RP detectors, a scaler block for the trigger monitoring and sets of registers for the system configuration.

The trigger logic blocks (Subsection 3.1.2) contain combinational logic and look-up tables (LUT) to cover needs of pre-processing and reducing amount of trigger bits at the individual detector level for the T2 and Roman Pot detectors including a minimum bias and high multiplicity cut trigger.

The scaler Block and programmable time (Subsections 3.1.3) base are used for continuous real-time monitoring which is important for system calibrations. Also the information about the trigger signal rates received from individual detectors is very important. Thus a large number of counters with a predefined integration time, the so-called "scalers" is implemented in the OptoRx trigger firmware. The scalers are also used to monitor deserializer block error signals.

The VME interface and register blocks are implemented in the OptoRX firmware (see Subsection 2.2.6). This part allows a comfortable configuration and data readout of the board.

3.1.1 Hardware deserialiser, synchronization logic and masks

The optical data streams (8 to 10 bit encoding is used) from individual detectors are converted to electrical signals by the on-board electronics of the OptoRX and enter the hardware transceiver blocks of the OptoRx's FPGA chip. Data and transmitter clock are decoded from the signal. These hardware transceivers are configured using Quartus II Mega-Wizard Plug-In manager in such a way that data exit each block using an 8 bit wide bus and 80 MHz clock. In the first

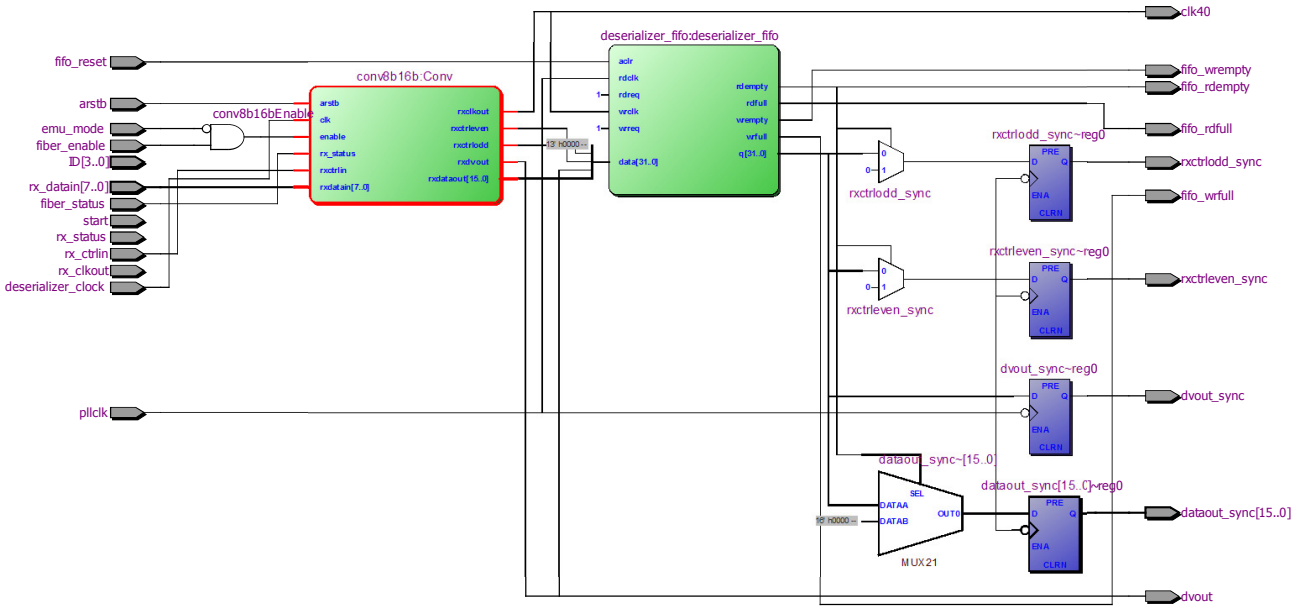


Figure 3.2: OptoRX channel processor block. This block converts 8 bit bus of the receiver to the original 16 bit bus. It is recovering high and low byte order. It also synchronizes two clock domains of de-serializer block and the rest of the trigger logic using FIFO.

step, data are realigned back to 16 bit wide bus by a channel processing block. Normally, the optical link is in the idle state which is detected and signalized by the receiver block. Thus the first and consecutive bytes of a received data frame are very well defined. A difficulty of the TOTEM trigger system is that optical links have to transmit trigger data continuously. For a proper operation, the transmitters are put in the idle state for a single clock cycle about every 100 ms (such operation is not standard). Thus a final state machine (FSM) is present and detects this idle state signal and then starts to toggle between two states to identify the high and low byte and data are copied to the 16 bit output bus accordingly to the FSM state. It also checks that the idle state signal arrives when the FSM is in the high byte state. If the

signal arrives when FSM is in the low byte state then it means a data skew and an error signal is generated and counted by the dedicated scaler. The FSM also generates the 40 MHz clock for the synchronization FIFO.

The receiver part of the FPGA uses clock decoded from the data stream and is synchronous with the detector side. The rest of the FPGA uses clock that is provided by TTCRx located on a TOTFed board. Despite the fact that the clock frequency is common for both parts, a clock phase between those two domains is unknown. For this reason a FIFO buffer is used to cross those two clock domains. In a case that either transmitter or receiver clock is not synchronous (for example a clock PLL is not locked), the FIFO starts to overflow or underflow. Thus the corresponding signals are also monitored.

To configure the signal receiving part, the "fiber enable" register FBREN needs to be written (Table 3.1). In the register, each bit corresponds to a single fiber and value '1' enables its output. To verify correct operation of each receiver, "fiber lock" register FBRSTAT can be checked. The bits are set to '1' if the block decoded clock from data stream and its PLL is locked to this frequency.

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	8	FBRSTAT	-				fiber status											
8	20	FBREN	-				fiber enable											

Table 3.1: "Fiber enable" and "fiber status" registers (base-address 0x00840000) are used to enable data outputs from individual receiver blocks and to check fiber statuses.

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	3C	RST	-													analog	digital	FIFO

Table 3.2: Reset register (base-address 0x00840200) is used to reset analog and digital part of the FPGA device. It is also to resets an internal synchronization FIFO blocks.

Once the detectors are powered-up, it is recommended to reset the deserializer modules by resetting the analog and digital parts of the firmware using the reset register RST (Table 3.2). During the detector power-up or during the receiver (analog) reset the buffer FIFO is filled with unknown number of bytes. The FIFO content has to be also reset using the same register. The digital reset also affects other blocks inside the firmware except the VME and register blocks thus the register content is unaffected.

Before the trigger bits enter the trigger blocks, it is needed to disable (mask) faulty and noisy ones. To do this a set of registers is used (see Table 3.3). Ease each register is used for one optical fiber and each bit in the register represents the corresponding trigger bit. The AND function is used between the registers and trigger bits, thus writing 0xFF to the register enables all the trigger bits from a given fiber (writing 0x00 disables all the trigger bits).

reg.	address	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	8	MASKA (fiber 1)	fiber 1 high Byte								fiber 1 low Byte							
3	C	MASKB (fiber 2)	fiber 2 high Byte								fiber 2 low Byte							
4	10	MASKC (fiber 3)	fiber 3 high Byte								fiber 3 low Byte							
5	14	MASKD (fiber 4)	fiber 4 high Byte								fiber 4 low Byte							
6	18	MASKE (fiber 5)	fiber 5 high Byte								fiber 5 low Byte							
7	1C	MASKF (fiber 6)	fiber 6 high Byte								fiber 6 low Byte							
8	20	MASKG (fiber 7)	fiber 7 high Byte								fiber 7 low Byte							
9	24	MASKH (fiber 8)	fiber 8 high Byte								fiber 8 low Byte							
10	28	MASKI (fiber 9)	fiber 9 high Byte								fiber 9 low Byte							
11	2C	MASKJ (fiber 10)	fiber 10 high Byte								fiber 10 low Byte							
12	30	MASKK (fiber 11)	fiber 11 high Byte								fiber 11 low Byte							
13	34	MASKL (fiber 12)	fiber 12 high Byte								fiber 12 low Byte							

Table 3.3: Registers for enabling of individual trigger bits (base-address 0x00840200). Each fiber represents a 16 bit wide bus. Each bit can be enabled by writing '1' to the corresponding bit.

3.1.2 Trigger logic blocks

T2 and Roman Pot detectors use the same trigger firmware for the OptoRX receivers and for each detector type there is an independent trigger logic block inside the firmware. Output trigger bits from the individual blocks are multiplexed and the trigger control register TRGCNTRL bits 0 to 3 are used as the select vector (Table 3.4). Table 3.5 shows possible values that can be written to the register. Based on the selected trigger mode an output 12 bit wide trigger bus bits are assigned corresponding values (Table 3.6).

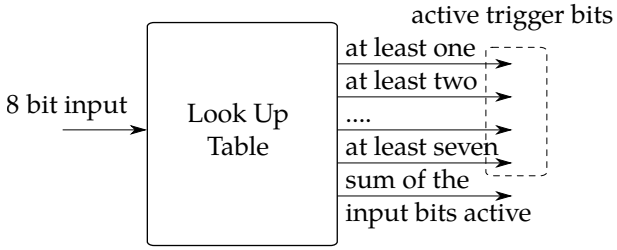


Figure 3.3: LUT is one of the main components of the OptoRx firmware. Its outputs are driven if at least one, two, .., 7 bits of the input vector are active. It also makes a sum of all active bits.

The main component is LUT (Figure 3.3). Its 8 bit wide input is related to the geometry of T2, namely it's 8 bits per wedge, and it generates two sets of outputs: 7 bit wide vector where bits are active if at least one, two, .., seven input bits are active and a sum of active bits in the input vector. Despite the fact that those LUT have been implemented for T2 they are also used for RP. Since an individual projection contains 16 active strips, only 2 LUT are needed to pre-compute sum of all active bits. Consecutively, a sum block is used. The "at least one bit active" signal is used for the RP trigger logic blocks.

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
34	88	TRGCNTRL													Mode select			

Table 3.4: Trigger control register (base-address 0x00840200) is used to select trigger logic scheme accordingly to the used detector type. The option list is shown in Table 3.5.

value	detector type	mode
0	T2	Telescope 2 minimum bias + high multiplicity
1	RP	Roman Pots minimum bias
2	RP U or V	OR function between U,V planes
3	RP U and V	AND function between U,V planes
4	RP U(1) and V(1)	only 1 sector active in each plane
5	RP HM U or V	high multiplicity cut + OR function between U,V planes
6	RP HM U and V	high multiplicity cut + AND function between U,V planes
7-15	—	reserved

Table 3.5: Possible setting values for the trigger control register (base-address 0x00840200).

bit	T2 minimum bias	RP minimum bias(not tested)	RP mode 2-6
0	minimum bias	RP BT FR U min. bias	BT FR U/V
1	HM bit	RP BT FR V min. bias	HR FR U/V
2	HM wedges	RP BT NR U min. bias	TP FR U/V
3	at least 6 tracks	RP BT NR V min. bias	BT NR U/V
4	0	RP HR FR U min. bias	HR NR U/V
5	0	RP HR FR V min. bias	TP NR U/V
6	0	RP HR NR U min. bias	0
7	0	RP HR NR V min. bias	0
8	0	RP TP FR U min. bias	0
9	0	RP TP FR V min. bias	0
10	0	RP TP NR U min. bias	0
11	0	RP TP NR V min. bias	0

Table 3.6: OptoRX Output trigger bus – bit description for individual modes.

T2 trigger logic

Originally, the T2 trigger firmware contained only a minimum bias trigger logic. Later on, the high multiplicity cut logic was implemented, too. Based on the T2 geometry, two blocks were implemented: The HM cut for individual wedges and for entire quarters. Those trigger bits

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	0C	BITCNT	-						minimum number of all active bits									
24	10	BITVETO	-						maximum number of all active bits									
25	14	WEDGECNT	-						minimum number of active bits in wedges									
26	18	WEDGEVETO	-						maximum number of active bits in wedges									

Table 3.7: Registers controlling the limits for the high multiplicity cuts for T2 (base address 0x00840200).

are propagated individually to LONEG (Table 3.6). The limits for the HM cuts can be set by

writing to registers listed in Table 3.7.

When the sum of the corresponding bits reaches the programmed minimum, then the output trigger bit is generated. When it reaches the maximum value, a veto signal is generated. Despite a fact that the veto function is implemented in the trigger logic block, it has never been used.

Roman Pot trigger logic

The Roman Pot trigger functionality was extended (several times) during its operation. It was convenient to add blocks, instead to rewrite the already existing code already tested and commissioned. As listed in Table 3.5, there is a minimum bias trigger block which generates trigger bit if any trigger bit in RP is active. The functionality of the RP U or V block is basically the same, except its implementation. Also the meaning of the output trigger bit is different (see Table 3.6). The RP U and V generates the corresponding trigger bit only when at least one bit is active in each projection u and v. The next mode U(1) and V(1) gives 1 at the output when there is exactly one bit active in each projection. The last two modes implement

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
35	8C	RPHMLESS	NR HR				NR VT				FR HR				FR VT			
36	90	RPHMMORE	NR HR				NR VT				FR HR				FR VT			

Table 3.8: Registers controlling the limits for the high multiplicity cuts for the Roman Pots(base address 0x00840200).

HM cuts. The number of active bits in each projection is calculated and the trigger bit is generated according to the programmed values. Those modes differs in consecutive OR/AND function applied between the planes. The limits for the HM cut can be set by writing to the registers RPHMLESS and RPHMMORE (Table 3.8).

3.1.3 Scalers

The scalers are used to monitor rates of incoming signals from detectors and also the internal signals in FPGA for set-up, calibration and monitoring purposes. These devices contain counters and use a pre-defined time interval (a time-window or a time-base) to periodically sample and reset the counter values. The time-window can be defined by another internal dedicated counter or by external signals. In the TOTEM trigger system a lot of scalers monitoring trigger bits and system state signals was implemented. To reduce resource requirements, one programmable time-base block is used. A simplified diagram of the scaler is shown in Figure 3.4.

In this firmware, the time-base module receives the LHC clock and it internal counter counts the number of clock cycles and this value is compared to a reference value. Once the counted value meets a desired condition, counter-reset and sample-hold strobes are generated and distributed to all scalers, their values are stored and counters are reset.

It is convenient to know the rates in Hertz and, therefor a one second integrating interval is primarily used. However, sometimes it is useful to be able to set longer or shorter integrating time. Thus a programmable time-base with 10 ms, 100ms, 1 s and 10 s options was implemented (mainly 16 bit counters are implemented inside the firmware to save logic elements and such a counter can easily overflow).

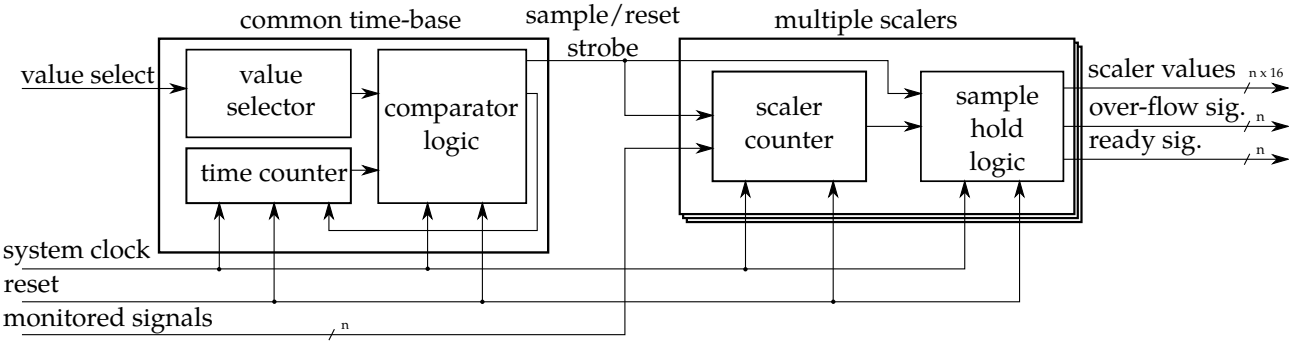


Figure 3.4: Time-base and scalers block diagram.

Trigger bit output scalers

Trigger bits generated by the trigger logic blocks are transmitted to the LONEG over 12 bit wide buses and each bit is monitored by a corresponding scaler, see Table 3.9. Each scaler meaning is defined by the selected trigger logic scheme described in the previous subsection.

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5	0x14	SCTRGOUTB0	output trigger bus - bit 0															
6	0x18	SCTRGOUTB1	output trigger bus - bit 1															
7	0x1C	SCTRGOUTB2	output trigger bus - bit 2															
8	0x20	SCTRGOUTB3	output trigger bus - bit 3															
9	0x24	SCTRGOUTB4	output trigger bus - bit 4															
10	0x28	SCTRGOUTB5	output trigger bus - bit 5															
11	0x2C	SCTRGOUTB6	output trigger bus - bit 6															
12	0x30	SCTRGOUTB7	output trigger bus - bit 7															
13	0x34	SCTRGOUTB8	output trigger bus - bit 8															
14	0x38	SCTRGOUTB9	output trigger bus - bit 8															
15	0x3C	SCTRGOUTB10	output trigger bus - bit 10															
16	0x40	SCTRGOUTB11	output trigger bus - bit 11															
17	0x44	SCTRGOUTRDY	-				scaler trigger out ready											
18	0x44	SCTRGOUTOVF	-				scaler trigger out overflow											

Table 3.9: OptoRX output trigger rate scalers registers (base address 0x00840200).

T2 scalers

At the beginning, T2 detector contained a lot of noisy channels when default thresholds were applied to VFATs. This is quite common for gas detectors compared to silicon detectors. For each channel individual threshold had to be obtained and set, therefor for a faster identification of noisy channel, four scalers were implemented for each wedge. Those scalers can be read indirectly by writing the corresponding address (Table 3.12 also describes mapping of the T2 wedges in the OptoRX receivers) to the register SCA (Table 3.10 also describes control registers for a reset and time-base settings). The scaler value can then be read from the SCV register, see Table 3.11. This table also describes the over-flow and ready registers. In the past those four scalers were assigned to the output of LUT "at least 1,2,4 and 6". All scalers displayed as a table, were very useful to identify noisy channels in wedges. Later on, the HM cut outputs were more important and the middle two scalers were reassigned.

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	0x7C	SCA	-									scaler address						
32	0x80	SCTB	-														time-bases	
33	0x84	SCRST	-															reset

Table 3.10: T2 scaler block control registers (base-address 0x00840200).

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0x00	SCV	scaler value															
1	0x04	SCRDYA					scalers ready A											
2	0x08	SCRDYB					scalers ready B											
3	0x0C	SCOVFA					scalers overflow A											
4	0x10	SCOVFB					scalers overflow B											

Table 3.11: Scaler block read only registers (base address 0x00840100).

fiber	wedge	wedge	mask reg.	address	scaler select address				scaler select address			
0	10	8	2	208	7	6	5	4	3	2	1	0
1	6	4	3	20C	15	14	13	12	11	10	9	8
2	2	0	4	210	23	22	21	20	19	18	17	16
3	1	3	5	214	31	30	29	28	27	26	25	24
4	5	7	6	218	39	38	37	36	35	34	33	32
5	9	11	7	21C	47	46	45	44	43	42	41	40
6	-	-	8	220	55	54	53	52	51	52	49	48
7	-	-	9	224	63	62	61	60	59	58	57	56
8	-	12	10	228	71	70	69	68	67	66	65	64
9	-	-	11	22C	79	78	77	76	75	74	73	72
10	-	-	12	230	87	86	85	84	83	82	81	80
11	-	-	13	234	95	94	93	92	91	90	89	88

Table 3.12: Individual wedge scalers of Telescope 2 - indirect addressing. The table shows indirect addresses of the individual wedges and the corresponding masking address.

Roman Pots u/v projection scalers

In addition to the output trigger bits, scalers monitoring individual projection planes of the Roman Pots are implemented. The related register addresses are in Table 3.13. Those scalers

reg.	address	name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
33	84	SCALER_RP_FR_BT_U	scaler value															
34	88	SCALER_RP_FR_BT_V	scaler value															
35	8C	SCALER_RP_FR_HR_U	scaler value															
36	90	SCALER_RP_FR_HR_V	scaler value															
37	94	SCALER_RP_FR_TP_U	scaler value															
38	98	SCALER_RP_FR_TP_V	scaler value															
39	9C	SCALER_RP_NR_BT_U	scaler value															
40	A0	SCALER_RP_NR_BT_V	scaler value															
41	A4	SCALER_RP_NR_HR_U	scaler value															
42	A8	SCALER_RP_NR_HR_V	scaler value															
43	AC	SCALER_RP_NR_TP_U	scaler value															
44	B0	SCALER_RP_NR_TP_V	scaler value															
45	B4	UV_RDY	-		v scalers ready						-		u scalers ready					
46	B8	UV_OVF	-		v scalers overflow						-		u scalers overflow					

Table 3.13: Mask registers for individual trigger bits. Each bit from each fiber can be masked individually (twelve fibers represents one hundred ninety two bits in total, base address 0x00840100).

are important for timing of the RP trigger bits. If the trigger bits of individual projections are off time, then a coincidence rate between them drops.

3.2 Electrical trigger - hardware

The triggering information about particles detected by the Roman Pots at 220 meters is transmitted over an electrical line. This part is called "electrical trigger". The electrical trigger is used due to a lower propagation delay inside the used metallic wires compared to the optical fiber (4.2 ns per meter in the metallic wire; 5.0 ns per meter in the optical fiber). The hardware part of the electrical trigger uses the LVDS standard and the overall length of each transmission line is about 270 m in total and it is divided to segments about 70 m long. Signal repeating devices (repeaters, Sub-section 3.2.4) are placed between every two segments to reshape and amplify individual trigger signals.

Data have to be send over lines with a minimum latency, thus the repeaters are designed as simple buffering devices without any sophisticated signal reconstruction and also without synchronous logic stages. Such a solution has a lot of advantages and some disadvantages. The most important advantage is its small signal propagation delay in the device. The measured propagation delay is less than 2 ns for a single repeater. If there were synchronous logic stages on the device, then the delay of such a device would be at least one clock cycle (25 ns at 40 MHz clock). As there are five repeaters in the line, this would lead an overall delay of at least five clock cycles (125 ns). Such a delay is already about 10% of the propagation delay of the installed cables. Unfortunately, an asynchronous solution does not provide a consistent propagation delay for all parallel bits leading to a non negligible signal skew on each line. Moreover the repeater does not reconstruct the length of the original pulse. The difficulty is

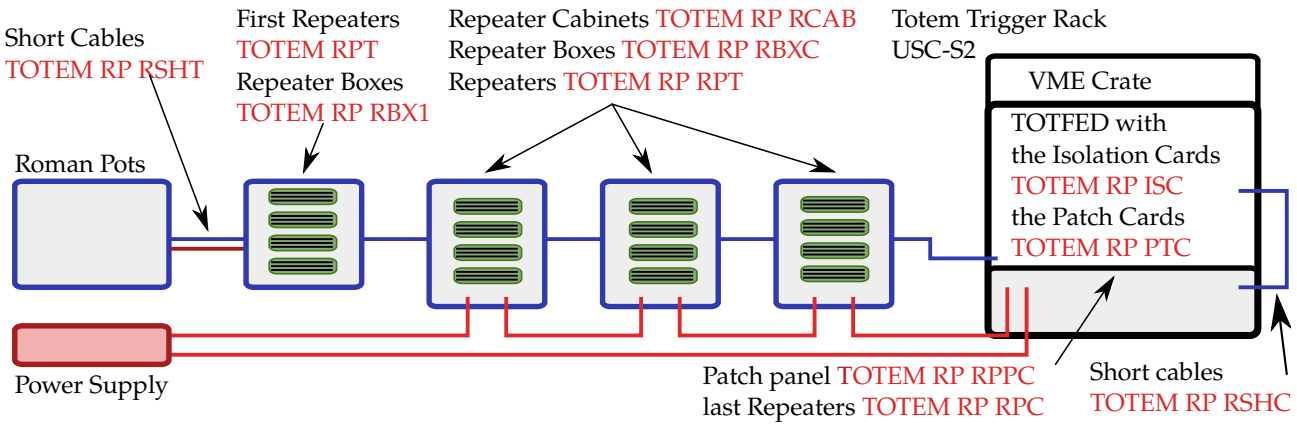


Figure 3.5: Electrical trigger chain. This block diagram shows the trigger signal path from the Roman Pot detectors to the counting room. The signal is amplified and reshaped by the repeaters. Galvanic isolation between the electronics in the counting room and the rest of the chain is provided by the isolation cards in the VME crate.

that the trigger signals from the Roman Pot mother board are not modulated at all. Data are being sent as raw pulses. This means that one signal state is dominant and creates a DC bias. This leads to a wide frequency bandwidth of the signal and that complicates the data transmission. This has to be compensated according to the parameters of the cables. The problematic is described in more detail in Sub-section 3.2.4.

The complete chain of the electrical trigger is shown in Figure 3.5. There is the Roman Pot as the source of the signal. There is a Maraton power supply as a power source. The trigger signal outputs of the Roman Pot are connected to the first repeater (TOTEM RP RPT) by

thin short cables (TOTEM RP RSHT) about 2.5 m long (Each Roman Pot uses two cables with 32 LVDS pairs in total). The first repeater is powered by the Roman Pot and is mechanically encapsulated in a protective box (TOTEM RP RBX1) which is fixed to the mechanical structure of the Roman Pots. The output of the first repeater is connected to a thick and 70 m long industrial cable. This cable follows the LHC tunnel towards the IP5 and it leads to the first repeater cabinet (TOTEM RP RCAB). Further three similar segments follow and the cable ends in the patch panel (TOTEM RP RPPC) in the Totem's trigger rack at CMS USC-S2 where also the last repeater (TOTEM RP RPC) is located. This repeater reshapes the signal and sends it to the isolation card (TOTEM RP ISC, Sub-section 3.2.2) where the galvanic isolation of the Roman Pot (detector) side and the counting room side is provided. This card is interconnected with the TOTFed via the patch card (TOTEM RP PTC, Sub-section 3.2.3) and they make a compact block.

3.2.1 Hardware Overview

The autor has developed specific hardware to meet the requirements of the TOTEM experiment. It was crucial to achieve minimum delay of the system and maximum robustness from a mechanical, electrical and radiation point of view. To fulfill this, several electronic devices have been created, see Table 3.14.

Device	CERN EDA ID	CMS ID	Sec. 45	Sec. 56	USC	Total	Sub-sec.
repeater-box	01630-V2-0	TOTEM RP RPT	48	48	0	96	3.2.4
repeater-box-pp	02082-V1-0	TOTEM RP RPC	0	0	24	24	3.2.5
isolation board	01882-V1-0	TOTEM RP ISC	0	0	12	12	3.2.2
patch card	01883-V1-0	TOTEM RP PTC	0	0	3	3	3.2.3

Table 3.14: List and numbers of hardware devices installed for the electrical trigger.

The repeater device was originally designated to be installed in cabinets without any protective box and the original name of the device in the CERN EDA database is repeater-box. Later on a small repeater box has been added into the project. In order to avoid ambiguities the original device will be here after devoted as "repeater" and the physical box for the repeater as "repeater box".

3.2.2 Isolation board

The purpose of the isolation board (Figure 3.6 and 3.7) is to provide the galvanic isolation for the trigger signals arriving from the Roman Pots and entering the electronics inside the CMS service cavern (this reduces possible side effects created by ground loops between power supplies and protects the electronics located in the service cavern). The distance (over 270 m) means that each side has a different ground potential that might lead even to a damage of the electronics.

The isolation board uses LVDS to CMOS converters to convert the incoming. The CMOS signals enter the digital isolator chip (SI8440), which is capable to provide electrical isolation up to 5 kV. Both sides are powered from the UCS-S2 side. In order to provide power to the detector side, an isolated DCDC converter is used together with a low voltage drop power regulator. This combination provides a stable voltage source for the LVDS to CMOS converters

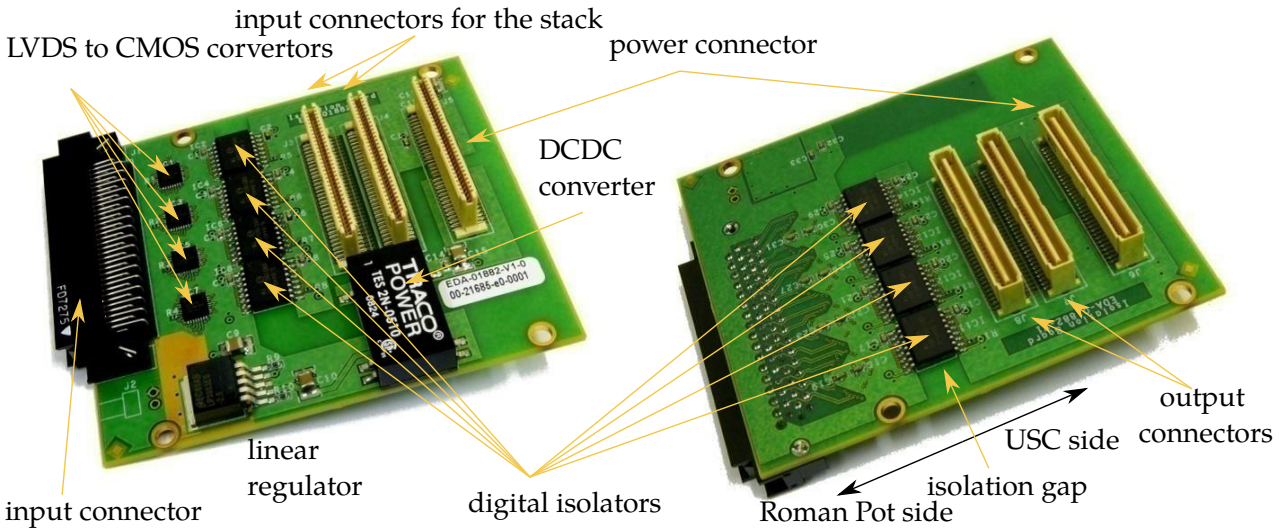
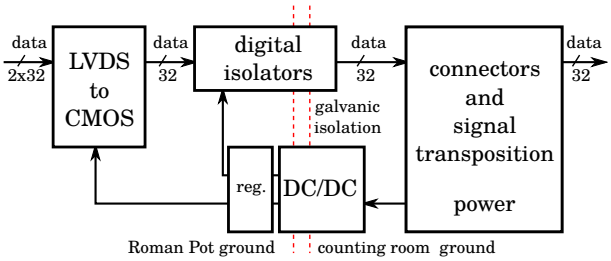
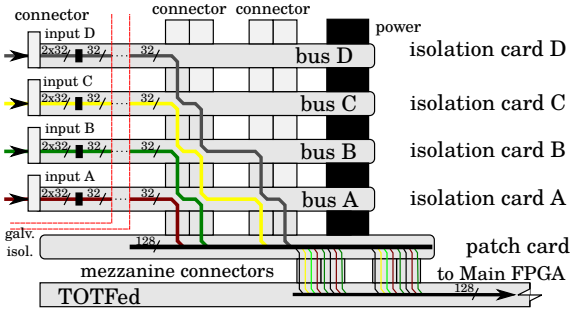


Figure 3.6: Isolation board provides galvanic isolation between the incoming LVDS lines of the electrical trigger and the rest of the electronics in the counting room. Each isolation card can isolate up-to 32 LVDS pairs.

and also for the digital isolators and improves the signal integrity. An input-part ground of the isolation board is connected to the Roman Pot ground potential. The rest of the board shares a local ground potential. A simplified block diagram of the card is shown in Figure 3.7.



(a) Block diagram of a single isolation board. Incoming LVDS signals are converted to CMOS. Then digital isolators are used to propagate these signals and provide galvanic isolation between the Roman Pot and USC grounds.

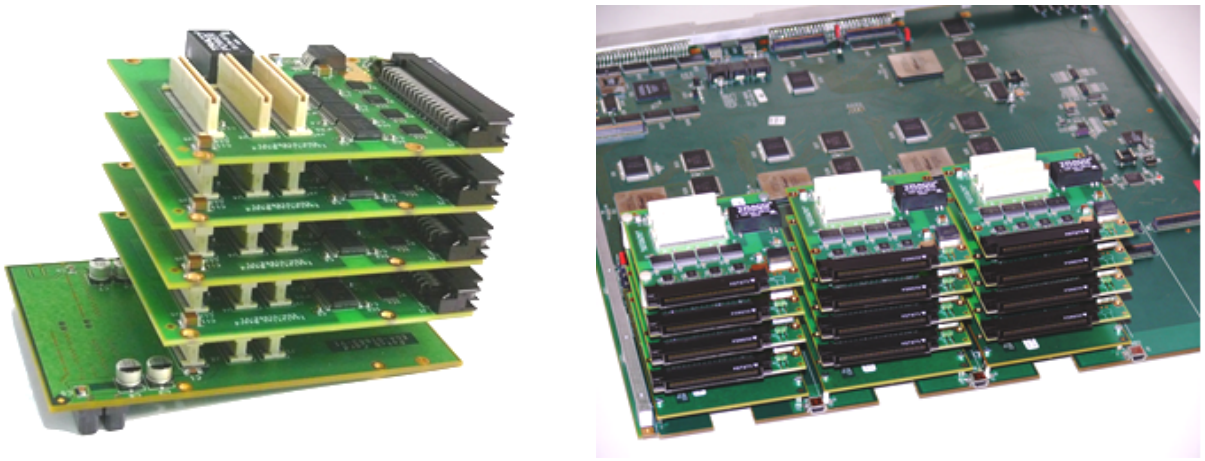


(b) Figure shows a way how the signals are propagated through the stack of the parch card and isolation boards. The patch card is used to provide a connection between the isolation boards and a TOTFed mezzanine slot.

Figure 3.7: Isolation board stack principle.

The isolation board is designed in such a way that a stack of up to 4 cards can be created providing a connection for up to 128 LVDS pairs. For the electrical trigger, 394 LVDS pairs had to be connected to the trigger crate. This was achieved with 3 stacks of isolation boards and one TOTFed card (Figure 3.8). To provide the necessary connection between the stack and the TOTFed, the patch card (see Sub-section 3.2.3) was produced. It looks as an unnecessary step, but the patch card simplified the design of the isolation board.

Figure 3.7 shows propagation of the signals through the stack of the isolation boards. It's made as a transposition of the signals between the connectors on each board. This transposition



(a) Single stack.

(b) Three stacks installed on the TOTFed.

Figure 3.8: Stack of the patch card and isolation boards called “Big Mac”.

limits the stack to maximum number of four boards.

Figure 3.8 shows the stack of the patch card and isolation boards (on the left) and the TOTFed with three stacks installed (on the right).

3.2.3 Patch card

This card is designed to provide interconnection between the TOTfed and up to 4 isolation boards. This card fits into mezzanine slots of the TOTFed board. The reason of having this card between the Isolation Card and TOTFed is to simplify the design of the isolation cards.

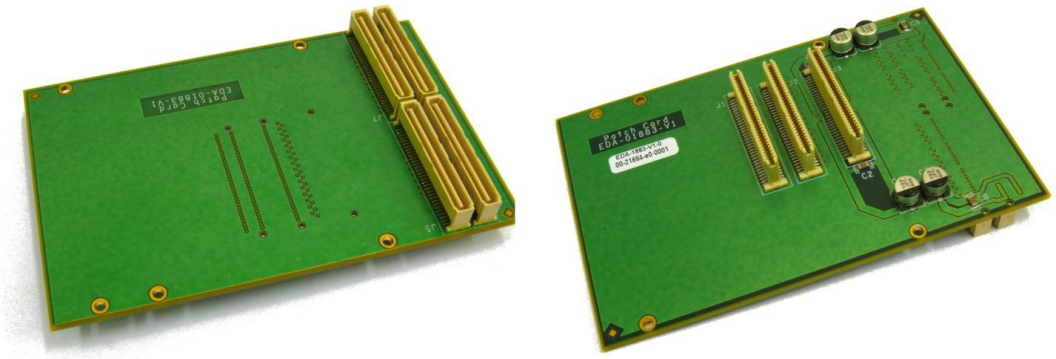


Figure 3.9: Patch Card

The card design is focused on signal integrity. All signal lines are tuned to impedance of 100 Ω and signal layers are separated by ground layers to eliminate cross talks.

3.2.4 Repeater

The trigger system uses repeaters (Figure 3.10) to reconstruct original signal shapes after passing long segment of a cable which behaves like a low pass filter and degrades wave-forms of the signals (especially by suppressing higher harmonics frequencies). Thus this cable attenuation has to be compensated. Figure 3.11 shows a repeater performance and a corresponding measurement of a signal that transmitted over a 270 m long line segmented each 70 m and equipped with the repeaters (signal is measured at the beginning and the end of the line). The pre-emphasis of the signal is used to compensate the cable attenuation, which is implemented by adding high pas filters to outputs of the repeater chip.

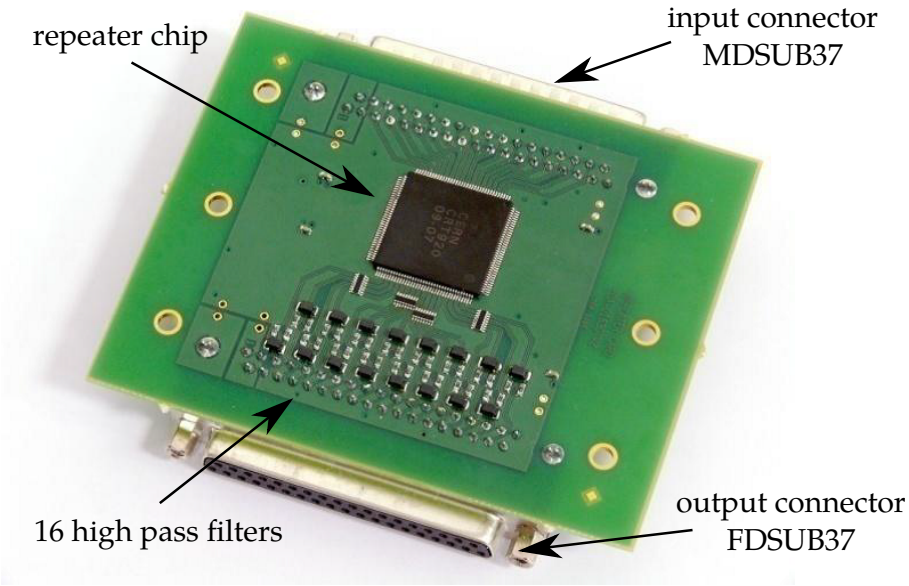


Figure 3.10: Electrical trigger repeater based on a 32-LVDS-line-wide buffer chip developed by the CERN Electronics Group. At the output of each LVDS pair, there is a high pass filter designed to compensate a cable attenuation.

Problematic of long distance transmission and repeater design

Every cable behaves like a low pass filter and its length is increasing the final attenuation. The resonance frequency of the cable usually is around 40 kHz. For higher frequencies, parasitic parameters and processes (e.g. a skin effect, a proximity effect, line capacity) take a place. In general, an increase of the cable length reduces the maximal modulation frequency of the signal. There are several possible approaches how to compensate those effects and reach higher data rates: a reduction of used frequency bandwidth by modulating the signal or a compensation of the cable attenuation by filters at the input or output of transmission lines.

Figure 3.12(a) and 3.13 shows a fatal consequence of signal attenuation for a differential bus. Without a compensation, the cross-over of a positive and negative peak is shortened in time and thus the length of the pulse is shortened by a consecutive buffer placed at the output of a cable.

In the worst case, the signal amplitude is so reduced that the positive and the negative signals do not cross over at all. Thus the signal is lost for good.

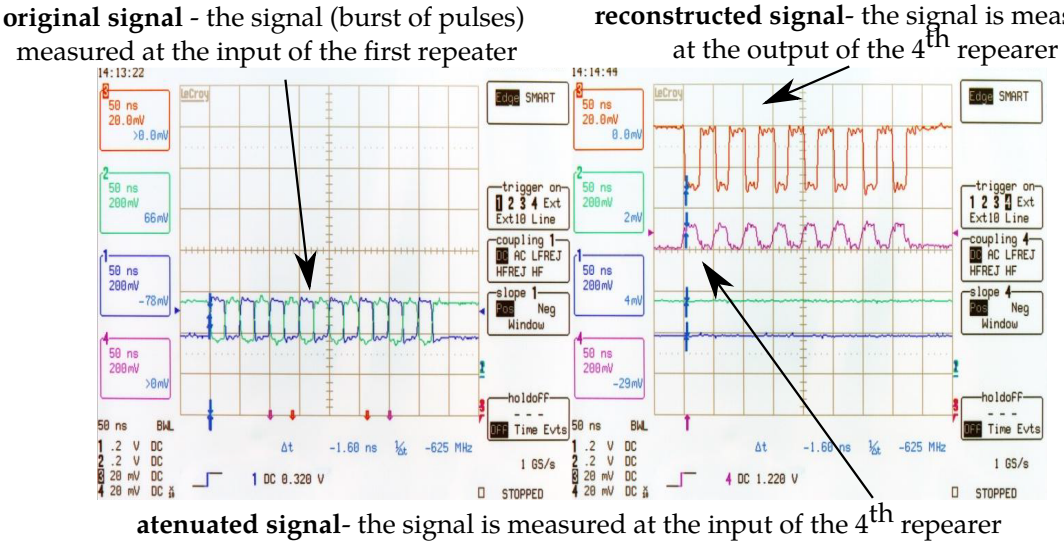
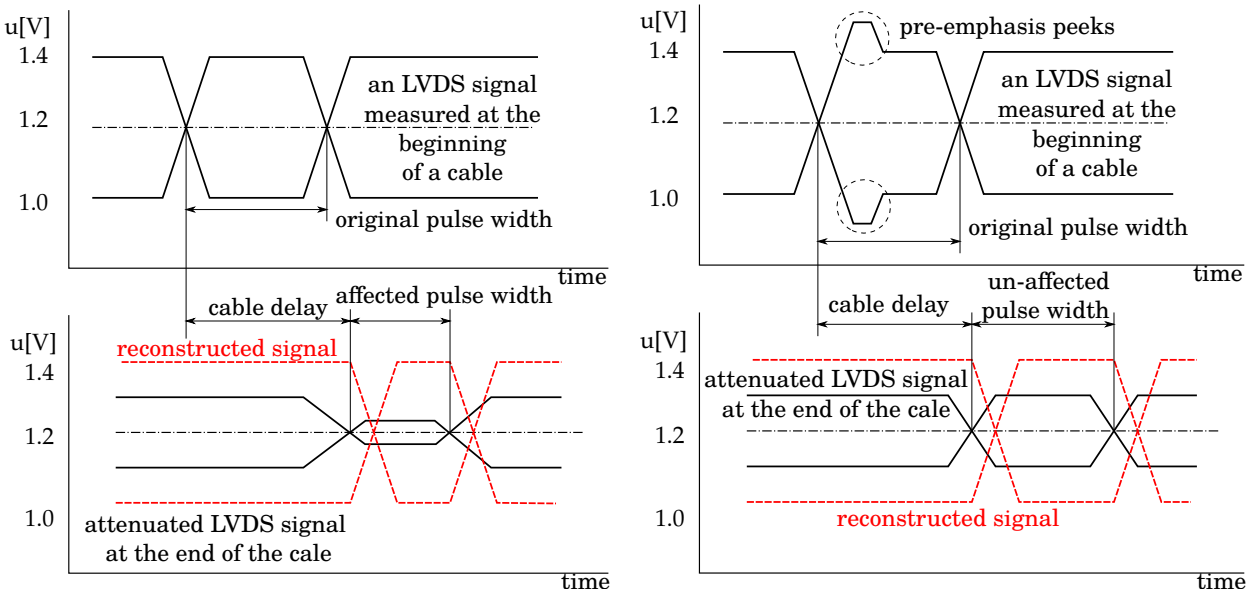


Figure 3.11: Performance of the repeaters. A burst of 25 ns wide pulses has been generated by a pulse generator and transmitted over four 70 m long segments of cable. The repeaters have been plugged at the beginning, between the segments and at the end of the line. The last repeater did not have a high pass filter assembled and the line was terminated. The output of the last repeater confirms a good performance of the repeaters for the electrical trigger (four channel oscilloscope without differential probes was used thus only single point measurement have been done for the last repeater).

Figure 3.13 shows a real measurements of series of burst of LVDS pulses measured at long cable. The dominating DC component and lower frequencies of the signal are slowly suppressed and the signal is improved after a certain number of pulses. This means that by periodical swapping of the line state, the frequency bandwidth of the signal was reduced and this reduced effects of the long cable signal attenuation. It means that in future, the TOTEM trigger bit data transmission can be improved using some kind of signal modulation for transmitted data. This is very important for a possible future upgrade. So far the output of the VFAT is without a modulation of any kind.

The author had to find another solution for the existing system. After several tests, he decided to use the pre-emphasis of the signal. It means to add the short burst of energy when the bus changes the state. The principle is shown in Figure 3.12(b). There are several design flaws inside the repeater chip. It is not possible to get more energy from the chip. The main issue is that the output stage of an internal buffer is implemented as a simple current source. The problem is visible in Figure 3.14. On the left, there is the measured transient of the signal without pre-emphasis. The time of the transient is about 1 μs. This is too far from the nominal values for our signal. In the first moment the internal capacitor for the common bias discharges and then the internal current source keep charging the cable capacity by 5 mA current. This behavior of the chip limited a number of possible solutions and the author had to use the passive output filter to reduce the amplitude of the signal. The author also tested several configurations of output filters. The best results were achieved with an RL filter. It is not very convenient to use an inductance in the LHC environment (due to the large number of sources of the electromagnetic field). Unfortunately, poor results were achieved with an RC filter. Most likely, it is due to a large non-linearity the repeater chip outputs. The behavior of



(a) Without compensation.

(b) With pre-emphasis compensation.

Figure 3.12: The long-cable attenuation affects the transmitted pulse. The image shows what happens without the proper compensation.

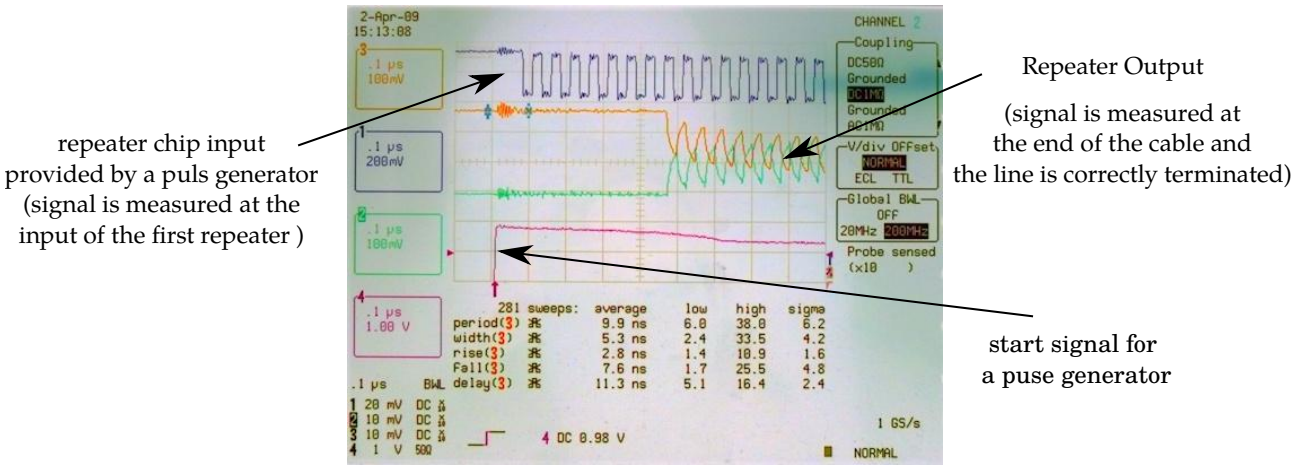


Figure 3.13: Measurements of the repeater signal integrity over the long cable. Only two repeater chips are used (at the beginning and at the end of the long cable). The signal is totally corrupted.

the repeater with the output filter) is on the left side of Figure 3.14.

For all the tests related to repeater chip design, test setup shown in Figure 3.15 and 3.16 was used. The pulse generator was used as a source of a signal. The signal went into the first channel of the repeater 1. The output of the repeater 1 was connected to the long cable. At the end of the cable there is the repeater 2. the output of the repeater 2 goes back to the repeater 1 but is shifted by one. Like this the author could test the 16x70 m long transmission line.

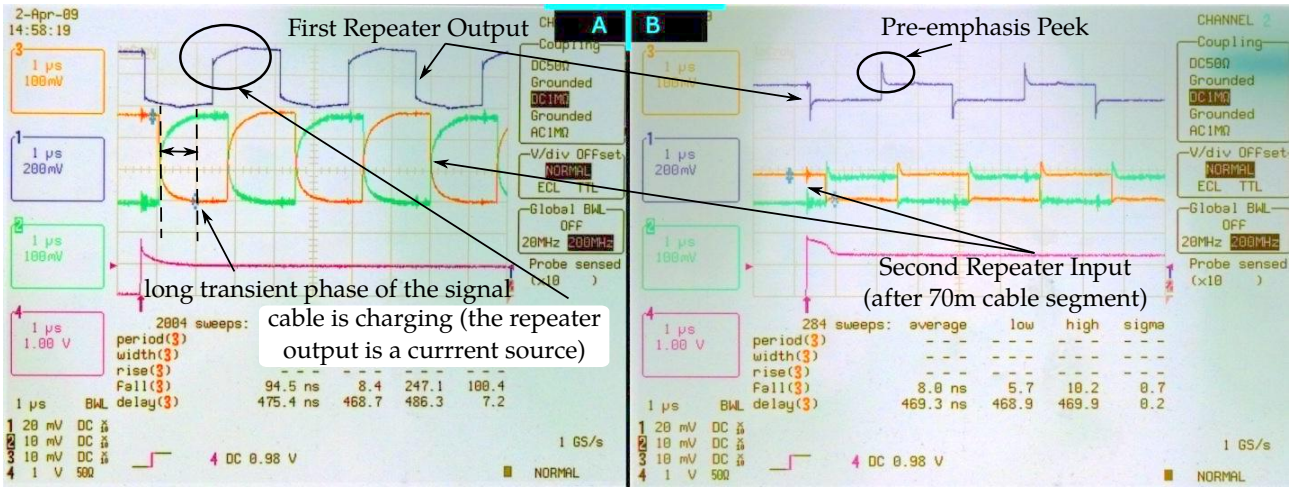


Figure 3.14: Transient of the signal at the end of the cable without (A) and with (B) pre-emphasis filter. In this case, the length of the pulse is almost 2 μs which helps to understand a pulse response.

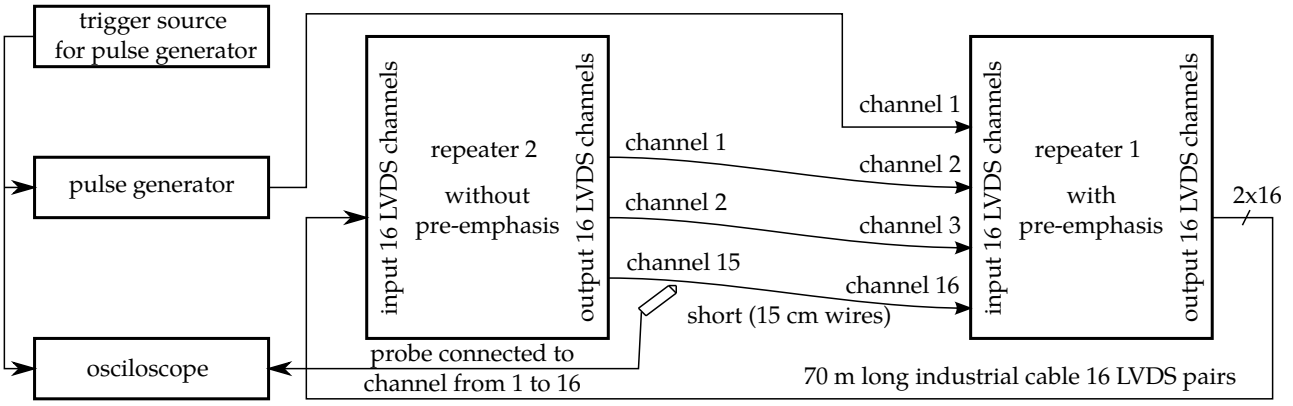
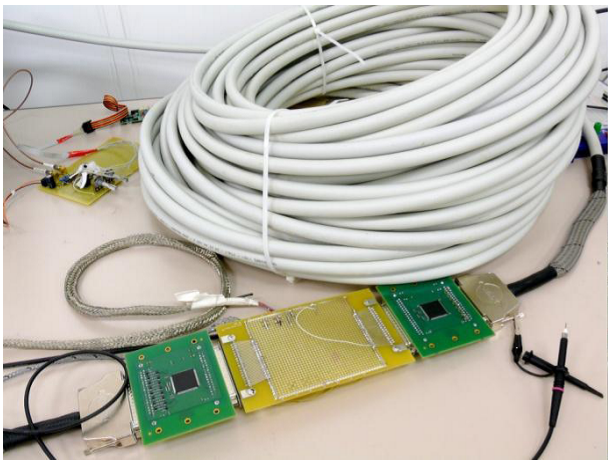


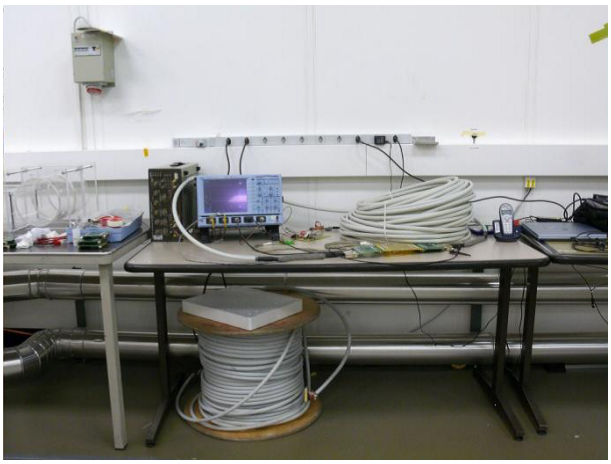
Figure 3.15: Block diagram of the laboratory test-setup for the repeaters. The trigger source periodically starts the generic pulse generator and a burst of 25 ns pulses are generated. The output of the generator is connected to the first channel of the repeater 2 and its output is connected to the 70 m long cable. At the end of the cable there is the repeater 1. Its first output line is connected to the second one of the repeater 2. Like that, 16 passes by the long cable can be measured.

3.2.5 Modified repeater for a patch panel

As all the electrical lines arrive the trigger rack, it is needed to convert thick the industrial cables to thinner ones in order to avoid mechanical stress to galvanic isolation cards and the rest of the electronics. Concerning the length of lines, an active element was placed between the two different cable types to avoid possible signal reflections. For this purpose, the original repeater card was modified and the output connector was changed from DSUB37 to a small micro ribbon (Figure 3.17). In contrast to the 70 m long segments, the cable length does not require the output filter and therefore the filter components are not mounted (however the board contains the pads if the filter is needed in future). In this case, the board is not powered by the DSUB37 connector but by the dedicated Molex connector.



(a) Two repeaters with transposition card for individual channels.



(b) Complete test setup.

Figure 3.16: Pictures of the test-setup for the electrical trigger in the laboratory.

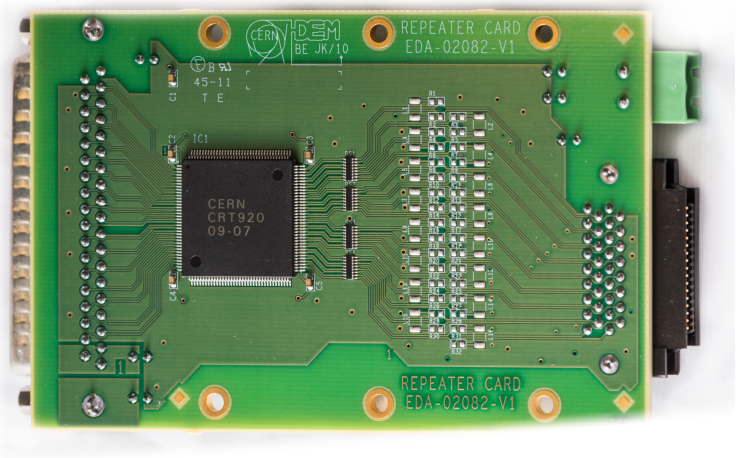
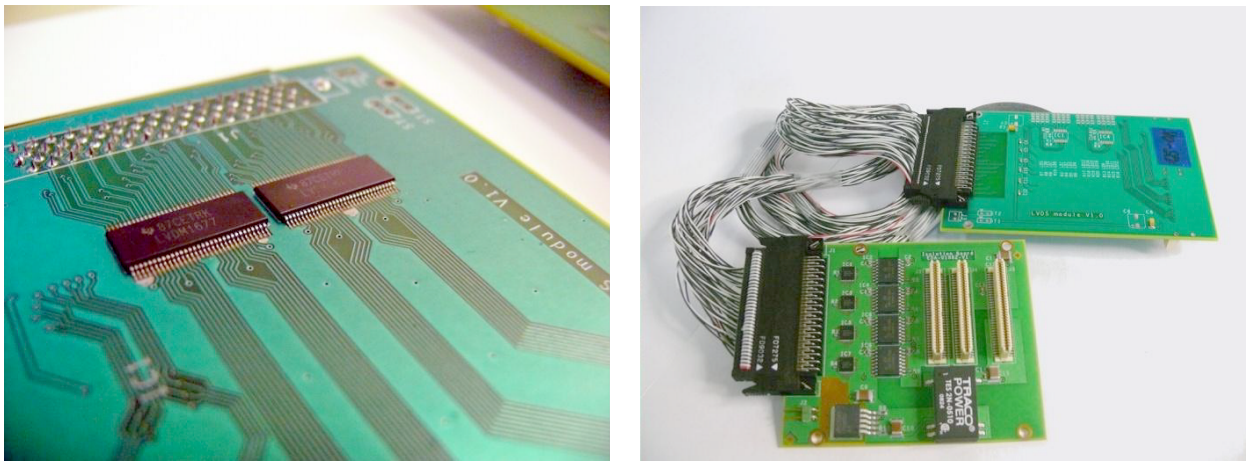


Figure 3.17: Modified repeater for a patch panel: The output 37 pin DSUB connector was replaced by a micro ribbon connector to provide adequate connectivity for the thin output cable.

3.2.6 Transceiver card

The transceiver card (Figure 3.18) has been created for testing purposes. It contains two LVDM transceivers (SNLVDM1677) with integrated termination resistors.

The LVDM chip is designed to provide sufficient current for 2 termination resistors (one on the chip and one on the end of the line which makes difference between LVDS and LVDM standards). The transceiver transmission lines are grouped by 4 and each group can be separately configured as an input or output. The card also holds 8 LED diodes for the indication of the direction and the same number of LED diodes for general purpose (debugging or signalization). This card has one advantage: thanks to 32 LVDS channels it can be used to test all 16 channels of repeaters thus only one FPGA on TOTFed is needed to send and receive testing signals. This simplifies the firmware for the testing as there is no need for synchronization and data



(a) Detail of a transceiver card. (b) A transceiver card together with an isolation card

Figure 3.18: The transceiver card was designed as a TOTFed mezzanine card to provide sufficient number of LVDS links for testing of electrical trigger components.

transmission between FPGAs.

3.2.7 Cabling

There is a large number of cables needed for the electrical trigger. A significant part of the optical trigger delay is created by serialization and de-serialization of a parallel bus data that are outgoing from Roman Pot mother boards. For the electrical trigger, the parallel data bus was used for a data transmission (this eliminates this part of delay). The list of used cables is in Table 3.15. Using parallel bus meant to replace tiny optical fibers by a bunch of 24 thick industrial cables. Each cable had to be segmented and repeating devices had to be added to reach the desired data rate. To reduce the mechanical stress load caused by heavy cables to electronics, thin short cables were used from Roman Pots at the first repeaters. The same applies to the receiving part of the transmission chain. A mechanical protection for the cables and the repeaters is also needed. Boxes and the patch panel for these purposes have been constructed in the CERN mechanical workshop.

cable	LHC ID reference	length [m]	Sector 45	Sector 56	Total
Short RP-1st Rep.	TOTEM RP RSHT	2.5	12	12	24
Short PP-TOTFED	TOTEM RP RSCH	2.7	6	6	12
Long RP-RP		70	48	48	96
Long Power Rep		70	4	4	8

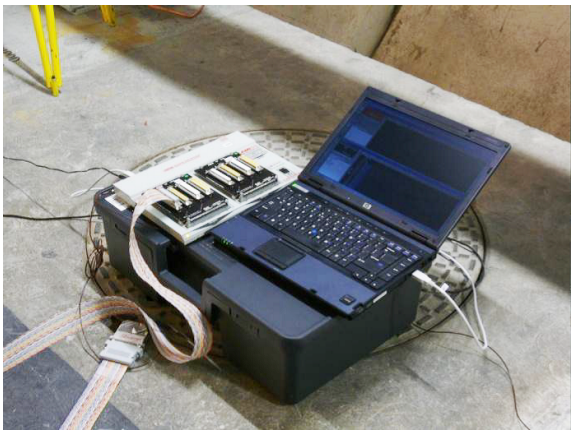
Table 3.15: List and numbers of pieces of the cables installed inside LHC for the electrical trigger.

- **Short cable TOTEM RP RSHT from the Roman Pot Motherboard to the 1st repeater.** This cable is used to provide a connection between the Roman Pot and the first repeater board. This cable is also used to power up the first repeater. The cable is

about 2.5 m long and it has a standard 40pin header connector on the Roman Pot side and a Dsub37F connector on the repeater side.

- **Long cable for LVDS.** The long cable is a pin to pin cable with the DSUB37 male at the beginning and DSUB37 female connector at the end. There is only one small modification: the female DSUB37 connector is also used to power-up repeaters using the pin 1, 2, 20 for the ground and 19, 37 for a power supply and these pins are provided with short cables that are connected to the power cable via a distribution frame.
- **Long power cable for the repeaters.** This heavy industrial cable is used to power the repeaters inside the LHC tunnel. The size is chosen for a minimum voltage drop over the distance. Such solution is used because it is dangerous to use linear regulators exposed to high radiation.
- **Short cable TOTEM RP RSCH from the last repeater to the isolation card.** This cable segment is the last and most complicated one. Its purpose is to combine 2 cables with 32 LVDS pairs in total into one thin cable.

Although a testing inside the LHC tunnel was in principal trivial, the inconvenient environment had to be taken into account. Therefore, the author prepared a test setup (Figure 3.19), allowing to place all equipment in to a comfortable position and thus reduce the testing time.



(a) Portable computer with a cable tester.

(b) Overall view at a test setup LHC.

Figure 3.19: Test setup for the electrical trigger cabling inside the LHC tunnel.

3.2.8 Mechanics

All the electronics for the electrical trigger is located in sites accessed by personnel thus mechanical protection had to be provided for all devices providing appropriate safeguarding for a personnel. The list of mechanical boxes for electrical trigger is in Table 3.16.

Repeater box

The repeater box is designed to contain three repeaters and provides them sufficient mechanical and electromagnetic protection. It is used as a standalone solution for the first repeaters in the transmission line. It is mounted to the mechanical structure of the Roman Pots.

box	Part Numbe	Sector 45	Sector 56	In total
repeater box	TOTEM RP RBXC	8	8	16
patch pannel box	TOTEM RP RPPC	0	0	2(UCS-2)
repeater cabinet	TOTEM RP RCAB	3	3	6
first repeater box	TOTEM RP RBX1	2	2	0

Table 3.16: List of the mechanical enclosures installed in the LHC machine to protect the electrical trigger electronics.

Figure 3.20: Mechanical box (repeater box) for the repeaters. Each box carries three repeaters. The box provides sufficient protection against the mechanical stress created by the cabling.

On the other hand, it does not provide sufficient protection to the connectors of the incoming cables. It means that additional protection is needed on exposed locations. For that reason the box is enclosed inside the repeater cabinet in the rest of repeater locations.

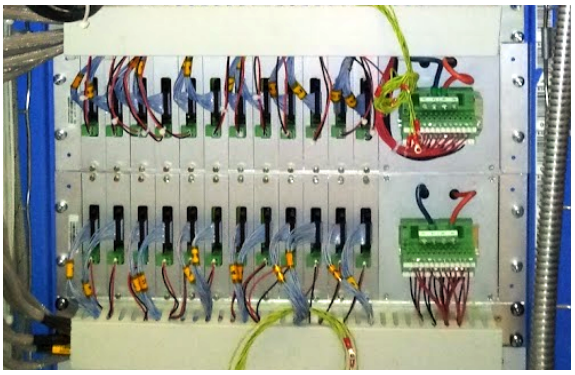
Patch panel

The patch panel is designed to provide mechanical support for the incoming (thick and robust) industrial cables, in order to protect the last repeater against the mechanical damage. Another function of the patch panel is to keep the power cables fixed in a proper position. These cables are incoming together with the signal cables and they provide the power for the last repeater and a solid ground for the isolation card.

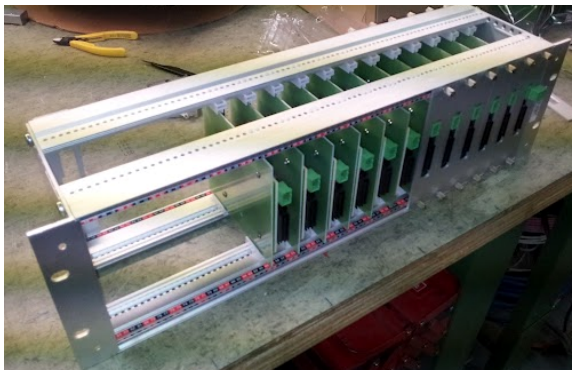
The last function of the patch panel is to hold the set of the last modified repeaters (Subsection 3.2.5) which were designed taking into account the limited space inside the rack and the different way of powering up of the repeaters.

Repeaters cabinet

These are solid industrial wall mounted boxes providing sufficient mechanical protection for the repeaters and cable connectors located in between of the long cable segments (i.e. every 70 m).



(a) Patch panel installation the trigger rack in the CMS service cavern.



(b) Picture taken during the patch panel assembly in the CERN workshop.

Figure 3.21: Patch panel is a rack mount box with a standard height of 3 u. Two pieces are mounted in the trigger rack in the CMS service cavern and hold twenty-four modified repeaters converting large-size industrial cables (not visible) into the thin cable (visible) suitable to be plugged into the electrical trigger TOTFed. Each repeater can be removed separately for a fast replacement.

3.3 Electrical trigger - firmware

The electrical trigger infrastructure was installed during the March 2012. The block diagram of the current firmware is in Figure 3.22. The most important part is the input signal sampling stage (Sub-section 3.3.1) and the Roman Pot trigger logic block (Sub-section 3.3.2) for a minimum bias and high multiplicity cut trigger. In the firmware, is also a VME interface block with

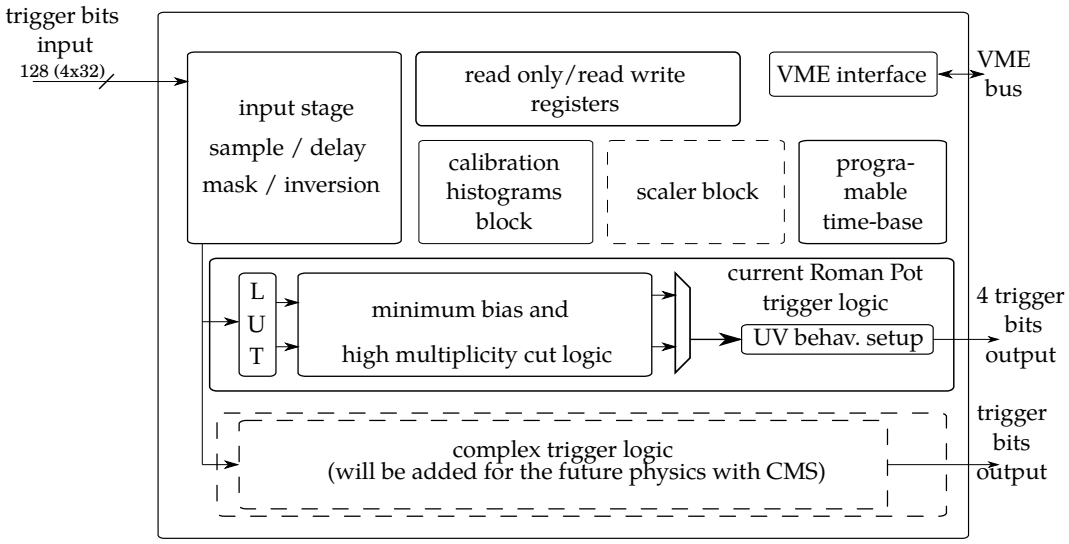


Figure 3.22: Block diagram of the electrical trigger firmware. The sampling input stage is responsible for sampling of incoming electrical trigger signals. Next blocks are the Roman Pot trigger logic responsible for a trigger signal processing, calibration histogram, and an VME interface with programmable registers. More complex logic and monitoring scalers have to be implemented.

read-only and read-write registers. Another important module is the calibrating histograms block, which allows to monitor the sampling of the individual trigger bits for calibration purposes. A scaler block for trigger system online monitoring has to be added in the future. In the moment the optical trigger scaler part is used for trigger rates monitoring.

The firmware is implemented inside the TOTFed's Main FPGA chips 1, 2 and 3. Each chip receives 128 bits (this corresponds to 4 Roman Pots). Thus one TOTFed is sufficient to receive the electrical trigger bits from all Roman Pots.

3.3.1 Input sampling logic

Each FPGA chip has to correctly sample 32 trigger signals from 4 Roman Pots (128 in total per FPGA) received through the electrical trigger line and "Big-Mac" stack of the isolation cards. Each Roman Pot bus represents 2x16 bits related to detector projections u (bit 15..0) and v (bit 31..16)). The buses are designated as follows in Table 3.17).

bus name	bits-v projection	bits-u projection	isolation card stack position
isolation_card_A	31..16	15..0	top
isolation_card_B	31..16	15..0	2^{nd} from the top
isolation_card_C	31..16	15..0	3^{rd} from the top
isolation_card_D	31..16	15..0	bottom

Table 3.17: Names of the trigger bits input buses used inside the electrical trigger firmware.

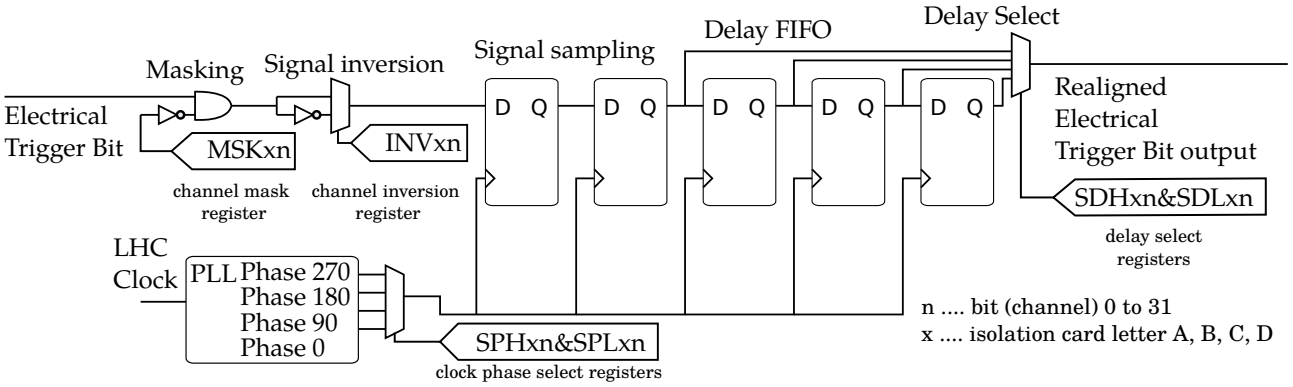


Figure 3.23: Input signal sampling stage of a single electrical trigger signal. The 25 ns wide pulses are incoming from the Roman Pot detectors and each line has an unknown phase and delay with respect to the system clock. For this reason each line sampling has to be programmed separately and each line has to be delayed accordingly to synchronize all channels.

Each line of each bus has a different propagation delay with an unknown phase. This means that the signal sampling is not a trivial task. Any possible signal skews and meta-stability have to be prevented. To do this, there is a dedicated programmable sampling stage for each channel. It's block diagram is shown in Figure 3.23 and the corresponding configuration registers are listed in Table 3.18. The author used the fact, that he had 32 bit wide registers and buses as well. The configuration bits for individual sampling stages are grouped in columns. It means that the bit 0 corresponds to channel 0.

reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	1C	SPHA	set phase high A																															
8	20	SPLA	set phase low, isolation card A																															
9	24	SDHA	set delay high, isolation card A																															
10	028	SDLA	set delay low, isolation card A																															
11	2C	INVA	inverse channel, isolation card A																															
12	30	MSKA	mask channel, isolation card A																															
13	34	SPHB	set phase high, isolation card B																															
14	38	SPLB	set phase low, isolation card B																															
15	3C	SDHB	set delay high, isolation card B																															
16	40	SDLB	set delay low, isolation card B																															
17	44	INVB	inverse channel, isolation card B																															
18	48	MSKB	mask channel, isolation card B																															
19	4C	SPHC	set phase high, isolation card C																															
20	50	SPLC	set phase low, isolation card C																															
21	54	SDHC	set delay high, isolation card C																															
22	58	SDLA	set delay low, isolation card C																															
23	5C	INVC	inverse channel, isolation card C																															
24	60	MSKC	mask channel, isolation card C																															
25	64	SPHD	set phase high, isolation card D																															
26	68	SPLD	set phase low, isolation card D																															
27	6C	SDHD	set delay high, isolation card D																															
28	70	SDLD	set delay low, isolation card D																															
29	74	INVD	inverse channel, isolation card D																															
30	78	MSKD	mask channel, isolation card D																															

Table 3.18: Sampling stage read-write registers, base-address 0x00840000.

Sampling phase setup registers SPHA(B, C, D) and SPLA(B, C, D)

These registers are dedicated to set the phase of the sampling stage with respect to the system clock. Possible values for individual bits are in Table 3.19. This stage allows us to setup correct sampling moment to avoid incorrect sampling due to the signal jitter. As an example, to set

SPHx bit n	SPLx bit n	phase [deg.]
0	0	0
0	1	90
1	0	180
1	1	270

Table 3.19: Sampling stage phase configuration.

the sampling phase to 90 degrees for the channel 10 at the isolation card A, write 0 to bit 10 in the register SPHA and 1 to a bit 10 in the register SPLA.

Signal delay setup - Registers SDHA(B, C, D) and SDLA(B, C, D)

These two registers are used to program a signal delay on the clock cycle level. The possible values are listed in Table 3.20. This programmable delay is essential for the signal alignment.

SDHx bit n	SDLx bit n	delay (num. of clock cycles)
0	0	0
0	1	1
1	0	2
1	1	3

Table 3.20: Sampling stage delay configuration.

For example, to delay channel 10 from isolation card B by two clock cycles, write 1 to bit 10 in the register SDHB and 0 to bit 10 in the register SDLB.

Signal inversion setup register INVA(B, C, D)

In total there are 384 LVDS pairs for the electrical trigger installed in LHC. For the case that

INVx bit n	function
0	input signal n is NOT inverted
1	input signal n is inverted

Table 3.21: Sampling stage signal inversion configuration.

an LVDS pair is swapped in the cabling by an accident, the signal inversion option is made inside the firmware. For example, to invert channel 15 at isolation card C, write 1 to bit 15 in the register INVC.

Signal masking setup register MSKA(B, C, D)

Any noisy channel on the trigger bus (e.g. a silicon detector is damaged or transmission line is broken) has to be masked to reduce its impact on the trigger system. Each channel can be

MSKx bit n	function
0	input signal n is NOT masked
1	input signal n is masked

Table 3.22: Sampling stage - signal mask configuration.

disabled separately by writing 1 to the corresponding masking bit in the masking register. For example to disable channel 1 at isolation card D, write 1 to bit 1 in the register MSKD.

3.3.2 Trigger Logic

The implemented trigger logic is related to the Roman Pot geometry. The two orthogonal projections u and v are represented by 16 bits per each projection. In the first step a number of active trigger bits in each projection is calculated. For this purpose two 8 bit LUT are used

for bits 15-8 and 7-0. A block diagram is shown in Figure 3.24. The LUT results are summed with an adder. Then the adder output is compared to limit values according to the following condition:

$$\text{value min} \leq \text{computed sum} \leq \text{value max}. \tag{3.1}$$

If the condition is fulfilled a corresponding output trigger signal is generated. In the same moment, also a veto signal is generated. This signal is conceived for a possible future usage in the final trigger logic and is based on following condition:

$$\text{computed sum} > \text{value max}, \tag{3.2}$$

where value max is common for the trigger and veto bits.

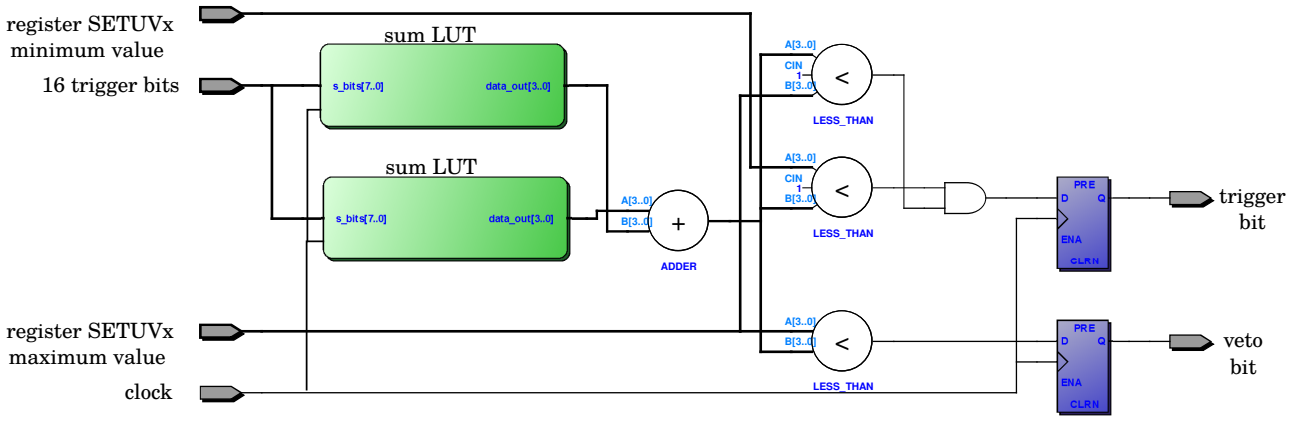


Figure 3.24: Roman Pot single projection plane logic - for each projection in each Roman Pot, the total number of the active trigger bits is calculated and compared to programmed minimal and maximal value set in registers SETUVA(B, C, D). Accordingly the trigger and veto signals are generated.

Once the projections u and v are analyzed separately, a coincidence of the results is made. It is possible to chose between AND and OR function for the trigger and veto bits (Figure 3.25). This setting has an enormous impact to the trigger efficiency and purity. The u, v coincidence can be set separately for each Roman Pot and for the trigger and veto signals.

reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	10	UVBHV													D	C	B	A													D	C	B	A
50	C8	SETUVA	unassigned																maxV			maxU			maxU				minU					
51	CC	SETUVB	unassigned																maxV			maxU			maxU				minU					
52	D0	SETUVC	unassigned																maxV			maxU			maxU				minU					
53	D4	SETUVD	unassigned																maxV			maxU			maxU				minU					

Table 3.23: Trigger logic behavior setup registers (base-address 0x00840000). Those registers allow to configure the u/v planes trigger logic behavior (Table 3.25) and set minim and maximum values (Table 3.24) for the trigger conditions.

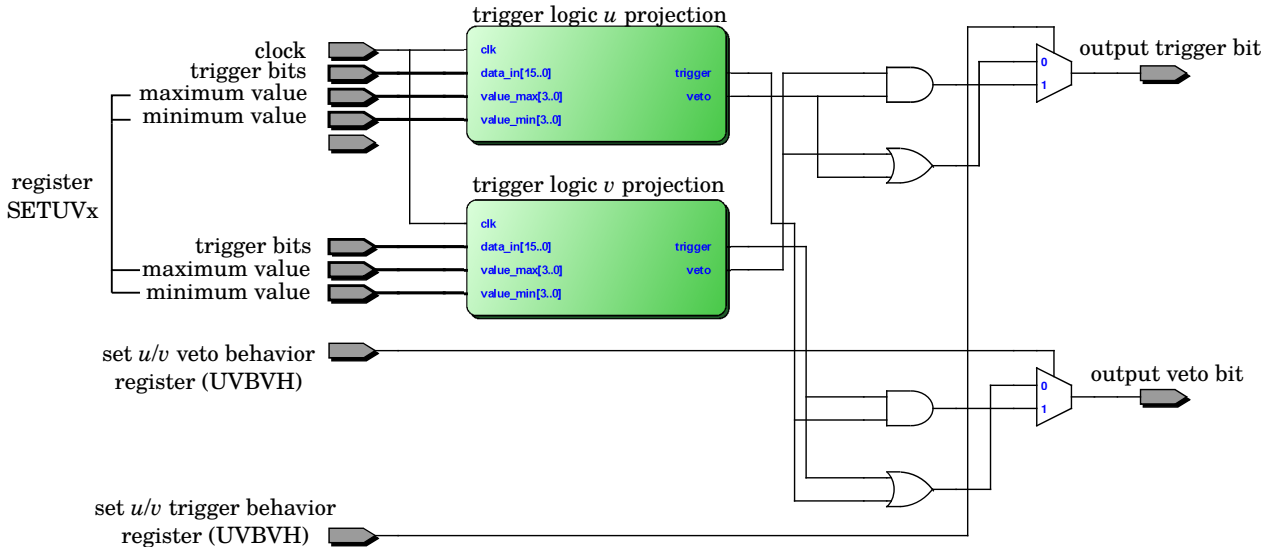


Figure 3.25: Roman Pot u, v trigger logic block diagram. The AND or OR function can be set for the u and v projection trigger processing.

Single plane setup registers SETUVA(B, C, D)

To set the minimum and maximum value for the individual u and v projection plane trigger logic, the registers SETUVA, SETUVB, SETUVC, SETUVD are used (Table 3.23). The meaning of the bits is explained in Table 3.24.

bits	meaning
31..16	unassigned
15..12	v projection - maximum value
11..8	u projection - maximum value
7..5	v projection - minimum value
4..0	u projection - minimum value

Table 3.24: Bit description for the trigger logic setup register SETUVA(B, C, D).

The minimum and maximum values for an individual projection trigger logic are represented by 4 bits. It means that values from 0 to 15 can be programmed. For example if the minimum bias trigger is requested (any bit is active), the value 0xFF11 should be written to these registers.

Coincidence of u, v projection planes behavior setup register UVBHV

To setup the u, v planes coincidence behavior, the register UVBHV is used (Table 3.23). This register is common for all four buses from the isolation cards A,B,C,D. The meaning of the individual bits of the register is explained in Table 3.25. Corresponding bit values represent selection between OR(0) and AND(1) function at the output of the u/v trigger logic block.

For example, to set all Roman Pots u, v planes in AND configuration, it has to be written 0x000F000F to the register UVBHV.

bits	meaning
31..20	unassigned
19	D bus Veto setup
18	C bus Veto setup
17	B bus Veto setup
16	A bus Veto setup
15..4	unassigned
3	D bus trigger setup
2	C bus trigger setup
1	B bus trigger setup
0	A bus trigger setup

Table 3.25: Trigger logic u, v coincidence behavior setup register UVBHV bit description.

3.3.3 Scalers setup and value read out

At the moment, the functionality of the scaler block for the trigger system monitoring is limited inside the electrical trigger firmware. There are four trigger and four veto scalers assigned to the logic block output and one scaler counting the bunch crossing 0 signal pulses. The scaler time-base is set by TMBS register (Table 3.26) and the possible values for configuration are described in Table 3.27.

reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5	14	TMBS	unassigned																															SCTB

Table 3.26: Scalers time-base read-write register (base-address 0x00840000).

SCTB 1	SCTB 0	time-base integration time [s]
0	0	0.01
0	1	0.1
1	0	1
1	1	10

Table 3.27: Scaler time-base possible configurations of integration time.

The actual scaler values can be read via the corresponding read only registers listed in Table 3.28.

reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
129	204	SCTA	unassigned																														trigger scaler value bus A	
130	208	SCTB	unassigned																														trigger scaler value bus B	
131	20C	SCTC	unassigned																														scaler value trigger bus C	
132	210	SCTD	unassigned																														scaler value trigger bus D	
133	214	SCBC0	unassigned																														scaler value BC0	

Table 3.28: Scaler value read-only registers (base-address 0x00830000).

3.3.4 Sampling stage calibration histogram

The sampling stage calibration histogram is an essential component for the electrical trigger calibration. A histograms for each channel is needed which means 128 histograms per FPGA. Such a number of histograms requires a lot of FPGA resources, thus these histograms cover only 64 bunch slots to reduce resources demands. The first bunch can be selected by programmable register as described in the following text. This allows to select desired bunch slots according to a concrete filling scheme. The histogram block diagram is shown in Figure 3.26. The first two important parts are the data delay and trigger delay blocks. The incoming trigger bit signals can be delayed by the delay data by up to 128 clock cycles using the programmable FSM and FIFO to observe the pre-trigger bus state. A histogram triggering signal is delayed by programming the delay trigger FSM which is started by the incoming signal and counts until the programmed value is reached. Then the delayed triggering signal is generated and propagated to histogram FSM. This means that the possible consecutive triggers are ignored by the system.

The biggest parts of the Histogram Logic are the histogram memories and FSM. The delaying trigger signal starts the histogram FSM. The reset signal sets the read, write counters and histogram memory cells to zero. Those counters defines the read and write memory addresses. In the same step the FSM is put in the wait state. Once the delayed triggering signal is received, FSM enables counters and sets memory read/write enable signals. As the counter values rise the corresponding memory cell is read. According the trigger bit value, the original or increased by one value is back-written to the corresponding memory cell. In parallel, the same value is stored into the output buffer memory. Once the read counter reaches maximum value, FSM goes again to the wait state. The output buffer memory block allows to access the histogram values in real time without canceling the histogram integration loop.

Histogram registers

To control and use the histogram, there are the following registers.

Reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	A0	HSTADDR	indirect histogram address																															
42	A8	TRGDELAY	delay trigger value																															
43	AC	HSTSEL	select histogram source																															
44	A8	HSTDEL	delay for the histogram data																															

Table 3.29: Histogram RW registers (base-address 0x00840000).

Reg.	address	name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
128	200	HSTVAL	Histogram value																															

Table 3.30: Histogram RO registers (base-address 0x00820000).

The first part is 128 bit wide programmable delay buffer (FIFO + FSM). This part is used to store pre-trigger data. The second part is the trigger delay FSM.

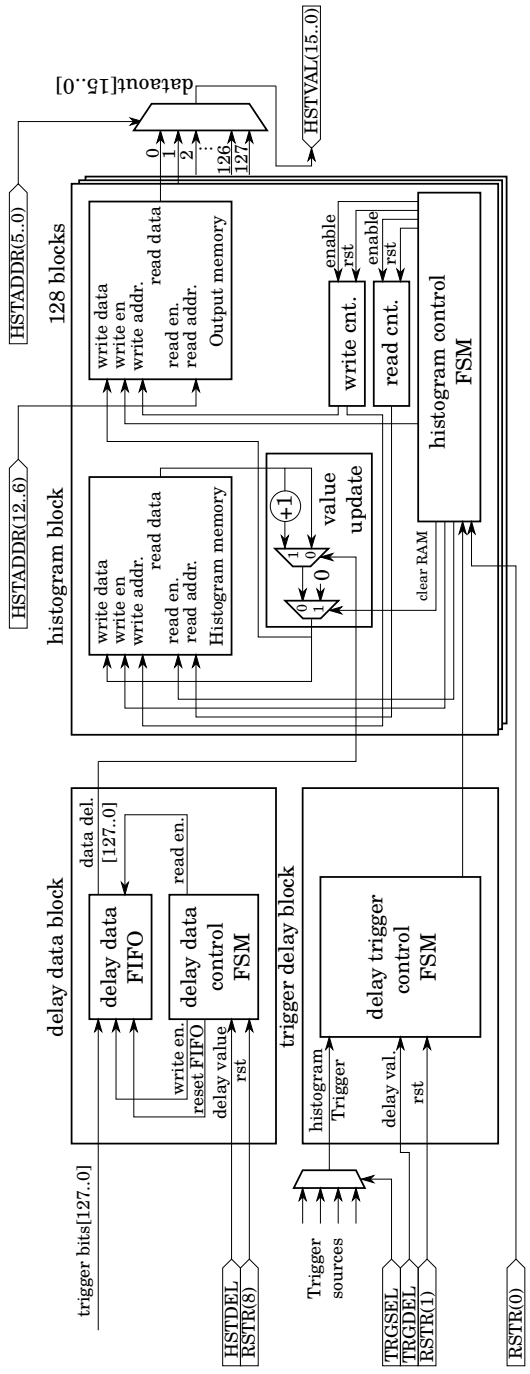


Figure 3.26: Electrical trigger sampling stage calibration histogram block for calibration purposes is shown in this figure. It contains three main blocks. A data delay block is used to store pre-trigger conditions (up to 128 clock cycles). A delay trigger block is used to delay a start histogram trigger signal. A histogram block contains a controlling FSM and two blocks of memories. According to the input rigger value the memory value is increased by one, back stored in the memory and stored in the readout memory. This allows a real-time readout without canceling a histogram accumulation process.

3.4 LONEG Firmware overview

The pre-processed trigger information (by the OptoRx or electrical trigger firmware) from each detector is send into the LONEG mezzanine card while each detector is represented by a set of trigger bits. A block diagram of the LONEG firmware is shown in Figure 3.27. In the first step, the trigger bits enter a programmable delay block to synchronize all trigger bits from individual detectors because each detector has different distance from the IP and the signals are delayed due to the cable length and the time of flight of the particles.

In the 2 step, there is a mask for disabling detectors that are not desired to participate in trigger and a programmable monostable is applied, allowing to stretch the trigger bit for up to 16 clock cycles. The default value of the monostable length is one clock cycle for the Roman Pots and four for T1 and T2. This values are chosen based on a detector technology and the consequent detector signal development that jitters for more than three clock cycles.

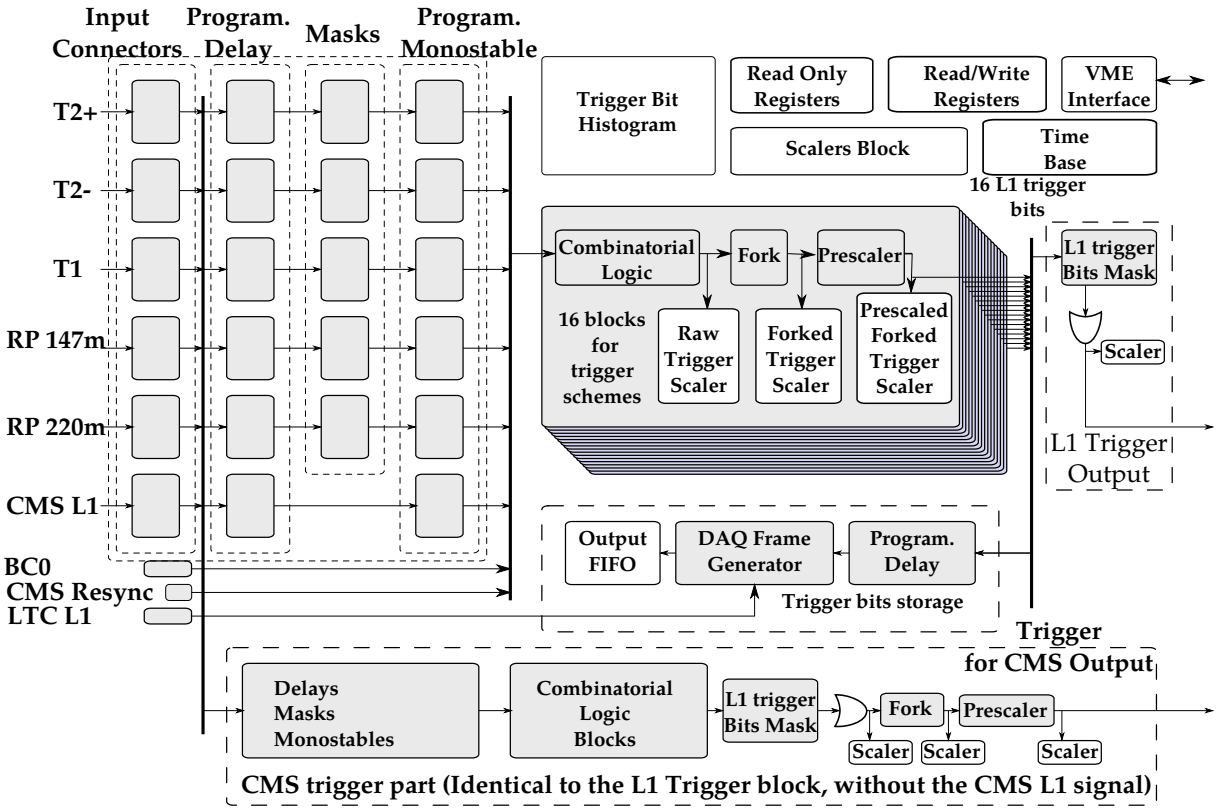


Figure 3.27: Block diagram of the LONEG firmware.

Once all the bits are synchronized, they enter the individual trigger schemes combinational logic blocks related to TOTEM physics program. For example, the elastic scattering measurement requires a proton in a vertical Romans Pot on one side of IP5 and one proton in a diagonal vertical Roman Pots on the other side. Then the signal is compared to the so-called "fork" which is a programmable gate containing information about a beam filling scheme structure allowing the trigger signal to be further propagated only in the time slots of bunch collisions in order to eliminate possible noise. At the end of the block there is a pre-scaler allowing to reduce a trigger rate. Also a scaler in each step of the logic block is implemented allowing a trigger online monitoring and a rate optimization. Also the coincidence of the trigger and the

fork is very important for us because in the ideal case, the rate before the fork and after the fork is the same and any difference indicates that there is a problem with a system timing or that there are noisy channels generating false trigger bit signals. The output trigger bits from all the trigger combinational logic blocks go in two different blocks. One is used to store the trigger bits together with the DAQ data for the offline analysis. The second one is the output stage for the L1 trigger. This stage contains a mask for individual trigger schemes masking to choose desired trigger function schemes followed by the OR function to combine trigger bits to the final trigger bit – Level one (L1) trigger bit – and it's output is connected to the LTC block and it drives directly the data read out request from all detectors. For the purpose of the TOTEM, CMS trigger integration, the entire TOTEM trigger block was duplicated allowing to generate and propagate an independent trigger information to CMS. This information is processed by CMS and the result is returned to TOTEM and may be used for triggering the TOTEM experiment.

A way how the TOTEM and CMS trigger systems are merged together is shown in Figure 3.28.

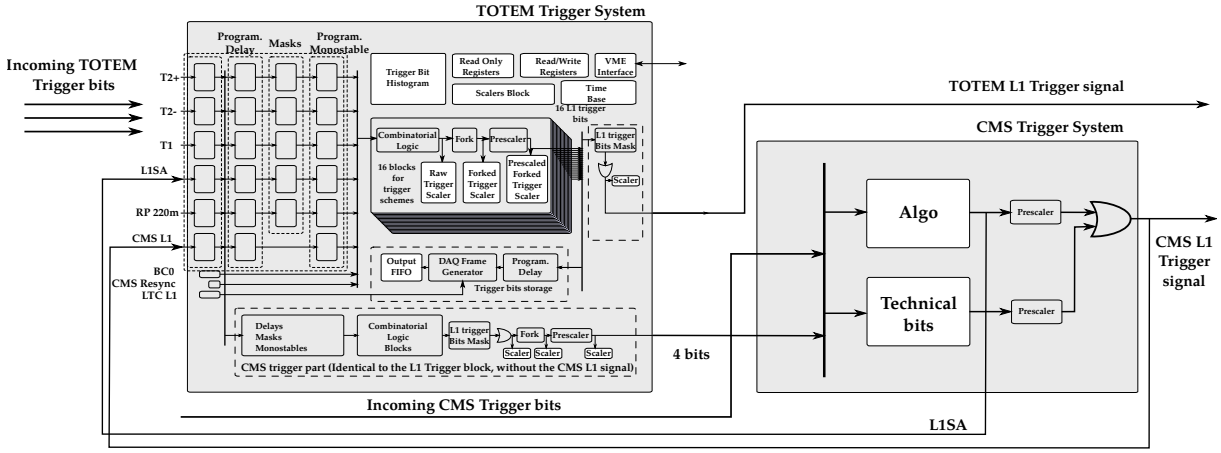


Figure 3.28: TOTEM-CMS trigger exchange. Totem and CMS trigger signals arrive to corresponding systems. Firstly, TOTEM experiment applies CMS related trigger conditions and propagates results to the CMS detector. The CMS trigger system process this information together with its own trigger signal and sends global L1. TOTEM experiment receives back L1 and L1SA signals (a special subset of L1) and mix it with its own trigger menu and TOTEM L1 is generated.

Chapter 4

TOTEM trigger system results, measurements and calibrations

The TOTEM Trigger system calibration and commissioning was a challenging part of the trigger system development. The system required its individual blocks to be tuned and calibrated to make all the parts to work together.

Section 4.1 shows latency measurements needed for system time alignment. This includes measurements of detector trigger signal delays needed for FIFO's configuration values and VFAT latency scans. The measurement method is explained and several examples are given. In order to perform the above measurements, the entire system must be fully configured and operational which requires a cooperation between TOTEM experts. Also LHC has to be in operation to allow the author to proceed with these measurements.

Section 4.2 discusses the first data of the experiment. The author uses these measurements to demonstrate the functionality of the entire system. For physics descriptions and results see [26]-[33].

An example of trigger efficiency studies is shown in Section 4.3.

Section 4.4 describes author's measurements during the electrical trigger installation and commissioning. A way of powering repeating devices is mentioned (due to radiation levels in LHC, the repeating devices are powered over a large distance and voltage drops has to be taken in a count. Radiation levels prevent power supplies to be safely operated locally). Also connectivity tests, sampling stage calibration and Roman Pot detectors PLL phase tuning are discussed.

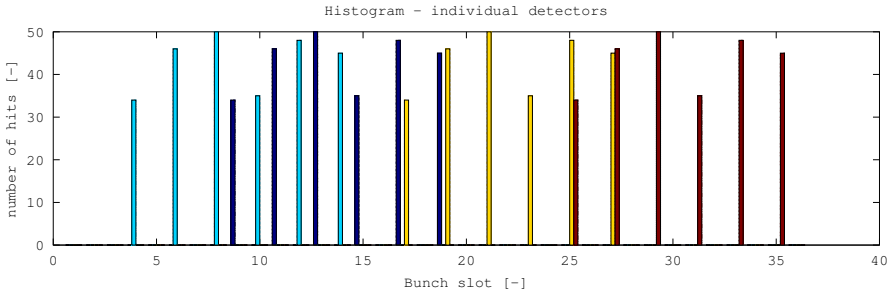
The final measurement of a delay of the optical and electrical trigger links is discussed in Section 4.5.

The electrical trigger was needed to combine data from TOTEM and CMS. Common operation is an important achievement based on this thesis and is demonstrated in Section 4.6.

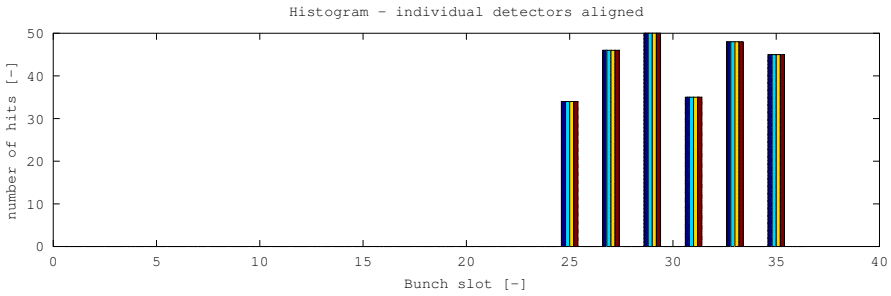
4.1 Trigger system - timing

Individual detectors are displaced by hundreds of meters which complicates the overall system calibration and also the access and diagnostics on the spot during an LHC operation is not possible. On the other hand, the precise timing is essential because, for the trigger system, every clock cycle represents a unique time window. Also in each detector, the particles incoming from a single event are detected in different time windows. Thus to combine all the information about events we have to relate individual detectors data (from different time windows) together.

4.1.1 Detectors delay FIFO configuration and trigger bit histogram importance



(a) Unaligned trigger signals.

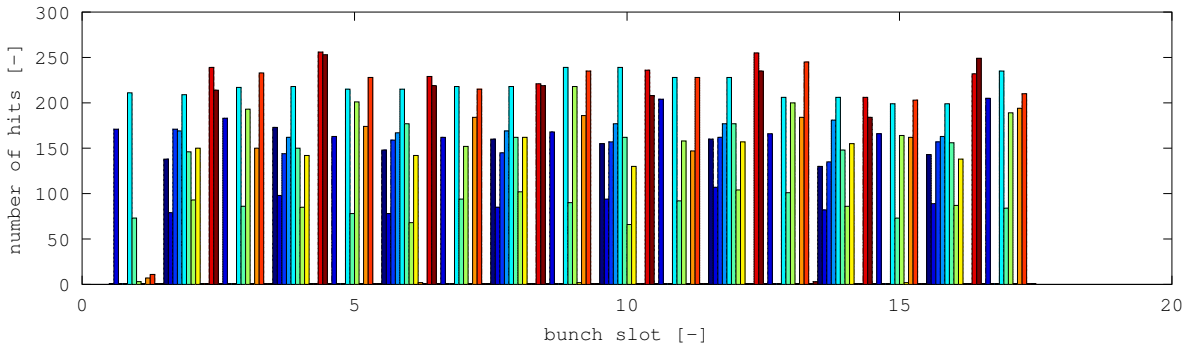


(b) Aligned trigger signals.

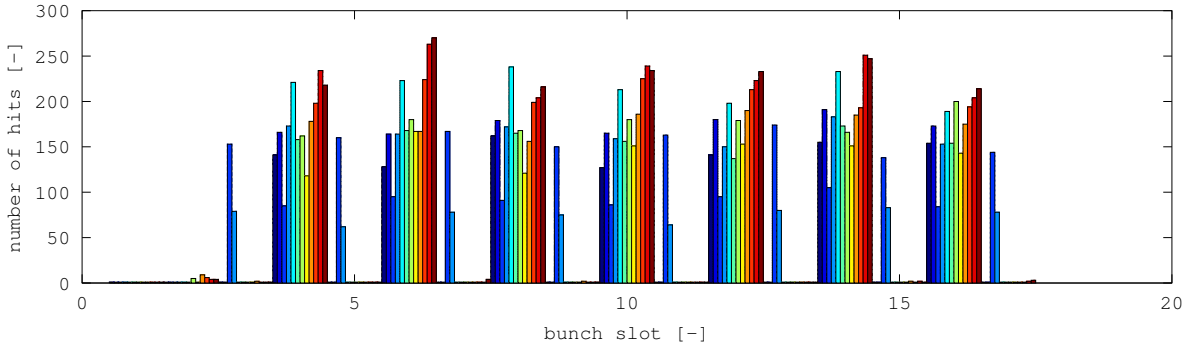
Figure 4.1: Illustrative (non real) trigger signal histograms and their time alignment. The x axis represents bunch slots orbiting LHC with 25 ns spacing and each slot can be populated with particles. Detector are represented by a different color. In Case (a), detector trigger signals arrive in a different time due to different latencies. Case (b) shows histogram made after delaying signals accordingly to the latest one.

Trigger data from different detectors arrive into the counting room with different delays. This is mainly due the following two facts:

- detectors are located at different distances from IP5 thus transmission lines with different lengths have different propagation delays and
- particle time of flight from the interaction point to detector increases the trigger signal latency.



(a) Unaligned trigger bit signals



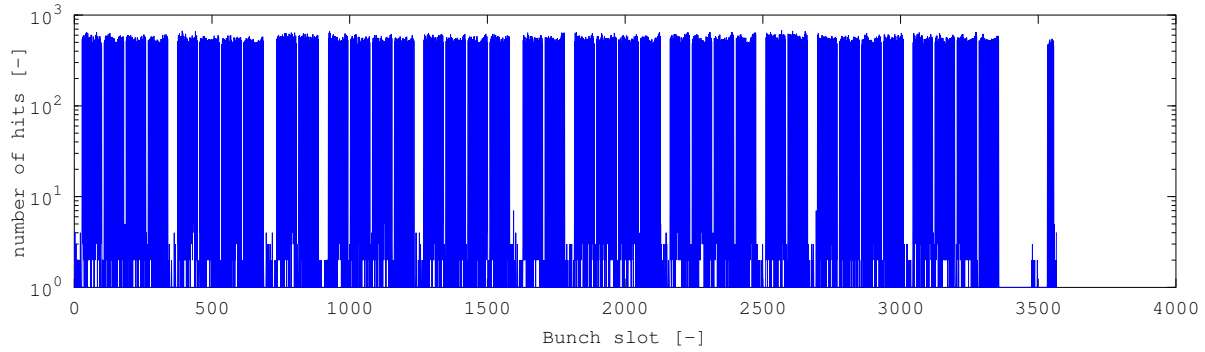
(b) Aligned trigger bit signals

Figure 4.2: Roman Pot Electrical trigger signals and a real world measurement. Both graphs show the same part of trigger bit histograms (single train) for all twelve Roman Pot detectors (each color represents a single Roman Pot). Case (a) shows unaligned trigger bit signals. Case (b) shows the situation after the alignment. The train is visible in Case (b) (a space between occupied bunch slots) and the trigger bit signals are in the same bunch slots except two RP. Their trigger bits are split in two neighboring bunch slots – in this case it is a problem of local PLL settings (explained later).

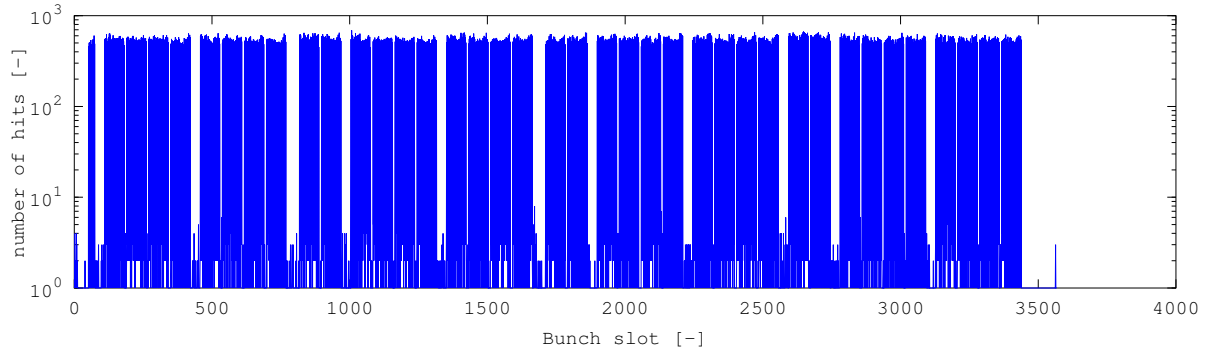
First of all, the incoming trigger data have to be synchronized. The reference is given by a trigger signal with the longest delay. All the Trigger data are delayed by a programmable FIFO accordingly to the reference. A good solution to find correct configuration values for delays FIFO is provided by histograms of trigger bits for each detector. The result of such measurement is a set of histograms shifted in time. This shifts correspond to values we need to program into FIFO FSM control registers for signal delays.

An illustrative example is in Figure 4.1. It shows a single train as might be seen by individual detector histograms before (Case (a)) and after (Case (b)) the alignment. Mainly histogram patterns are important for us. Amplitudes may vary for different detectors and bunch slots due to many factors e.g. beam distances, bunch occupancy etc. Figure 4.2 shows a real histograms for all twelve individual Roman Pot detectors. In this case two Roman Pots have a problem with its internal PLL clock and the histogram peaks are decaying into two neighboring bunch slots – a solution to this problem is described in Sub-section 4.4.4.

The last thing that has to be done to check that the pattern in the final trigger histogram corresponds to the LHC filling scheme. If the pattern is shifted with respect to the filling



(a) Rotated histogram. In this case a bunch 0 peak with lower intensity appears around bunch slot 3500.

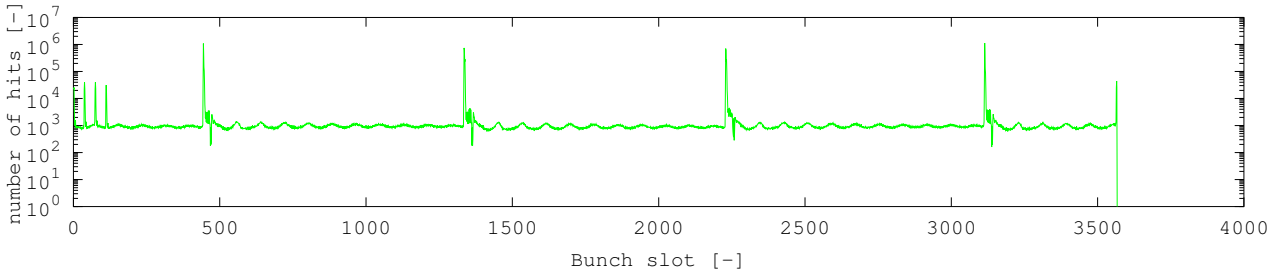


(b) Histogram made after the shift correction. Bunch 0 is present at bunch slot 0.

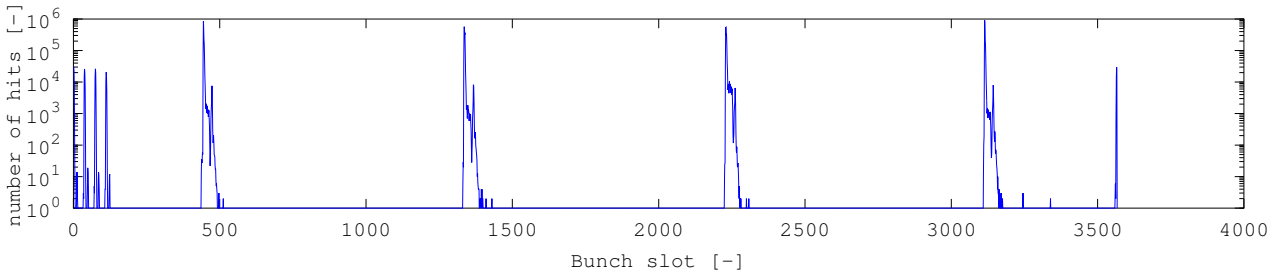
Figure 4.3: Final trigger histogram. This histogram was taken before the long LHC upgrade period. It shows the beam structure of highly populated beams. Case (a) shows the situation when bunch crossing 0 signal adjustment register was badly programmed. This causes a rotation of the histogram. Case (b) shows a histogram with the correct value programmed. The entire beam structure is rotated with respect to Case (a).

scheme, it means that the bunch crossing 0 signal is not synchronous with the system and the corresponding delay FIFO for this signal has to be reprogrammed too (Figure 4.3).

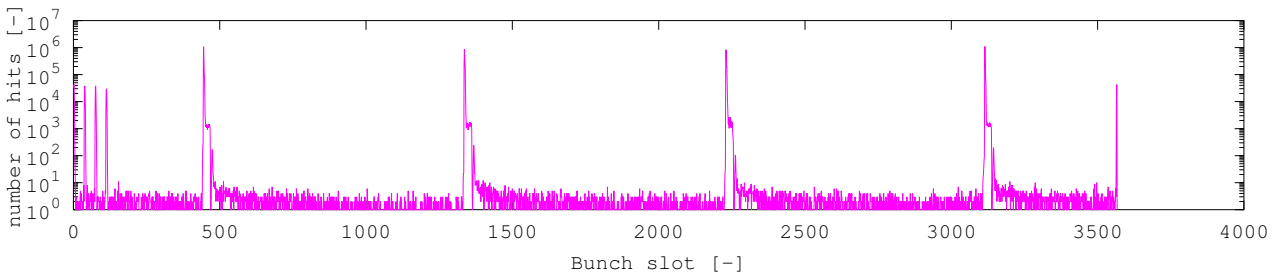
Finally, Figure 4.4 gives an example of the histogram importance for detector performance analysis. This figure shows the first histograms of the trigger bits of T2. In this case the histogram was done on software level and it took about twenty minutes to make it. The result was really surprising. A problem with high voltage dividers for the GEM foils was found out for all four quarters of T2 and it had to be resolved (this demonstrates an importance of histograms for the trigger system). Since than many histograms were implemented directly inside the FPGA firmware and we can monitor the trigger system almost in real time to detect possible problems.



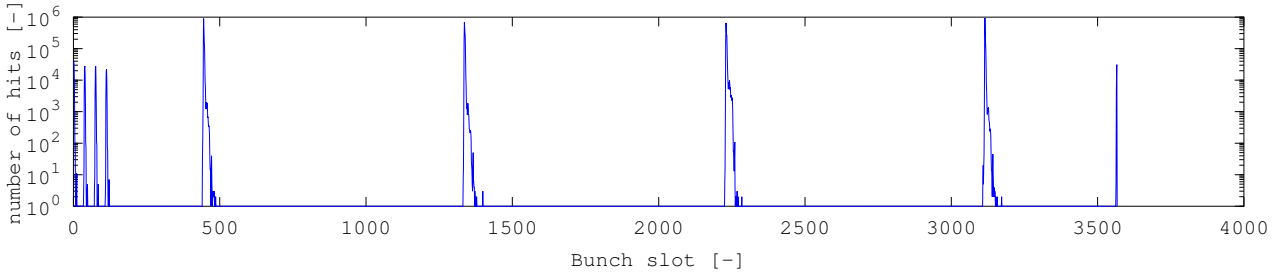
(a) T2 Plus Far



(b) T2 Plus Near



(c) T2 Minus Far



(d) T2 Minus Near

Figure 4.4: The first measurement of the trigger bit histogram for the T2 detector. Scalers integrate the number of the trigger bits over time. This means that the important value is lost – the trigger bits distribution in time. Those first histograms have been produced basically just for author's curiosity to see this time distribution. The result was surprising and the histograms became very important part of the system (e.g. they are used to see a noise distribution). In this case they, shown also that the T2 detector was loosing its efficiency due to the charge depletion in GEM (the sharp peak at the beginning of each train).

4.1.2 VFAT latency scan

Once the trigger system is correctly configured, the VFAT latency has to be investigated to provide correct data to the DAQ system. A simplified diagram of VFAT is in Figure 4.5. The incoming analog signals from the sensor are continuously converted into digital data by the analog-front-end block and stored into the local delay buffer. In parallel, trigger data are

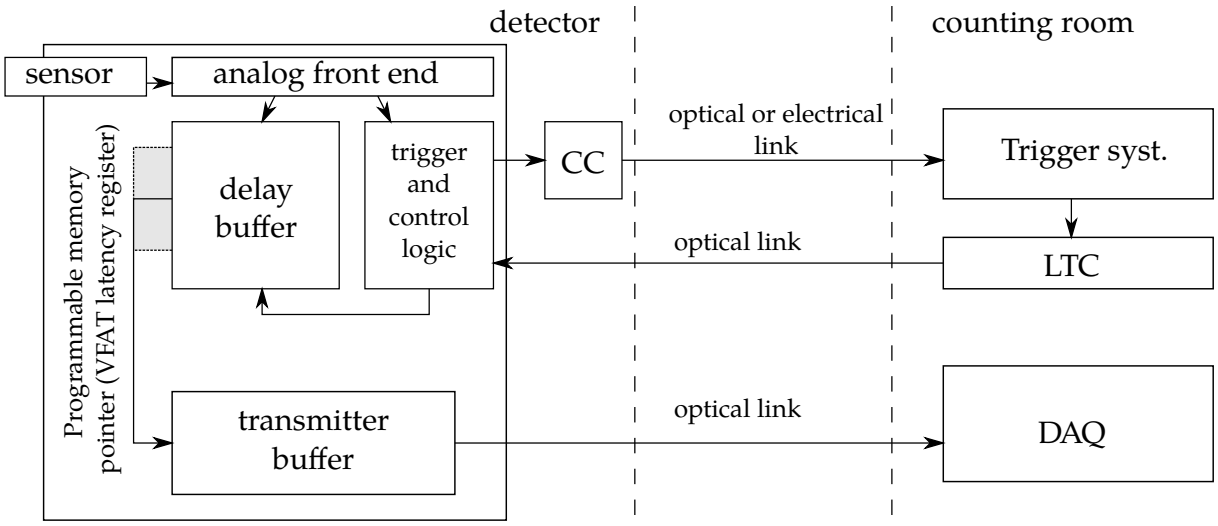


Figure 4.5: VFAT programmable latency buffer. Each VFAT chip continuously samples input signals and stores values in a local buffer. Once triggered, the chip transmit buffered data via DAQ. To select specific buffer memory position a corresponding register with a correct value has to be programmed. The latency scan measurement has to be performed.

generated and transmitted to the counting room for evaluation. According to the selected physics criteria, the data-read-out request (L1 signal) is generated by the trigger system and transmitted back to VFAT . Once the detector receives the L1 signal, the data stored in the buffer are copied from the memory position based on the value of VFAT latency register into the transmitter buffer. The goal was to find the correct latency register value for each VFAT chip in the system. The length of this VFAT-trigger system transmission loop is up to 600m and it's the overall latency is about 3 μs. This corresponds to 120 clock cycles and indicates the starting point for the so-called "latency scan". A principle was following: We selected a single detector as the trigger source and we evaluated data measured by this detector. If the latency value written in detector's VFATs was correct, not empty tracking data had to be stored. In contrary, if the latency was incorrect many zero value data were stored by DAQ – in such case new value value was written to the VFAT register and the measurement was repeated.

4.2 Triggering the TOTEM experiment

Once all the TOTEM systems are calibrated, it is possible to start looking on real events. The simplest way to trigger the system is to use the minimum bias trigger to store event data when any trigger bit is active.Even when the minimum bias trigger is not optimal for the consecutive physics analysis. The trigger system evolved over the years but the first sets of data have been taken only using minimum bias trigger. Figure 4.6 shows a visualization of the first data from

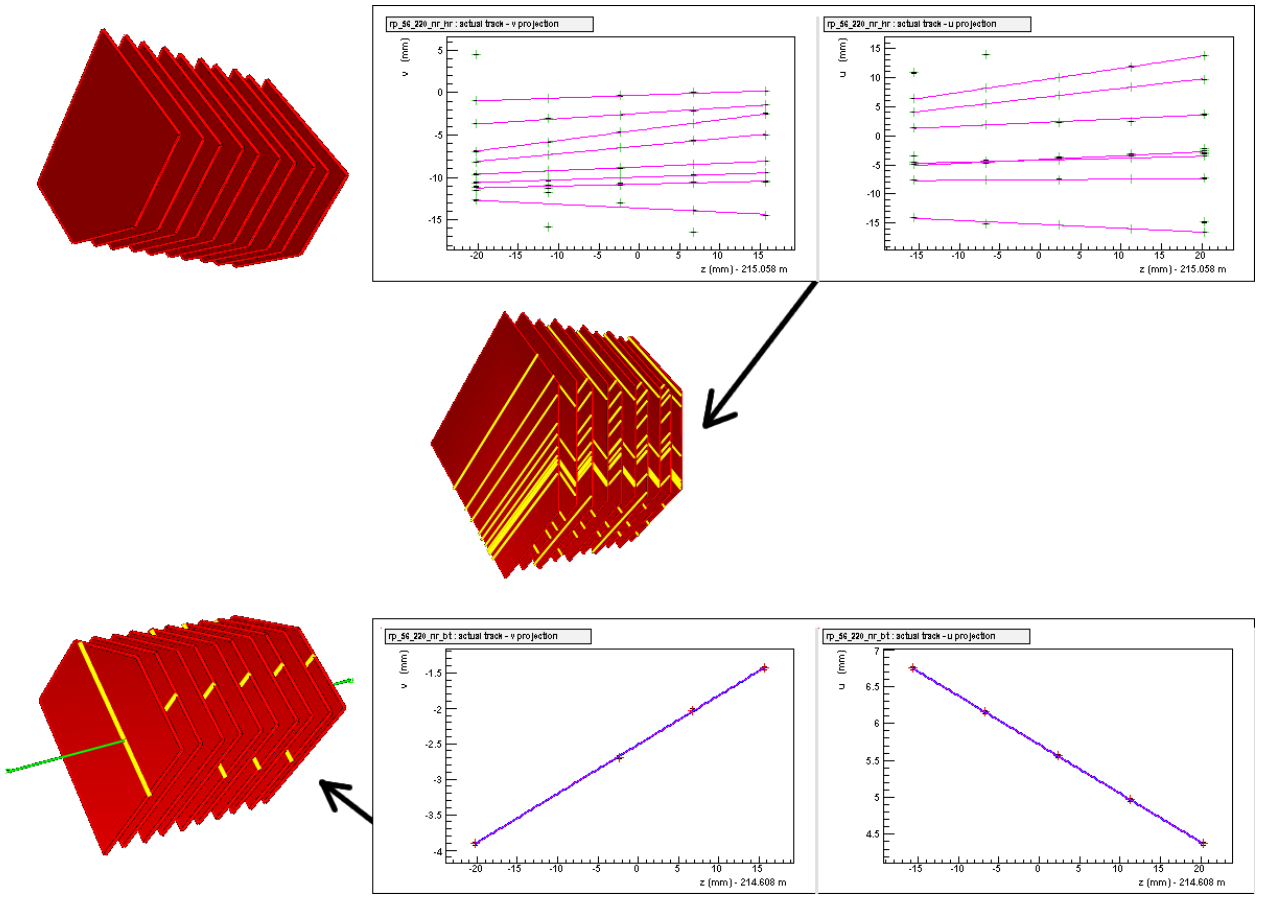
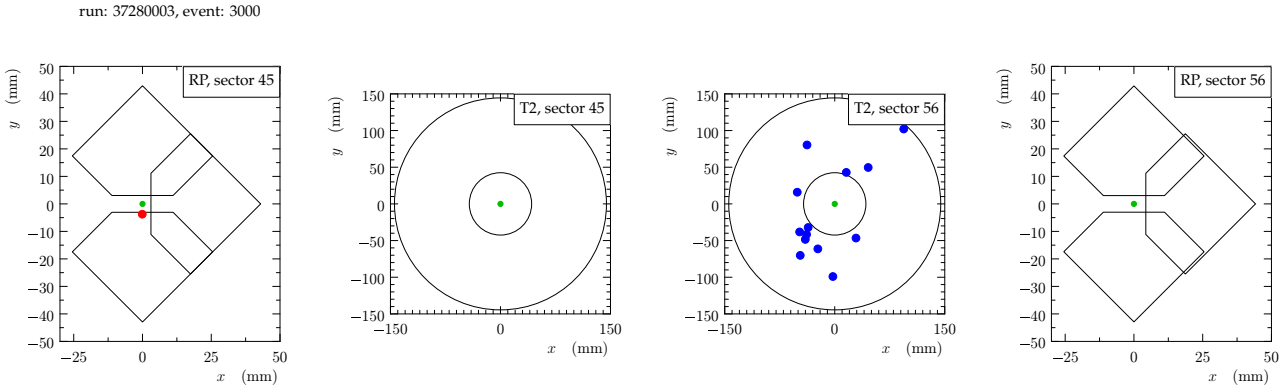


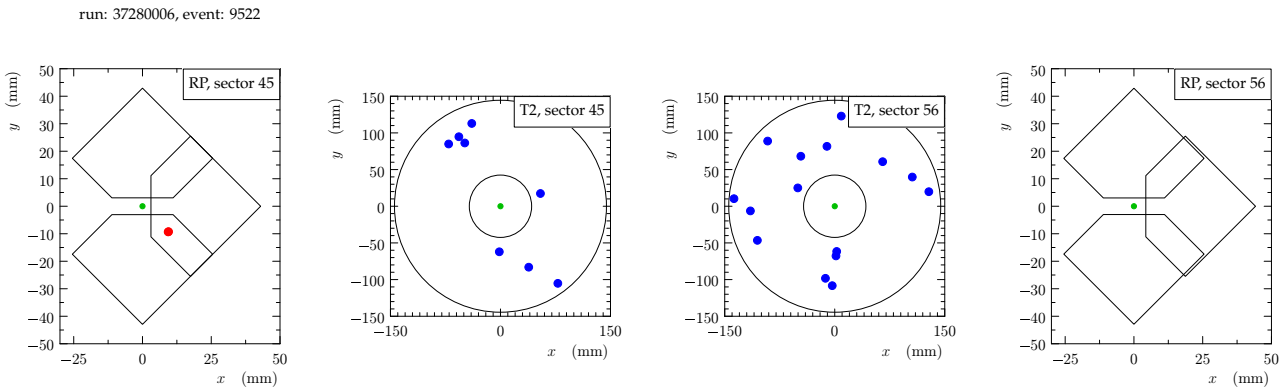
Figure 4.6: One of the first events recorded by the TOTEM experiment. Two Roman Pots are hit by particles. The bottom Roman Pot is hit by a single proton. The horizontal Roman Pot is hit (probably) by the particle shower. The green line shows the reconstructed track in the bottom Roman Pot (multiple hits in the horizontal Roman pot does not allow the tracks reconstruction).

the LHC collisions. The proton hitting the bottom Roman Pot has its origin in a proton-proton collision at IP5. The particle shower detected by horizontal Roman Pot is most probably caused by a proton hitting a piece of material in LHC close to the Roman Pot detectors.

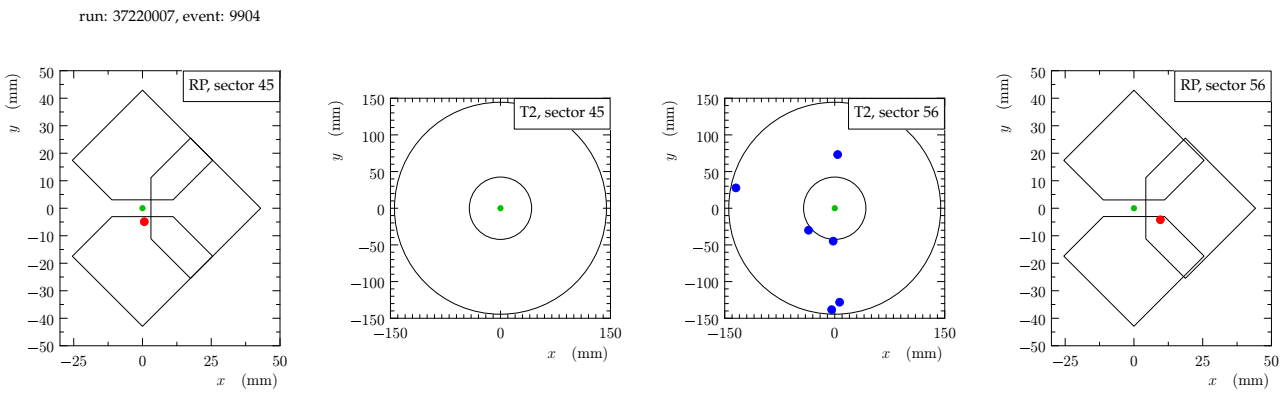
Figure 4.7 shows a visualization of several event types in the TOTEM detectors. At this point the author would like to recall Figure 1.7 from Chapter 1.



(a) Single diffraction (low momentum loss) - In this case one proton survives the collision and is detected by the RP in sector 45(red dot). Some of the particles created under small angles are detected by the Telescope 2 in the sector 56v(blue dots).



(b) Single diffraction (high momentum loss) - In comparison to the previous case, as the momentum loss grows, the newly created particles are spread over larger area and are detected by both T2 detectors.



(c) Double pomeron exchange. Both protons survive the collision in IP5 however their momentum loss allows for new particles to be created and subsequently detected by the T2 detector.

Figure 4.7: Examples of physics events as seen in the TOTEM experiment (green dots represent the beams).

4.3 Trigger efficiency studies

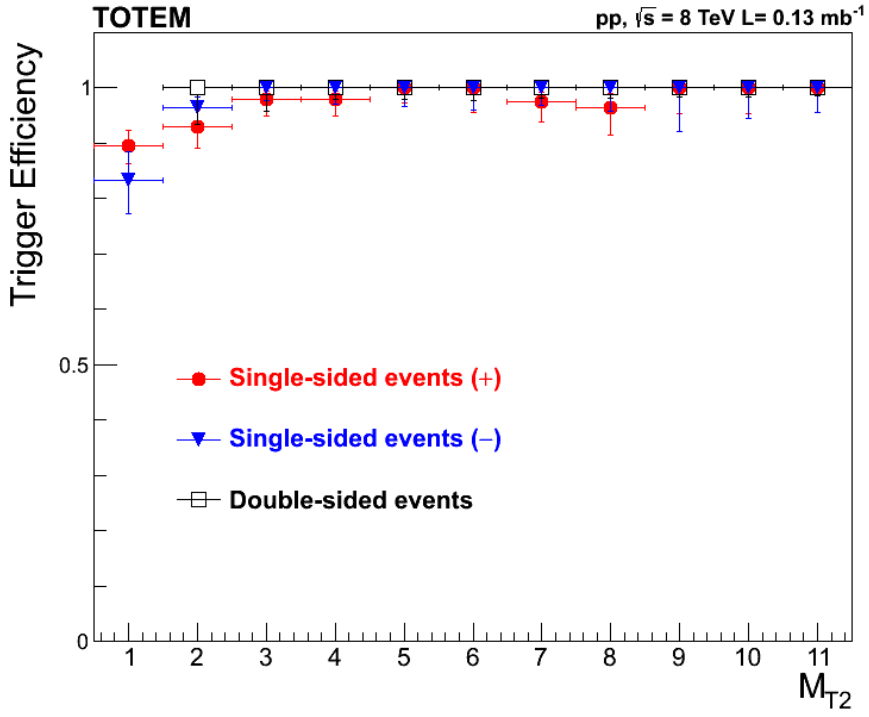


Figure 4.8: The graph shows the trigger system efficiency for the T2 detector (for a single measurement). On the horizontal axis, there is a number of tracks per event in T2 detector (only plus side arm , only minus side arm, both arms). On the vertical axis, there is a trigger system efficiency for the corresponding number of tracks. The efficiency for single track events is low due to a large number of masked noisy trigger channels.

The trigger efficiency and purity are the most important parameter characterizing the overall trigger system performance. The trigger performance studies are done by the TOTEM physics analysis group and for this reason the author shows only an example. Figure 4.8 shows results of the trigger efficiency studies for T2 during a single measurement of proton-proton interactions. To determine the trigger efficiency, a sub-sample of data triggered by a bunch crossing trigger has been used. The event type was determined and the corresponding event trigger bit stored by DAQ was checked (e.g. if an event was identified as elastic then an elastic bit was checked). In the graph there are values for three types of event: only the plus arm of T2 was hit, only the minus arm of T2 was hit and both arms was hit. On the horizontal axis, there is the number of tracks per event. The low efficiency of the T2 trigger for single track events is caused by dead or masked noisy channels.

4.4 Electrical trigger calibration and commissioning

4.4.1 The first power up

The first important step after the installation of the electrical trigger chain was to power up the system. the power supplies for the electrical trigger are located in a service cavern since they need to be shielded from radiation. The power for the repeaters is distributed via 300 m long cables, the voltage drop over the power line is not negligible and the voltage regulators could not be used due to radiation. For this reason, thick power distribution cables were used to distribute power for the repeaters to decrease the voltage drop. The power distribution had to be checked step by step and its functionality and stability had to be verified. The power supplies for the repeaters has its voltage sense wires connected to the power line close to the Roman Pot detectors, about 30 m from the power supply. This has two main reasons. The power supply provides voltage measurement and corresponding value is stored in an online database. Like that we monitor the maximum voltage applied to the repeaters. Also, this power line is about 300 long and the author worried about the stability of the control loop if longer sense wires were used.

Sector 45	Current [A]	Patch Panel [V]	Cab. 1[V]	S Cab. 2[V]	Cab. 3[V]
No cabinet	0	2.56	–	–	–
Cab. 1	1.26	2.54	2.46	–	–
Cab. 1+2	2.14	2.54	2.38	2.32	–
Cab. 1+2+3	2.89	2.54	2.32	2.20	2.15

Table 4.1: Electrical trigger power distribution commissioning in Sector 45. The 70 m long cable segments were plugged one by one and the voltage was measured at each segment. Also the total current was measured. For commissioning purposes, the power supply output was set to 2.56 V.

Sector 56	Current [A]	Patch Panel [V]	Cab. 1[V]	S Cab. 2[V]	Cab. 3[V]
No cabinet	0	3.01	–	–	–
Cab. 1	1.67	3.01	2.88	–	–
Cab. 1+2	2.88	3.01	2.79	2.707	–
Cab. 1+2+3	3.91	3.00	2.726	2.56	2.51

Table 4.2: Electrical trigger power distribution commissioning in Sector 56. For commissioning purposes, the power supply output was set to 3.01 V.

At the beginning, the author tested the repeaters in a lab. The nominal voltage value for the used silicon technology in the repeater chip is 2.5 V. In a real setup, they worked reliably in a range from 1.7 to 4.0 V. Any higher voltage would cause a permanent damage. The lower bound of the range is determined by internal current sources of the repeater chip that stop to operate correctly. Based on these measurements, different initial values for a tunnel installation in each sector, 2.5 V in Sector 45 and 3 V in Sector 56, were used to obtain corner values and to check the system operation during the power-up tests. The author connected the repeater cabinets one by one and measured the voltage drop in each cabinet. The results for sectors 45 and 56 are

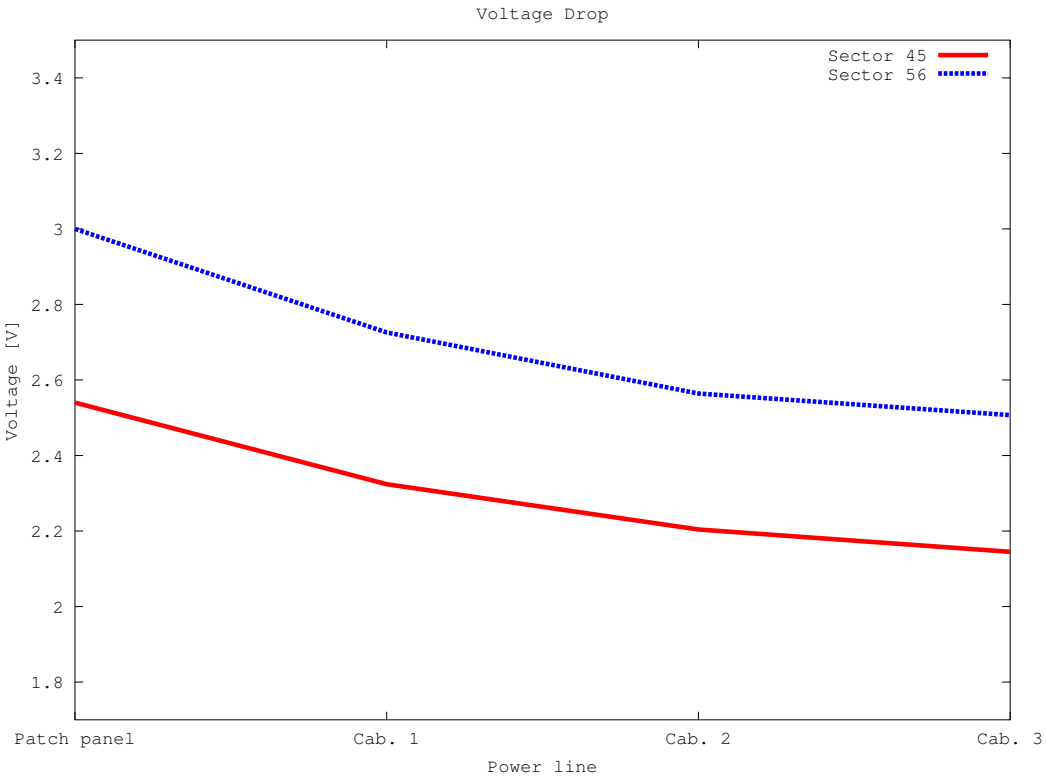


Figure 4.9: Electrical trigger power line voltage drop due to the resistance of the power distribution line. Once all repeaters were connected, the voltage at each cable segment (repeater cabinet) was measured. The graph shows consistent (similar) voltage drop between the cabinets two different power-supply settings – Tables 4.1 and 4.2 .

in Tables 4.1 and 4.2. The voltage and current measurements are similar between the sectors and only reflect different initial voltage settings. Test measurement results in both sectors are visible in Figure 4.9. In both cases, the system was stable and there were no fluctuations of voltage levels. For normal system operation, author decided to use 2.75 V as an initial value for the repeater power supplies in both sectors .

Unfortunately, during this test, the author found a flaw in a design of an electromagnetic shielding. The repeater box panels were made of anodized aluminum and D-SUB connector was creating enough stress to penetrate the isolating oxidized surface layer. This was causing ground loops in the shielding. To fix the problem, all the metallic panels were substituted with plastic ones (See Figure 3.20).

4.4.2 The first connectivity test

To do the first electrical trigger connectivity test, the transceiver card was used to pulsed all channels one by one in order to check that signals are propagated to FPGA over the line. To read out the FPGA pins corresponding to the signals, the Signal Tap Analyzer tool was used as it provided a sufficient way how to check all the trigger lines from the Roman Pots to the CMS counting room. The results of this test are shown in Figure 4.10 and listed in

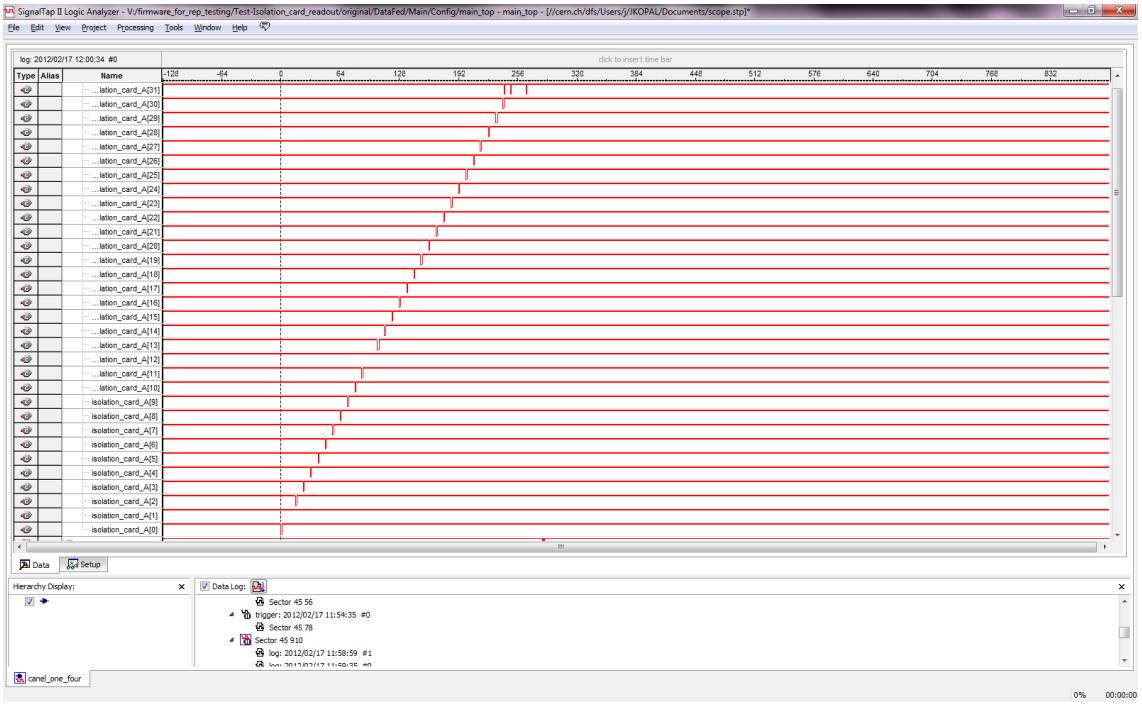


Figure 4.10: Test of the full length electrical trigger lines. Individual lines were pulsed. The pulse sequence measured at the very end of the chain is shown in this figure. Three channels 1, 2 and 31 can be identified as not working properly due to bad connections between connectors.

Table 4.3. Several dead channels were identified but it was decided to keep the system as it is because the installation took the place during the short so-called "Christmas shut-down" with a limited time window. The dead channels affect the trigger efficiency according to the trigger configuration and the type of the physics measurement. Figure 4.11 shows the mapping of dead channels to corresponding Roman Pot detectors channels. In most cases, TOTEM uses non-restrictive criteria for the trigger logic. This means that u and v planes and also near and far units are in OR mode. Therefore only the intersection points of the u and v projection strips. If only one projection is disabled the area is covered by redundant information from orthogonal projection. The totally blind spots are in less populated areas of the silicon chip. Also the near and far detectors generate redundant trigger information. To conclude, this small number of dead channels is not an issue for physics analyses, where a correction for the trigger inefficiency due to the missing channels can be performed.

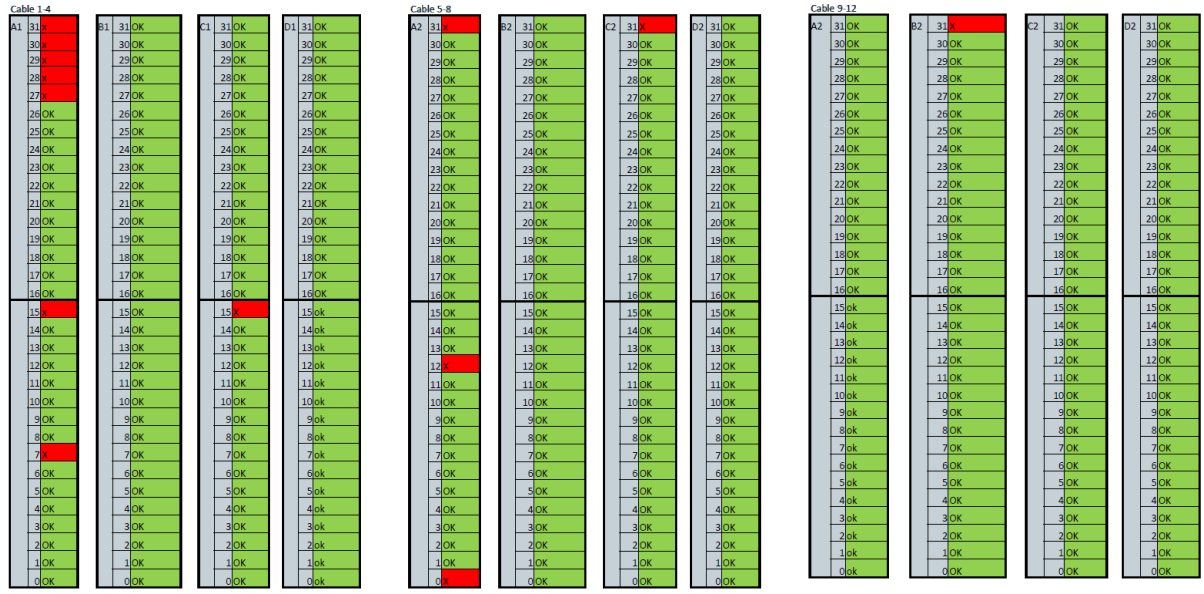


Table 4.3: Table shows a current status of all the 384 LVDS trigger bit lines of the electrical trigger after the installation during the winter shut-down in 2013. Most of the lines are working correctly but there are some broken connections.

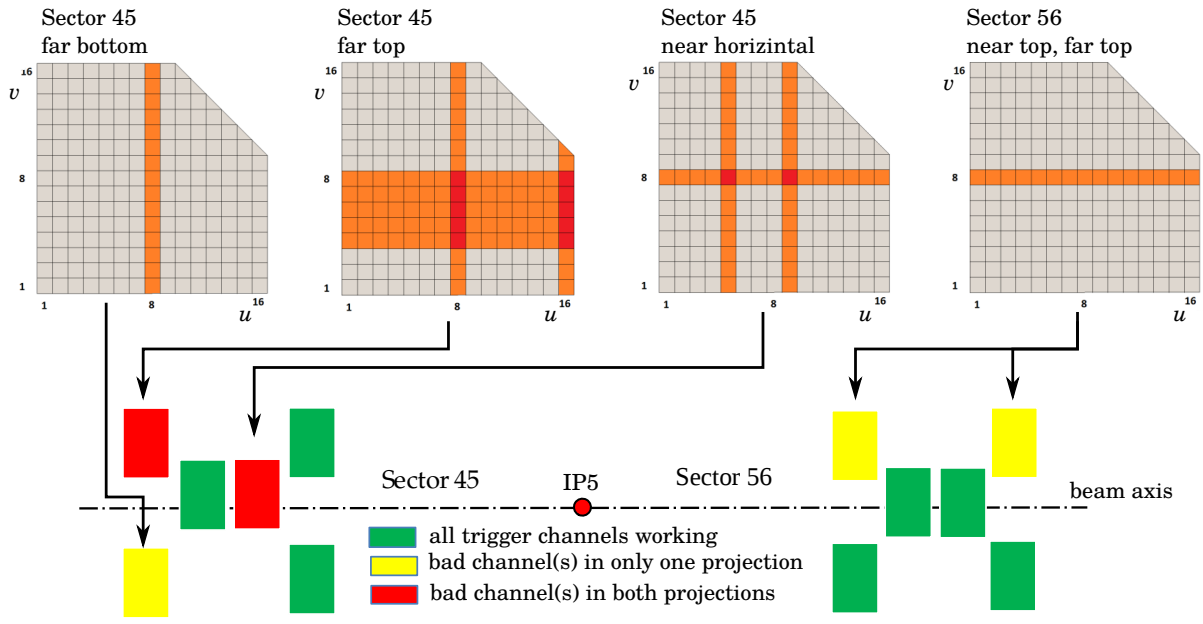
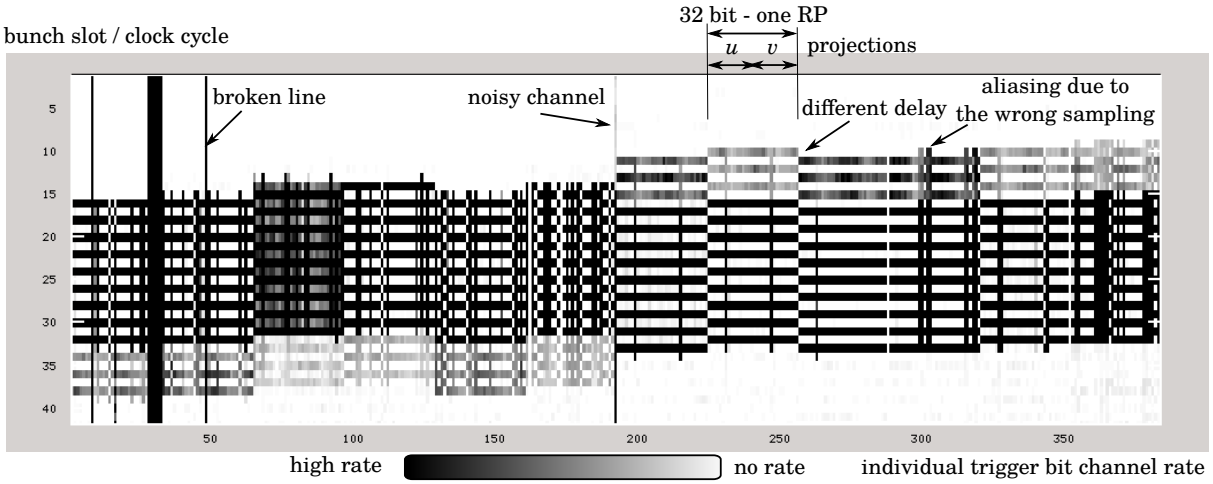


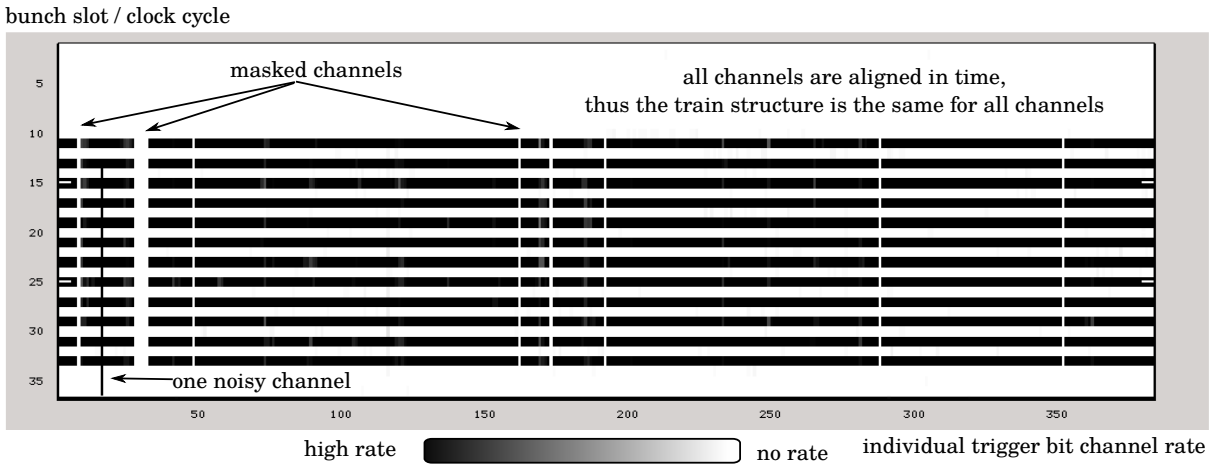
Figure 4.11: Mapping of the trigger links to the trigger strip sectors of silicon chips of the Roman Pot detectors. In most cases, the logic function OR is used to make a coincidence between trigger strip sectors in the u and v projections. In such case, the trigger system is not capable to trigger only when a particle hits an areas of an intersection of two strip sectors with broken connections (red color). However, the trigger efficiency is lower for the area covered by the signals from one projection due to the non-100% detector efficiency (orange color).

4.4.3 Signal sampling

The main challenge for the electrical trigger firmware is to setup the receiving part of the electronics to sample correctly all 384 incoming trigger bit signals. For this purpose, a special



(a) The input sampling stage is without a calibration and default values are written to it's control registers. The sampling stage does not work properly and output signals are not aligned in time (the train structure looks different for each trigger bit channel) and also a signal aliasing is present (trigger signals are stretched over more then one clock cycle). Broken line channels are not masked.



(b) This histogram was made using calibrated input sampling stage. Once calibrated, the input stage provides in-time synchronized trigger signals (the train structure is the same for every channel) for all Roman Pot detectors. Faulty channels are masked.

Figure 4.12: Electrical trigger input sampling stage histograms show a train structure of an LHC beam with a 50 ns spacing as seen by the trigger system with and without a calibrated sampling stage.

block (Figure 3.23) for each channel was implemented – the sampling stage. The author used an FPGA internal PLL and the 40 MHz input clock (synchronized with LHC) to generate four internal clock signals with the same frequency, but with a phase shift of multiples of 90°. An asynchronous multiplexer driven by a programmable register selects the clock source for a sampling synchronous D flip-flop to prevent possible meta-stability in the circuit. After this block the signal continues into a pipeline of a D flip-flops driven by the original clock. Each

stage of the pipeline goes to the final multiplexer (also driven by the register). The first part of the block allows to compensate the phase shift. The second part allows to compensate signal delays.

To calibrate the system, corresponding register's configuration values had to be obtained and written into the corresponding internal registers. To do so, there were several processes that had to be understood before getting calibration values. Thus first of all, Roman Pot clock phases had to be tuned with respect to the passing beams using programmable PLL and then four histograms of all incoming trigger bits were made for the input stage using all four clock phase setting in sequence. Those histograms are two dimensional. The horizontal axis represents all trigger bits (384) and the vertical axis represents Bunch slots. To reduce an FPGA resource usage, this histogram is limited to 64 bunch slots (the first bunch slot can be selected by a programmable register). The uncalibrated histogram is in Figure 4.12(a). For the trigger purposes, all the trigger signals have to be realigned in time and the sampling phase has to be selected using programmable registers. To get appropriate configuration values for the input sampling block registers, the author wrote an automatic program which records four individual histograms, one for each possible phase shift, combines them together and makes an analysis of combined data to obtain correct configuration values. The output of the program is a new configuration script. Figure 4.12(b) shows the trigger bit histogram after this new configuration script applied to the trigger system. The impact of the sampling block is significant: the peaks in the histogram are very well aligned in time.

4.4.4 Roman Pot detector PLL clock phase shift calibration

A critical step in the overall Roman Pot calibration is to determine the correct Roman Pot PLL clock phase shift for each detector to achieve one-clock-cycle time resolution because if the clock phase is not optimal, then detector output signals (both: trigger and tracking data) can jitter between two neighboring buffer memory slots, as shown in Figure 4.13, and in such case one-clock-cycle time resolution can not be achieved.

Finding the correct PLL phase is difficult because the detectors are displaced in space, there are inevitable delays in control loops that distribute the synchronous LHC clock and also bunches are in motion. Furthermore, the detectors and LHC are not accessible while the particle beams are present in LHC thus no direct measurement on electronics is possible. Only detectors measurements can be used for their own calibration. The electrical trigger sampling stage calibration and the PLL phase calibration are coupled and changing Roman Pot PLL settings affects the input sampling stage. It is hard to distinguish two cases:

- a decaying beam structure (Figure 4.13) seen by the input stage calibration histogram is present due to a wrong clock phase setting with respect to the passing bunches or
- it is present due to a wrong sampling of the trigger signal in FPGA.

It is not a trivial task to distinguish those two processes but it is essential for proper detector and trigger system calibrations. It can be achieved as follows. The input sampling stage can be set to sample in four steps of 7.5 ns and the detector PLL clock phase shift can be programmed in 1 ns steps. It is used to measure four trigger bit histograms for all four possible sampling stage settings for all detectors while repeating this measurement for all the possible PLL phase shift setting in 1 ns steps. Once measured, calibration data were analyzed by a dedicated program

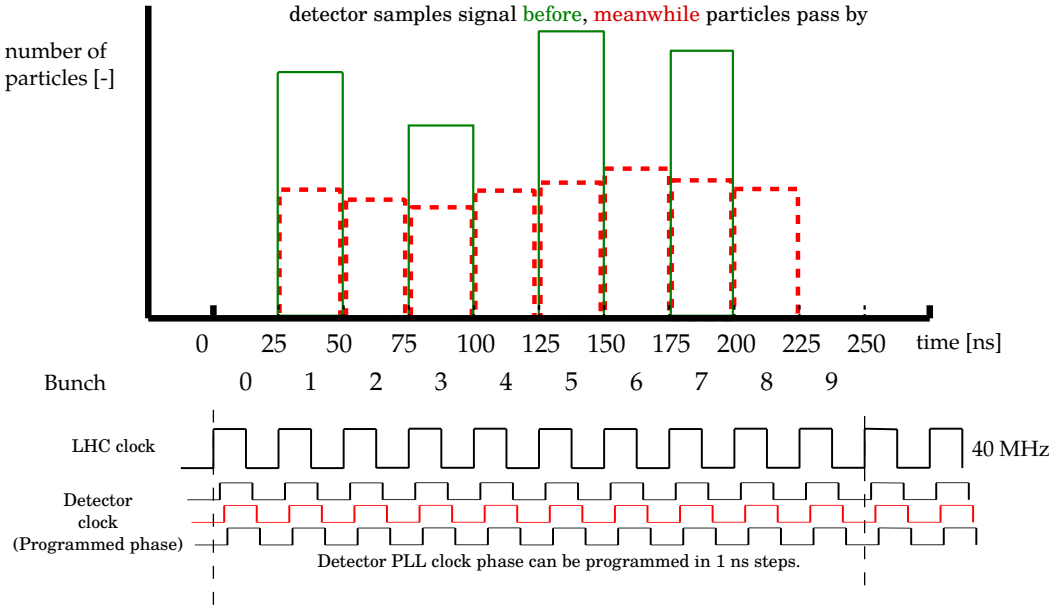


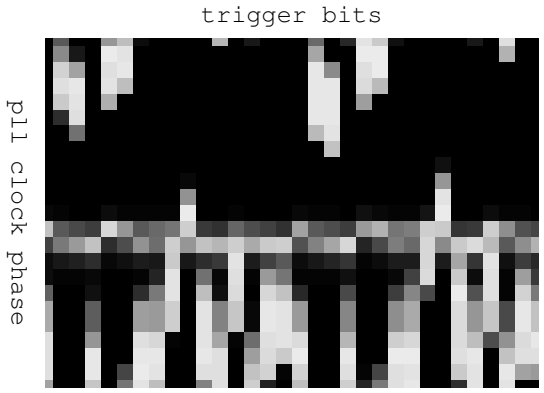
Figure 4.13: PLL phase shift tuning principle. The electrical trigger bit histogram is also used to fine tune the Roman Pot detector PLL phase shift. The vertical axis represents bunch slots and the horizontal axis represents number of trigger bits received over an integration time period. Normally, if there is a spacing between individual bunches then each bunch should be observed as a sharp peak in the trigger bits histogram. If the clock phase is such that a detector samples its analog input while a bunch pass by, sampled data jitter between two neighboring buffer memory slots and histogram peaks decay. Changing the PLL's output clock phase allows us to measure a relative phase between the LHC clock and a moment when bunches pass by detectors. Then we can select correct PLL value.

that looks at individual bit histograms and searches for peaks (from bunch 0 to 64, from left to right). If a peak is detected then the consecutive value corresponding to next bunch slot in the histogram is divided by the value of the peak bunch slot bin. This is done for every peak detected in the histogram. An average of a sum of all results is made for all peaks for individual trigger bit (this means each trigger bit is represented by a single average value). If peaks are decaying the average value is close to one or higher. Otherwise the average value is close to 0. Figure 4.14 shows two dimensional graphs for a single Roman Pot (one graph for each input stage phase settings). The horizontal axis represents Roman Pot PLL clock phase from -180° to 180°. The vertical axis represents 32 trigger bits and corresponding average values. In the graphs a, b, c and d, there are two patterns visible due to the bunch decaying:

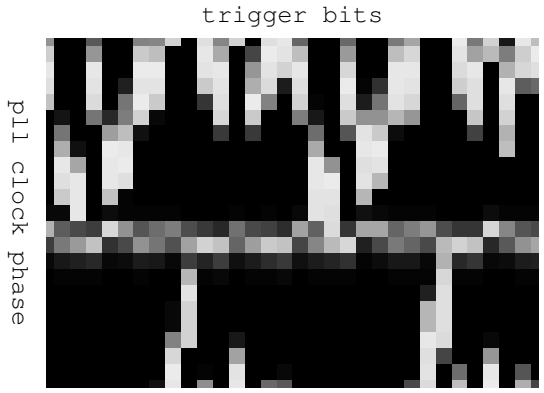
One process is dependent both on the PLL clock phase and sampling stage configuration, thus it changes with respect to the programmed sampling stage phase. This process is also different for each trigger bit due to the fact that the propagation delay is different for each line and creates zig-zag patterns in the graphs. This pattern is created on the FPGA level.

The other process is related only to the PLL phase and it happens for all channels for the same PLL clock phase configuration (the pattern is created on the detector level). It manifests the straight horizontal line at the same position in all four graphs. This line identifies such PLL configuration that detectors signals start to jitter between two clock cycles.

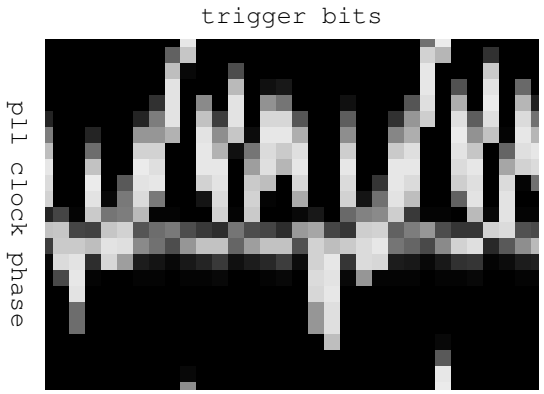
To verify this hypothesis, the author has done the sampling stage calibration for every



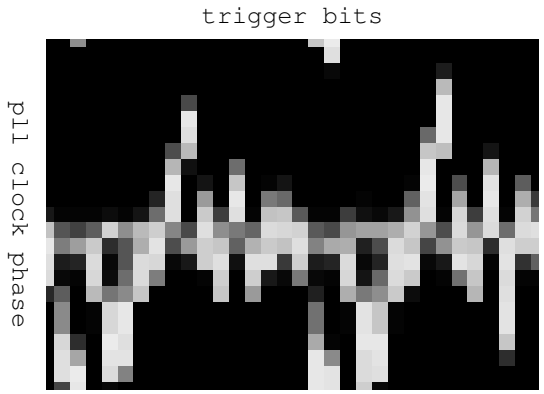
(a) Electrical trigger input sampling stage phase is set to 0°.



(b) Electrical trigger input sampling stage phase is set to 90°.



(c) Electrical trigger input sampling stage phase is set to 180°.



(d) Electrical trigger input sampling stage phase is set to 270°.

Figure 4.14: Input stage histograms analysis for different PLL sampling stage settings for a single RP. For each possible settings of the Roman Pot detector PLL, four histograms (subfigures a, b, c and d) were made: one for each electrical trigger sampling stage phase setting. In each histogram, an analysis program searched for peaks and gives a result value around 1 (white color) for decayed peaks and close to 0 (blacks) for histograms containing sharp peaks. The result for each detector PLL settings is presented in these 2D bitmap graphs. The vertical axis represents detector PLL clock phase and the horizontal axis represents trigger bit channel. There are two different processes responsible for the bunch decaying in the histogram: the PLL settings represented by a straight horizontal line with constant position for all four histograms and an electrical trigger sampling stage aliasing represented by a zig-zag structure which is shifting according to the selected input sampling stage phase.

possible PLL settings (to eliminate the input sampling stage aliasing) and the result is shown in Figure 4.15: the zig-zag structure is eliminated. All the Roman Pot detector PLLs have been calibrated using this method to optimize the clock phase for it's correct functionality and to achieve the one-clock-cycle time resolution.

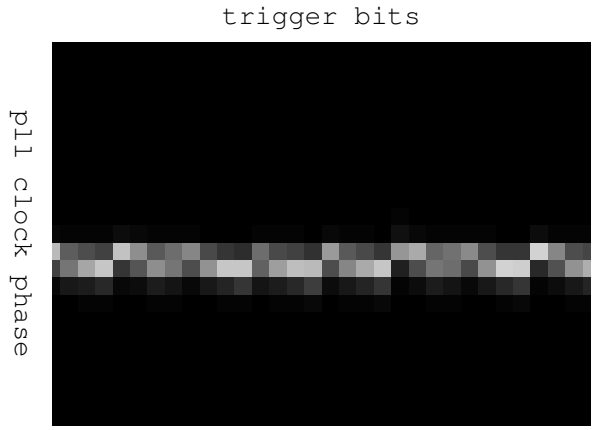
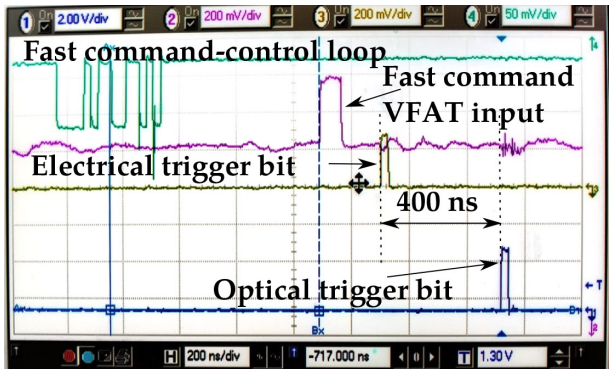


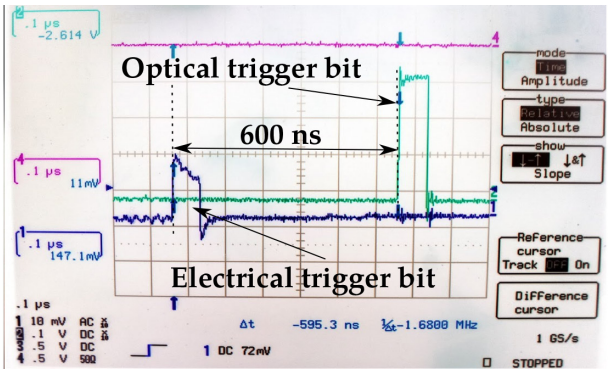
Figure 4.15: Bunch decaying for different Roman Pot PLL phase settings (single RP). This measurement is done with the calibrated sampling stage (compare with Figure 4.14). The white line identifies the value of the PLL phase when the Roman Pot detector samples in the middle of the filled bucket.

4.5 Comparison of the optical and electrical signal propagation delays

To compare performances of the electrical and optical trigger path, a relative latency measurements between the data coming via each path were done in a laboratory. Later on, the same measurements were performed with the final installation in LHC. Thus, we can distinguish between a delay produced by electronic devices and by cabling. Of course, the most important is to know the value of the sum of all the delays and time difference gained by using an electrical transmission lines.



(a) Laboratory test setup with short transmission line. The delay is mainly caused by the serialization and de-serialization of transmitted data.



(b) Final installation in LHC with almost 300 m long transmission lines contribution of additional 200 ns of a delay difference.

Figure 4.16: Electrical vs. Optical trigger signal delay measurements. The measurements show the difference in the propagation delay between the electrical and the optical signal

The lab measurement was done by sending calibration pulses to a VFAT that stimulated it's output trigger bit signals measured at the output of the VFAT chip and at the end of optical and electrical line. The result is shown in Figure 4.16(a). We can see that the delay difference between the signals, that are received via the electrical and optical line is about 400 ns. That means that we gain about 300 ns due to the fact that the optical signal is propagated trough the FPGA and the firmware adds about 100 ns extra delay. This is mainly because the optical line has to serialize and later on de-serialize a parallel trigger bit bus for the Gigabit Optical Link and the electronics contains several unavoidable buffers. Thanks to this measurement we know the relative (optical vs. electrical link) and absolute (with respect to the output trigger bit) delay of the signals.

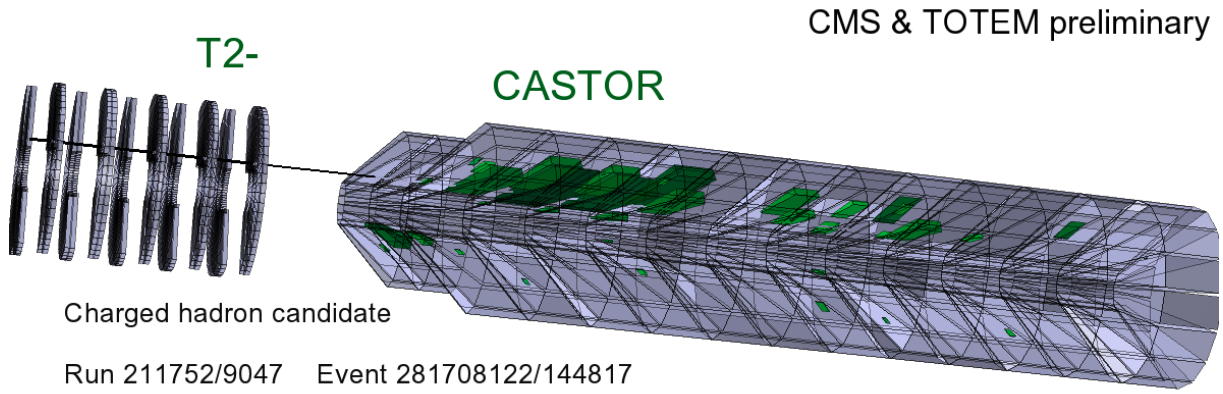
Inside the tunnel, the author measured only the relative difference between those two bits as shown in Figure 4.16(b). A different propagation delay in the optical fiber and the electrical wires added about 200 ns to the electronics delay.

What is important is that the electrical signal is compliant with the official CMS trigger system requirements and can be used to trigger the CMS experiment.

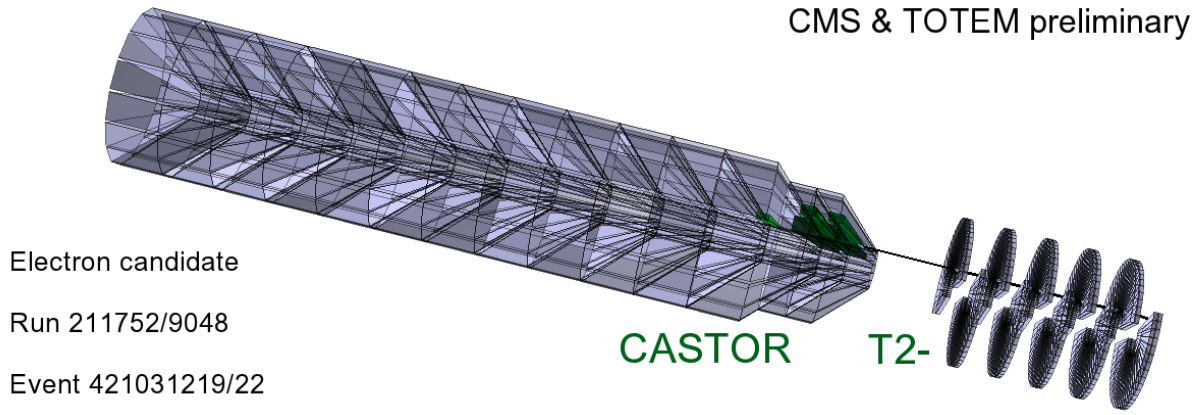
4.6 TOTEM CMS common operation

During the February 2013, the bidirectional trigger exchange (see Section 3.4) between the TOTEM and CMS experiments was tested and used for measurements. The common measurements data are still being analyzed, however, the concept of the common operation has been already proven.

The author would like to demonstrate the combined trigger system functionality and it's importance for both experiments by showing combined data that was measured by the T2 (TOTEM) and CASTOR (the Centauro And Strange Object Research, CMS) detectors. CASTOR is a very forward electromagnetic and hadronic calorimeter of CMS located on minus side behind T2, 14.37 m from the interaction point 5, covering pseudorapidity range $5.2 < \eta < 6.6$. [38].



(a) Charged hadron particle candidate.



(b) Electron particle candidate

Figure 4.17: Particles as seen by TOTEM-T2 (track) and CMS-CASTOR (energy) detectors.

Figure 4.17 shows two particles as seen by the TOTEM and CMS apparatus. T2 provides the tracking information and CASTOR measures the energy of the particle. It shows how a combining TOTEM and CMS data extends the physics measurement capabilities for both experiments.

In case of Figure 4.18, the TOTEM T2 detector was used as a trigger source. The trigger signal was propagated to CMS and used to trigger the CASTOR detector. Events with only one

track in T2 minus and only one sector active in CASTOR with an electromagnetic energy above 10 GeV (while the other sectors below the noise level cut at 5 GeV) were selected. The track information from T2 was used to extrapolate CASTOR enter point (see Figure 4.17) represent a position where particles hit CASTOR. The color reflect the CASTOR sectors where the measured electromagnetic energy was above the threshold. The black solid lines represent the CASTOR geometry. Most of the T2 tracks are occupying correct CASTOR sectors.

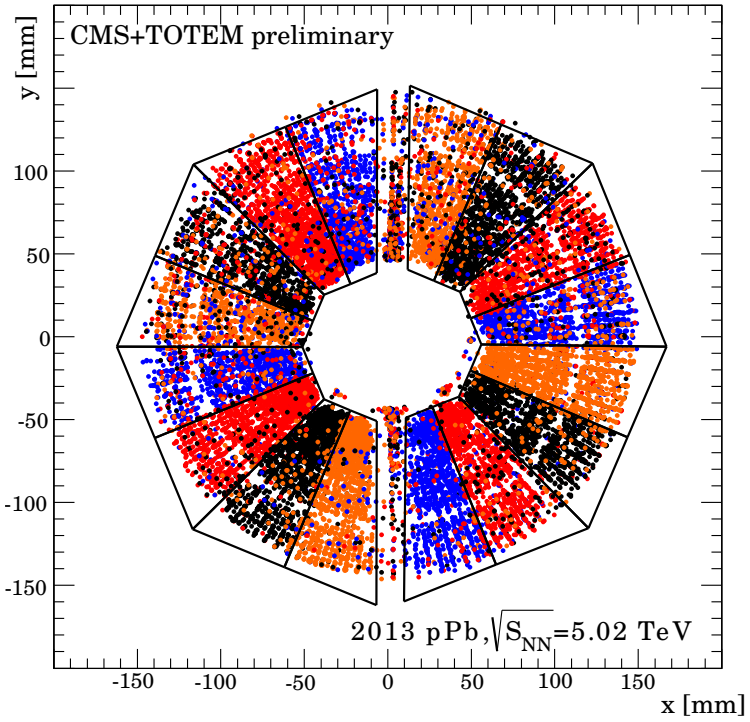


Figure 4.18: Correlation of the tracking data measured by the TOTEM-T2 detector and deposed energy measured by CMS-CASTOR.

The functional TOTEM and CMS trigger exchange had proven the original idea to combine data from both experiments. This created good background for the future collaboration of the TOTEM and CMS experiments.

Author's contribution to the TOTEM experiment

The author joined the TOTEM collaboration as a member of the Institute of Physics, AS CR v. v. i. in 2008 and started to work on TOTEM electronics as a test engineer. His work on the TOTEM trigger system started during the winter 2009/2010. In that time, the T2 and Roman Pots detectors were installed and also LHC started its operation. At that time the trigger system firmware was not ready yet. It was necessary to develop the trigger system and its functionality accordingly to the TOTEM's evolving physics program in parallel to physics measurements.

Author's first responsibility was to develop the OptoRX firmware for triggering T2 and the Roman Pot detectors including the logic, data synchronization, processing and development of monitoring capabilities described in Section 3.1. This OptoRX firmware was used during the physics measurements from the year 2010 to 2012.

In parallel to the OptoRX firmware development, the author worked on an implementation of the Electrical trigger transmission line for the Roman Pot detectors. This work included hardware and firmware development described in Section 3.2 and 3.3. The Electrical Trigger was installed by the author and a group of technicians during the LHC "winter shut down" period at the beginning of the year 2012. After the installation and calibration, the Electrical trigger was commissioned and fully integrated into the TOTEM trigger system replacing the Optical trigger of the Roman Pots. The main reason for the Electrical trigger installation was to reduce the trigger system latency and achieve the possibility of the TOTEM/CMS trigger exchange for common measurements.

The author also presented his work at the following conferences:

- Applied electronics, Pilsen, Czech Republic (September, 2013) [23].
- 14th ICATPP Conference on Astroparticle, Particle, Space Physics and Detectors for Physics Applications 2013, Como, Italy (September, 2013) [24].

From the summer 2012 up to February 2013, the TOTEM/CMS common measurements have been performed (Section 4.6).

The effort of both collaborations to perform common physics measurements and its success created excellent background for the future collaboration. In January 2014, the memorandum of understanding about the future cooperation between TOTEM and CMS have been signed by both collaborations. The author is proud that he could partially contribute to this achievement by his work on the TOTEM trigger system.

The TOTEM Trigger System have been used over the years for various physics measurement and based on these measurements the following physics papers have been published:

1. Proton-proton elastic scattering at the LHC energy of $\sqrt{s} = 7$ TeV [26]
2. First measurement of the total proton-proton cross section at the LHC energy of $\sqrt{s} = 7$ TeV [27]
3. Measurement of the forward charged-particle pseudorapidity density in pp collisions at $\sqrt{s} = 7$ TeV with the TOTEM experiment [28]
4. Measurement of proton-proton elastic scattering and total cross-section at $\sqrt{s} = 7$ TeV [29]
5. Measurement of proton-proton inelastic scattering cross-section at $\sqrt{s} = 7$ TeV [30]
6. Luminosity-independent measurements of total, elastic and inelastic cross-sections at $\sqrt{s} = 7$ TeV [31]
7. A luminosity-independent measurement of the proton-proton total cross-section at $\sqrt{s} = 8$ TeV [32]
8. Double diffractive cross-section measurement in the forward region at LHC [33].
9. Measurement of the forward charged particle pseudorapidity density in pp collisions at $\sqrt{(}s) = 8\,\text{TeV}$ [35]

The TOTEM experiment physics program is dynamic and evolves in time. This also implies future changes in the TOTEM trigger system. The future collaboration between the TOTEM and CMS experiments will require extensive trigger upgrade to cover all the future requirements of both experiments.

Conclusions

This thesis concludes the work of the author on critical parts (hardware, firmware) of the trigger system of the TOTEM experiment. Since the requirements and specifications related to the trigger system components evolved together with an overall performance of LHC, it was necessary to upgrade those trigger components accordingly; also new challenges appeared. Each firmware contains a wide number of monitoring and logic blocks related to various trigger schemes. It required the development of tools and methods for control, diagnostics and calibration.

The firmware for processing optically transmitted trigger bits from the T2 and Roman Pot detectors was the author's first task and has been used as an active part of the TOTEM experiment since the year 2011.

As the consequence of the agreement between the TOTEM and CMS experiments to perform common physics measurements, their independent trigger systems had to be combined (recorded data are combined offline). The idea behind the common operation was that both experiments cover different angle acceptance regions. Unfortunately, the size of local buffers inside CMS is limited and it was not possible to provide a trigger from TOTEM to CMS on time. It was inevitable to reduce the transmission line latency between Roman Pots and the final part of the TOTEM trigger electronics. For this purpose, the author designed and installed new transmission line based on special metallic wires which allow achieving a lower propagation delay compared to optical fibers. The transmission line also uses parallel configuration, therefor there is no need to serialize and de-serialize transmitted data. These two factors reduced the original latency by 600 ns which was sufficient to provide the TOTEM trigger to CMS on time and allowed the successful common operation of the TOTEM and CMS experiments in the years 2012 and 2013. The work on this transmission line concluded the design of electronics devices and development of firmware for the FPGA chips.

The combined data from both experiments are unique for studying to study diffractive phenomena where protons create a central production of particles (the forward protons are measured in TOTEM and central particles in CMS).

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List of abbreviations

ASIC *Application Specific Integrated Circuit.* An integrated circuit customized for the particular use.

ATLAS *A Toroidal LHC Apparatus.* An LHC experiment.

B1, B2 *Beam 1, Beam 2.* Designations for the LHC beams.

BT *Bottom.* It is used to determine a detector position.

CASTOR *Centauro And Strange Object Research.* A CMS sub-detector.

CC *Coincidence Chip.* A CERN ASIC chip developed for trigger systems.

CCS *Controller Card for CMS.* A common Front-End Controller card for the CMS detector electronics.

CCU *Communication and Control Unit.* A CERN ASIC chip for an embedded slow control

CERN *Conseil Europeénne pour la Recherche Nucléaire.* European Organization for Nuclear Research in Geneva, Switzerland.

CMOS *Complementary Metal Oxide Semiconductor.* A semiconductor technology.

CMS *Compact Muon Solenoid Detector.* An LHC experiment.

CNGS *CERN Neutrinos to Gran Sasso.* An experiment devoted to neutrino studies.

CSC *Cathode Strip Chambers.* a type of gaseous ionization detector.

DAQ *Data Acquisition.* System responsible for a data readout.

DCU *Detector Control Unit.*an ASIC chip developed for a monitoring system for the CMS Tracker used by TOTEM.

DOH *Digital Opto-Hybrid.*

ECAL *Electromagnetic Callorimeter.* A CMS sub-detector.

EDA *Electronics Design Archive.* A CERN electronics design database.

EDMS *Engineering and Equipment Data Management Service.* A CERN document, equipment and maintenance database.

ELT *Electrical trigger.*

FPGA *Field-Programmable Gate Array.* A type of the integrated circuit.

FR *Far.* It is used to determine a detector position.

FSM *Final State Machine.* Mathematical model of computation used for sequential logic.

GEM *Gas Electron Multiplier.* a type of gaseous ionization detector.

GOH *Gigabit Optical Hybrid.* A transmission module based on GOL chip

GOL *Gigabit Optical Link.* An ASIC chip developed by CERN for the data transmission over the optical fiber.

HCAL *Hadronic Callorimeter.* A CMS sub-detector.

HM *High multiplicity (cut).* Refers to the desired number of active trigger bits that should generate a trigger signal.

HR *Horizontal.* It is used to determine a detector position.

IP *Interaction Point.* An intersection point where two beams collide (It is also used as a designation for the whole infrastructure surrounding the intersection point).

IP5 *Interaction Point 5.* LHC beams intersection point shared with the TOTEM and CMS experiments.

L1 *Level One.* The first level of the trigger system. Large systems can contain several levels of trigger. For example CMS has hardware based L1 trigger activating DAQ and software based Level Two trigger that filters received data before a storage. TOTEM has only L1 trigger.

L1SA *Level One Special Accept.* A subset CMS L1 trigger signal.

LHC *Large Hadron Collider.* The world largest particle accelerator.

LINAC *Linear accelerator.* A CERN particle accelerator.

LONEG *Level One Generator.* TOTFed mezzanine card for the TOTEM trigger system.

LTC *Local Trigger Control.* The LTC allows to control detectors.

LUT *Look Up Table.* An associative array.

LVDM *Multi-point LVDS.*

LVDS *Low-voltage differential signaling.* An electrical digital signaling standard.

MeV, GeV, TeV *Mega electron Volt, Giga electron Volt, Tera electron Volt.* Units of energy used in high energy physics.

mFEC *mezzanine Front End Controller.* A controller board developed for CMS which is used by TOTEM.

NR *Near.* It is used to determine a detector position.

OPTORx *Optical Receiver.* An TOTFed mezzanine card for an optical signal reception.

PLL *Phase Loop Lock.* An electronics device for various applications. In TOTEM, it is used for a clock optimization.

PS *Proton Synchrotron.* CERN particle accelerator.

PSB *Proton Synchrotron Booster.* A CERN particle accelerator.

RC *Resistor-Capacitor.* An resistor-capacitor circuit.

RF *Radio Frequency*

RL *Resistor-Inductor.* An resistor-inductor circuit.

RO *Read Only.*

RP *Roman Pot.* A detector of the TOTEM experiment.

RW *Read/Write.*

SPS *Super Proton Synchrotron.* A CERN particle accelerator.

SRAM *Static Random Access Memory.*

T1 *Telescope 1.* A detector of the TOTEM experiment.

T2 *Telescope 2.* A detector of the TOTEM experiment.

TOTEM *TOTal Elastic and diffractive cross section Measurement. An LHC experiment.*

TOTFed *TOTEM Front End.* VME board developed for TOTEM and CMS used trigger and DAQ electronics. Mostly used as a carrier tor mezzanine cards.

TP *Top.* It is used to determine a detector position.

TTC *Timing, Trigger and Control Systems for the LHC.* A system for the clock, fast L1 trigger signal, and slow control distribution.

TTCrx *A Timing, Trigger and Control Receiver.* An ASIC chip for LHC Detectors

USC *Underground Service Cavern.* Underground cavern of CMS shielded from radiation dedicated for CMS and TOTEM infrastructure.

VFAT *Very Forward Atlas and TOTEM.* A TOTEM and ATLAS read out chip for sensors.

VME *Versa Module Europa bus.* Computer bus standard.

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