Design and Optimisation of Active Power Factor Correctors

Návrh a optimalizace aktivních korektorů účiníku

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I would like to dedicate this thesis to my loving family and fiancée Dominika …

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in a part for consideration of any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements. The doctoral thesis was established by the Latex template for Cambridge University Engineering Department made by Krishna Kumar [16].

Ing. Jan Moldaschl
March 2018

Acknowledgements

When I was at the decision how to continue after my master degree, the continuing on the PhD program was clear choice. The investigation of the power factor correctors was began during the preparation for the first examined learning course which was dedicated to switch mode power supplies. I designed several prototypes of the active power factor correctors which are not a part of this thesis. These prototypes were used for an investigation of the basic principles and verification design procedures.

The next impulse of the research was launched after learning course related to the special power semiconductor components. I focused on the new materials for power electronics as GaN and especially SiC. I was excited by SiC Schottky Barrier diodes which are an ideal choice for APFC. They combine advantages of the ultrafast and Schottky diodes, they are suited for a high speed switching and high voltage conditions. Therefore one chapter of this thesis was devoted to the investigation of the features and evaluation of different diodes.

The writing a first concept including basic principles and theoretical background bring me new ideas and challenges. In 2015, I had a honor to study in the Brunel University London. During this several months stay I met a professor Mohamed Darwish who fulfilled the role of mentor at the university. I passed two power electronic courses which gave me new viewing angle. I investigated digital controllers and organized my theoretical background.

When I came back to my home university, I started with developing of the prototypes which are described in this dissertation. During this period I was experienced by theoretical and practical aspects of the development stage. Very beneficial part was a measurement of the conductive emission. The investigation of the potential improvements leads to adjusting of the prototypes .

The power management was implemented by the Discovery kit as a next stage. Finally, features of the prototypes were measured by performance tests, EMC and thermal measurement.

Then I continued with a written part. I added chapters which deeply explain the process of the design of the prototypes and measurement.

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Abstract

A massive using of switched mode power supplies causes a high harmonic pollution of the line current. The distortion is significant due to a non-linear behaviour of the rectifying diodes and bulky input capacitor of SMPSs. The behaviour causes short spikes of the line current, which produces as a consequence low power factor. Therefore, the power factor correction is gaining importance in the recent two decades. Using power factor correctors are very likely to happen in the future due to a tightening of the international standards. This dissertation is devoted to design, optimization, and the evaluation of active power factor correctors.

Generally, a principle of correctors lies in the storing and releasing of the excessive energy during line cycles. If the load has a pure resistive character, the output power will be a constant. Contrary to this, the input power oscillates with double frequency from zero to maximum power. An average value of the instantaneous input power equals the output power. Passive power factor correctors are able to absorb the excessive energy and release it at a suitable time.

Active power factor correctors use a similar principle but they are able to compensate a full range of the input voltage due to the features of the boost converter. Thanks to these features the power factor can be corrected up to 0.999. Unfortunately, the high switching frequencies lead to an enhancement of the electromagnetic emission. Active correctors reduce the harmonic pollution at the cost of the increasing conductive interference. However, interferences shall be reduced by additional EMI filter.

This doctoral thesis explores several types of the correctors for the evaluation purposes. Each prototype is characterized by different features. The main targets of the work are the comprehensive overview of the topologies and control techniques including methods for improvements of the correctors. The improvements include SiC Schottky diode, frequency dithering, and power management. The evaluation of the prototypes gives valuable information about the performance and costs. All prototypes are compared with each other and their benefits are summed up in the conclusion.

Keywords

Power Factor Correction, Power Factor Correctors, Active Power Factor Correctors, Passive Power Factor Correctors, Interleaved Power Factor Correctors, Power Management for Interleaved Correctors, Power Management for Multiphase Correctors, SiC Schottky diodes, Power Factor, Frequency Dithering, Bridgeless Power Factor Corrector, Boost Corrector, PFC, APFC, Flat Profile Power Factor Corrector, Multiphase Power Factor Corrector.

Abstrakt

V současné době způsobuje masivní používání spínaných zdrojů harmonické znečištění síťového proudu. Zkreslení je významné z důvodu nelineárního chování usměrňovacích diod a velkého filtračního kondenzátoru na vstupu spínaného zdroje. Toto chování způsobuje úzké impulsy síťového proudu, které jsou příčinou nízkého účiníku. Proto se korekce účiníku stává důležitou především v posledních desetiletích. Lze předpokládat, že korektory účiníku budou v budoucnu využívány velmi často, kvůli zpřísňování mezinárodních norem. Tato dizertační práce se věnuje návrhu, optimalizaci a hodnocení aktivních korektorů účiníku. Obecně princip korektoru spočívá v ukládání a uvolňování nadměrné energie během cyklů sítě.

Pokud má zátěž čistě rezistivní charakter, výstupní výkon bude konstantní. Naopak vstupní výkon osciluje s dvojnásobnou frekvencí sítě od nuly do maxima. Platí, že průměrná hodnota okamžitého vstupního výkonu se rovná hodnotě výstupního výkonu. Pasivní korektory účiníku jsou schopné absorbovat nadbytečnou energii a uvolnit ji ve správný čas.

Aktivní korektory účiníku využívají podobný princip, ale jsou schopné kompenzovat účiník v celém rozsahu vstupního napětí kvůli vlastnostem Boost konvertoru. Díky těmto vlastnostem může být účiník korigován až na hodnotu 0,999. Bohužel, vysoké spínací frekvence vedou k nárůstu emisí elektromagnetického pole. Aktivní korektory účiníku snížují úroveň harmonického znečištění za cenu nárůstu elektromagnetických interferencí.

Nicméně interference mohou být redukovány pomocí dodatečného EMI filtru. Dizertační práce zkoumá několik typů korektorů pro účely evaluace. Každý prototyp je charakterizován různými vlastnostmi. Hlavním cílem práce je komplexní přehled topologií a řídících technik zahrnujících metody pro vylepšení korektorů. Tato vylepšení zahrnují SiC Schottkyho diody, rozmítání spínací frekvence a řízení výkonu. Evaluace prototypů dává hodnotnou informaci

o výkonosti a nákladech. Všechny prototypy jsou porovnány mezi sebou a přínosy jsou shrnuty v závěru práce.

Klíčová slova

Korekce účiníku, korektory účiníku, aktivní korektory účiníku, pasivní korektory účiníku, korektory s prokládáním pracovních cyklů, řízení výkonu pro korektory s prokládáním pracovních cyklů, řízení výkonu pro vícefázové korektory, SiC Schottkyho diody, účiník, rozmítání spínací frekvence, bezmůstkový korektor účiníku, Boost korektor, PFC, APFC, korektor účiníku s nízkým profilem, vícefázový korektor účiníku.

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Glossary

AC Alternately current. 47, 55, 84, 109, 146

ADC Analog-to-digital converter. 44, 120, 162, 167, 191, 192, 193, 195, 197, 199, 212

APFC Active Power Factor Corrector. vii, 1, 6, 9, 10, 11, 12, 13, 14, 15, 17, 19, 35, 36, 37, 42, 44, 48, 51, 54, 70, 81, 83, 86, 89, 100, 101, 115, 134, 147, 160, 189, 191, 211, 212

CCM Continuous conduction mode. 2, 11, 15, 17, 37, 38, 55, 81, 83, 86, 89, 107, 165, 177, 201

CrM Critical conduction mode. xiii, xiv, 11, 15, 17, 18, 22, 23, 24, 25, 38, 39, 108, 128

DAC Digital to Analog Converter. 197

DC/DC DC/DC converter. 11

DCM Discontinuous Conduction Mode. 11, 15, 17, 18, 106, 201

DUT Device Under Test. 53, 54

EADC Error Analog-to-Digital Converter. 195, 197

EDR Enhanced Dynamic Response. 63, 70

EMC Electromagnetic compatibility. 53, 211

EMI Electromagnetic interference. 1, 13, 15, 29, 43, 53, 64, 81, 89, 98, 118, 128, 134, 157, 158, 177, 182, 189, 200, 201

FCCrM Frequency clamped critical conduction mode. 1, 2, 15, 37, 38, 39, 103

FPGA Field Programmable Gate Array. 212

GPIO General Purpose Input Output. 199

GUI Graphical User Interface. 199

IGBT Isolated Gate Bipolar Transistor. 64, 98

LCD Liquid Crystal Display. 37, 42

LISN Line Impedance Stabilization Network. 53

LLC Resonant Converter. 44, 45

LTCC Low Temperature Co-fired Ceramics. 82

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 31, 36, 54, 58, 64, 98, 118, 128, 162, 177, 182, 199, 201

NTB Notebook. 11, 13, 42

NTC Negative Temperature Coefficient. 47, 54, 134, 208

PCB Printed Circuit Board. 74, 118, 157, 163, 165, 211

PF Power Factor. 2, 5, 11, 13, 35, 43, 51, 94, 115, 200, 202, 207

PFC Power factor correction or corrector. xvii, 1, 2, 117, 120, 167, 191, 192, 195, 198, 199, 200, 202, 212

PIN diode with a wide, undopped intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. 81, 82, 83

PMbus Power management bus. 44, 191, 199

POL Point-of-Load. 11

PWM Pulse Width Modulation. 13, 21, 44, 63, 66, 68, 106, 111, 112, 113, 144, 150, 159, 193, 195, 198, 199, 212

RISC Reduced Instruction Set Computing. 44

RMS Root Mean Square. 4, 55, 58, 60, 104, 109, 119, 142, 148, 167, 191

SBD Schottky Barrier Diode. 81, 83

SiC Silicon Carbide. vii, 15, 38, 59, 82, 83, 84, 86, 89

SMPS Switched Mode Power Supply. ix, 1, 5, 8, 9, 19, 35, 89

THD Total harmonic distortion. 15, 51, 69, 201

USB Universal Serial Bus. 199

UVLO Under Voltage Lock Out. 64

VAC Alternately voltage. 10, 13

VDC Direct voltage. 10, 13, 48, 145

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Chapter 1

Analysis of Current Status of Issues Dealt in Dissertation

1.1 Introduction

This doctoral thesis was created as a consequence of the expansion of switch mode power supplies for powering of consumer electronics and computers. Due to a number of the connected SMPS to the mains, it is necessary to reduce a harmonic pollution. The advantage of SMPSs is high efficiency but the rectifier and capacitor at the input take an active and reactive power. The reactive power is not involved in a conversion of the energy. A ratio between active and reactive power is determined by the Power Factor number. The power factor should be improved by an using of passive or active power factor correctors.

Passive PFCs are low-pass filters which are located at the input of conventional switch mode power supplies. They have a very low cut off frequency therefore these filters are relatively bulky and heavy. The passive filters do not have an adjustable output. They are not able to achieve the power factor greater than 0.9. They have a high total harmonic distortion and their dynamic response is slow. An optimization of the design is very difficult.

Active PFCs use high-frequency shaping techniques. Basically, each topology can be used for active PFCs. The boost corrector is the most common converter topology since this topology has a minimum number of components and grounded power switch. Active Power Factor Correctors are able to correct the power factor up to 0.999. Unfortunately, the using of APFCs leads to grow the conduction noise. An EMI filter shall be used for a limitation of the conduction noise which affects the line voltage.

Single phase boost correctors represent an affordable and easy to implement solution for a wide range of devices. The produces offer complex solutions for interleaved and bridgeless

topologies which are suitable for wider output power ranges. The typical commercial solutions use the single boost corrector with continuous conduction mode for medium power levels. The power levels below three hundred watts level take advantages of the boost correctors with FCCrM.

This doctoral thesis aims to give a description of the theoretical background of the PF correction. It includes also an overview of the control techniques and state of the art of the correctors. The main target is focused on the design and improvements of the active power factor correctors. The requirements are design and realization of three different prototypes. The first prototype is based on the single phase corrector with CCM operation and $500W$ output power at $230V$. The second prototype is characterized by the FCCrM and interleaved operation. The maximal output power at $230V$ input power is limited to $600W$. The corrector implies an unique mechanical construction and power management. The third prototype requirements define a corrector with $1kW$ output power at $230V$. It is designed as interleaved corrector with the CCM current mode and additional power management. All prototypes shall comply ČSN EN 61000-6-4 and ČSN EN 61000-3-2 standards.

This thesis gives a comprehensive account of a design process. It includes a component selection issue, internal controller blocks description, and perspective ways of the improvements. There are expressed methods for feature improvements of the correctors as boost diode replacement, flat profile corrector, frequency dithering, and power management feature for interleaved correctors. The boost diode replacement analyses a performance of the different types of the boost diodes. They are investigated at two switching frequencies. It presents an evaluation and discussion about appropriateness to the particular application. The flat profile corrector considers a new hardware solution with several advantages. The construction takes advantage of the embedded components which are installed into printed circuit board. The height of the corrector thanks to this solution does not exceed $22mm$. The planar inductor was also applied due to reduction of the height of the corrector. The frequency dithering deals with a opportunity of electromagnetic emission improvements in case of no layout adjustment. The focus is devoted to the switching frequency modulation. The part dedicated to the power management feature concentrates on the enabling and disabling of the interleaved corrector branches. The solution provides performance improvements for correctors worked under variable operation conditions. Last but not least part of this thesis is an evaluation and comparison of the prototypes with a commercial solution which is based on the $UCD3138$ PFC kit.

The remainder of this doctoral thesis is organized as follows. The first part explains the theoretical background. It includes mathematical apparatus and physical principle of the correction. Following parts describe a current state of the development in a field of the

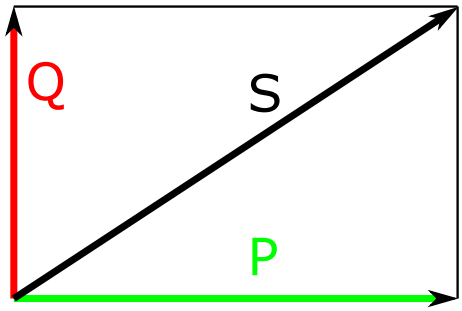


Fig. 1.1 Relations in linear systems.

power factor correctors, their control methods, and current conduction modes. The third part contains a description of the remarkable innovative topologies and features of the controllers. The part describes also several pitfalls which is typical for these topologies. The next part includes a design process of the prototypes, which contains one single phase corrector and two interleaved correctors. The part covers the corrector improvements. The measurement verifies a correctness of the hypothesis. The last part of this thesis includes experimental results, evaluation, discussion, and conclusion.

1.2 Definition of Power Factor and Total Harmonic Distortion

The power factor gives information about the distortion of a line voltage, a line current and a phase shift between them. Simultaneously, it gives information about the real power utilization in the power system. The figure 1.1 illustrates relations between an apparent, a real and a reactive power in linear systems. The figure 1.2 outlines relations between an apparent, real, displacement reactive power, and distortion reactive power in non-linear systems [39], [33].

$$PF = \frac{P}{S}[-] \tag{1.1}$$

$$PF = \frac{V_{RMS} \cdot I_{RMS} \cdot \cos\theta}{V_{RMS} \cdot I_{RMS}}[-] \tag{1.2}$$

Where I_{RMS} and V_{RMS} are line voltage and line current, θ is phase shift between them. Therefore the power factor in linear systems equals to a cosine of the phase shift. However, in power electronic systems due to non-linear behaviour of the power devices the power factor representation is not valid. The non-linear loads cause a typical distorted line current. The figure 1.3 illustrates this situation. A line voltage and a current are distorted therefore it

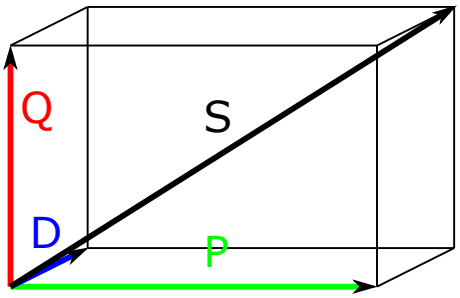


Fig. 1.2 Relations in non-linear systems.

shall be used Fourier representation of them [39], [33].

$$i(t) = I_{DC} + \sum_{k=1}^{\infty} I_{mn} \sin(n\omega t + \theta) \tag{1.3}$$

$$i(t) = I_{DC} + I_{m1} \sum_{k=2}^{\infty} I_{mn} \sin(n\omega t + \theta) \tag{1.4}$$

$$v(t) = V_{DC} + \sum_{k=1}^{\infty} V_{mn} \sin(n\omega t + \theta) \tag{1.5}$$

$$v(t) = V_{DC} + V_{m1} \sum_{k=2}^{\infty} V_{mn} \sin(n\omega t + \theta) \tag{1.6}$$

Inserting (1.4) [39] and (1.6) [39] into a definition of the power factor (1.2 [39]), it is obtained a representation of the power factor for non-linear systems.

$$PF = \frac{\sum_{k=1}^{\infty} V_{RMS,n} \cdot I_{RMS,n} \sin\theta_n}{V_{RMS} \cdot I_{RMS}} = \frac{\sum_{k=1}^{\infty} V_{RMS,n} \cdot I_{RMS,n} \sin\theta_n}{\sqrt{\sum_{k=1}^{\infty} V_{RMS,n}^2} \cdot \sqrt{\sum_{k=1}^{\infty} I_{RMS,n}^2}} \tag{1.7}$$

Where $V_{RMS,n}$ and $I_{RMS,n}$ are RMS values of the n^{th} harmonics of the voltage and current and θ is phase shift between n^{th} harmonics of the voltage and current. Generally, the most of power electronic systems have their input voltage from stable line voltage sources. Consequently, the equations can be written as ((1.8) and (1.9)) [39], assuming that the line voltage is a pure sinus and the current is distorted (non-sinusoidal).

$$v(t) = V \sin\omega t \tag{1.8}$$

$$i(t) = \sum_{k=1}^{\infty} I_{mn} \sin(n\omega t + \theta) \tag{1.9}$$

In the general cases the real power equals to:

$$P = \sqrt{P_{DC}^2 + P_1^2 + P_2^2 + P_3^2 + ...} \tag{1.10}$$

Due to an absence of the other voltage harmonics except the first one, the total real power can be computed by the following equation 1.11 [39].

$$P = V_{RMS,1} \cdot I_{RMS,1} \cdot \cos\theta_1 \tag{1.11}$$

$$PF = \frac{P}{S} = \frac{V_{RMS,1} \cdot I_{RMS,1} \cdot \cos\theta_1}{V_{RMS,1} \cdot \sqrt{\sum_{k=1}^{\infty} I_{RMS,n}^2}} \tag{1.12}$$

If the equation 1.12 [39] is simplified, it is obtained the following expression 1.13 [39]. The equation is composed of two factors k_{dist} and k_{disp}.

$$PF = \frac{I_{RMS,1}}{I_{RMS}} \cdot \cos\theta_1 = k_{dist} \cdot k_{disp} \tag{1.13}$$

Where θ is a phase shift between a voltage and a fundamental component of the line current. $I_{RMS,1}$ is a *RMS* value of the fundamental component of the line current, I_{RMS} is a *RMS* value of the total line current [39].

k_{dist} is a distortion factor which is defined as a fraction of the fundamental component of the line current and the total line current (contains all harmonics).

$$k_{dist} = \frac{I_{RMS,1}}{I_{RMS}} = distortion factor \tag{1.14}$$

k_{disp} factor describes an angle between the line voltage and the fundamental component of the line current.

$$k_{disp} = \cos\theta_1 = displacement factor \tag{1.15}$$

A further important parameter is a total harmonic distortion of the line current $THDi$, which is defined as follows:

$$THD = \sqrt{\frac{\sum_{k=2}^{\infty} I_{RMS,n}^2}{I_{RMS,1}^2}} = \sqrt{\frac{1}{k_{dist}^2} - 1} \tag{1.16}$$

Conventional SMPSs use a rectifier with a bulky capacitor. As result the line current is characterized by a high pulsation 1.3. $THDi$ comes over 70% and PF is poor, it does not exceed $0,67$. The equations (1.14) and (1.16) [39] demonstrate that the power factor and

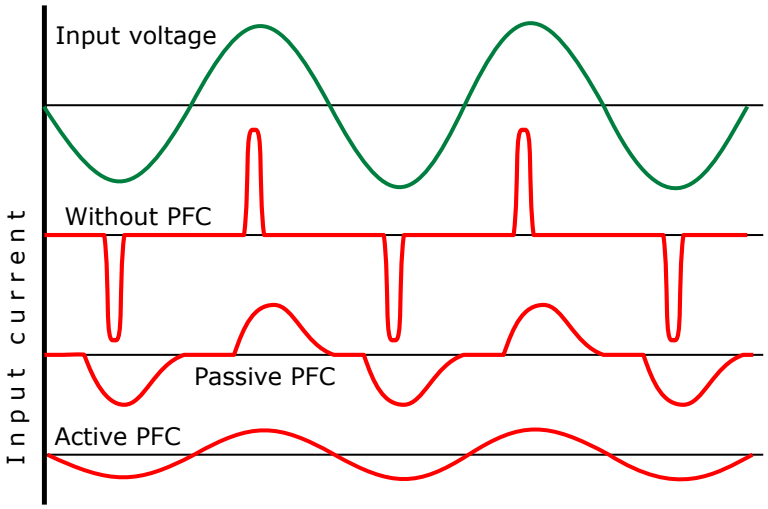


Fig. 1.3 Voltage and current waveforms.

total harmonic distortion are connected together. If the power factor is near unity, the total harmonic distortion is very small [39], [33].

1.3 Energy Balance

The function of the APFCs is based on the cycles of a storing and a releasing energy. This situation is described in the figure 1.4. An energy balance is explained by an ideal situation, i.e. the power factor equals to one. The line voltage and current are sinusoidal and they are in phase. They can be expressed by the following expressions (1.17 and 1.18) [39].

$$v(t) = V_m \cdot \sin n\omega t \tag{1.17}$$

$$i(t) = I_m \cdot \sin n\omega t \tag{1.18}$$

The equation (1.19) [39] represents the instantaneous input power.

$$p_{in}(t) = v(t) \cdot i(t) = V_m \cdot I_m \cdot \sin^2 \omega t \tag{1.19}$$

The average input power can be computed by the following equation 1.20 [39].

$$P_{in} = \frac{V_m \cdot I_m}{2} \tag{1.20}$$

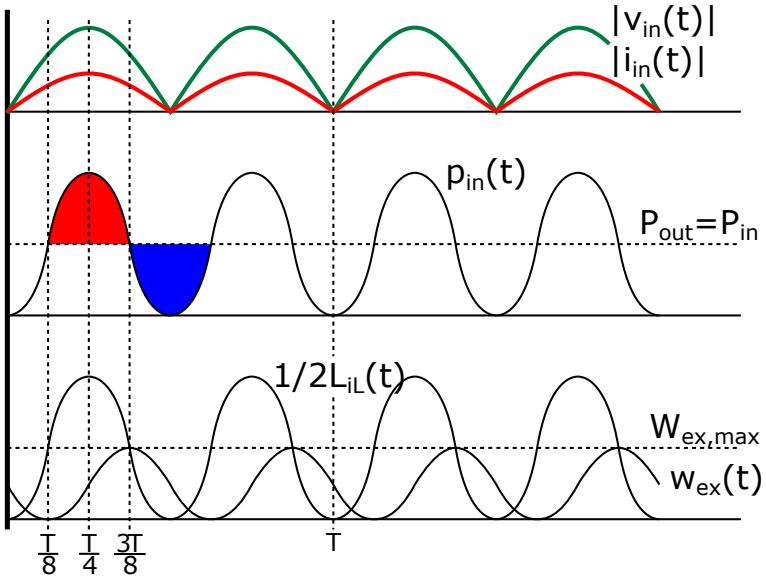


Fig. 1.4 Energy balance in PFC.

As it is clear from the equations 1.19 and 1.20, the instantaneous input power is defined in the equation 1.19 [39]:

$$p_{in}(t) = P_{in} \cdot (1 - \cos 2\omega t) \tag{1.21}$$

The instantaneous input power consists of the real power, i.e. the average power and the alternate component. This component has a twice line frequency. The principle of the power factor correction is to store the excessive input energy when the input power is greater than the output power and release the stored energy at the right moment when the input power is smaller than the output power. The equation (1.22) [39] represents the instantaneous excessive input energy. The energy is stored in the storage components, i.e. inductors and capacitors, and it is released at the right moment [39].

$$w_{ex}(t) = \frac{P_o}{2\omega_1} \cdot (1 - \sin 2\omega_1 t) \tag{1.22}$$

1.4 History of Power Factor Correction

Nowadays, we are dependent on many electric devices. The most of them consists of non-linear components, which are silicon diodes, transistors, etc. If the non-linear loads are connected into the power grid, they causes a non-linear line current. Consequently, the voltage distortion is propagated due to the non-zero system impedance. This power system pollution is a crucial problem.

The first regulation of the power factor was established at the end of the nineteenth century. The British Lighting Clauses Act of 1899 concerns of the power system disturbances which were caused by a flicker of incandescent arc-lamps.

The second mention of the power factor correction was during the sixties of the twenty century when large consumers begin to correct a poor power factor by the *VAR* compensator.

In the seventies and eighties of the twenty century, the first technical standards IEEE519-1981 and IEC 555-2 were adopted. The technical standards provide a technical reference for designers and manufactures. The creation of these norms caused a rapid research and development of power factor correctors. Researchers and industry were stimulated by the new movement of the SMPSs which let develop low-cost and effective devices.

The power electronic systems for reducing of the harmonic pollution were rapidly used in the nineties due to a massive development of the power semiconductor devices [39], [6].

Chapter 2

Current Status of Power Factor Correction

At present, a technical standard ČSN EN 61000-2-3 [42] regulates the power factor in the power systems. The standard is divided into six parts. The first part describes general considerations, definitions, and terminology. The second part deals with a description and a classification of the environment levels and compatibility. The third part shows emission and immunity limits. This part determines harmonic emissions of the equipment so that the compliance of a norm and emissions permitted from other equipment shall not exceed the electromagnetic compatibility level.

The standard defines four main classes which are called A, B, C, and D. The class A includes symmetric 3-phase equipments, household appliances except of devices which were identified as class D, stationary power tools, dimmer for bulbs, and audio devices. The class B includes portable power tools and unprofessional arc welders. The lighting equipment regulations are included in the class C. The class D contains televisions, personal computers and their monitors. Each class has different limits of electromagnetic emissions. The standard defines also measuring circuit, power supply, and other circumstances.

The fourth part explains testing methodologies, and measurement techniques. The fifth part contains installation and mitigation guidelines. The last part includes miscellaneous issues.

There is a 80$PLUS$ certification which determines that the power supply has the efficiency over 80% and power factor is over 0.9. The 80$PLUS$ performance specification is divided into six subclasses (see in the tabular 2.1) [34].

Table 2.1 80 plus definition [34].

% rated Load	10%	20%	50%	100%
80 Plus	-	82%	85%/PF=0.9	82%
80 PLus Bronze	-	85%	88%/PF=0.9	85%
80 Plus Silver	-	87%	90%/PF=0.9	87%
80 Plus Gold	-	90%	92%/PF=0.9	90%
80 Plus Platinum	-	92%	94%/PF=0.9	92%
80 Plus Titanium	90%	94%	96%/PF=0.9	94%

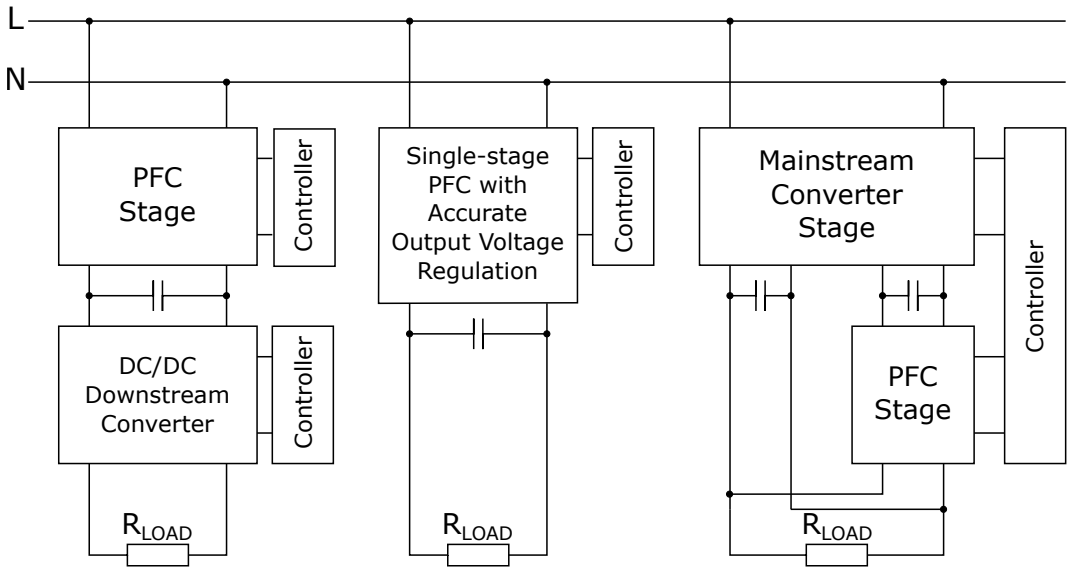


Fig. 2.1 System configuration.

2.1 System Configuration

This section is devoted to the configuration of APFC and SMPS. Basically, there are three power system configuration which are two stage, single stage and parallel stage converters. The configuration have influence on a correction performance, efficiency, output voltage regulation, and control complexity [39].

2.1.1 Two Stage Converters

This system configuration includes two stages which are cascaded. The first stage creates APFC. The APFC stage provides voltage conversion from AC line with the $85-265$ VAC voltage range to the 390 VDC output voltage and forces a line current to be sinusoidal in phase with the line voltage. In other words, the stage is used as a pre-converter. The output

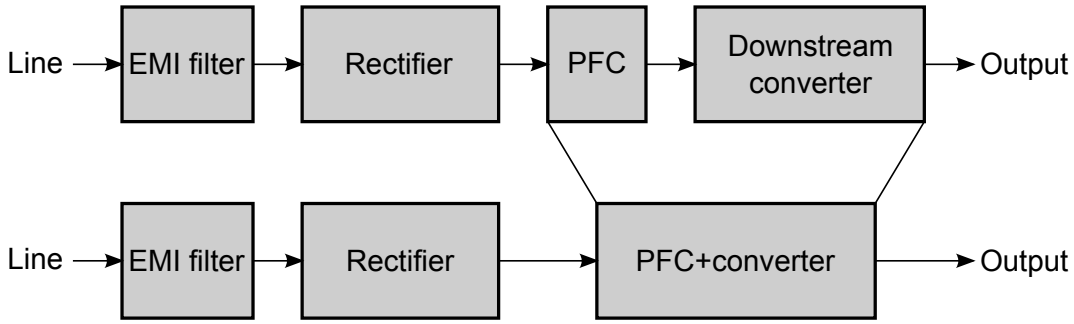


Fig. 2.2 Single-stage APFC.

voltage creates an intermediate voltage with a second harmonic pollution for a downstream converter. The converter creates the second stage. It provides a tight voltage regulation to the determined level.

This configuration is preferred due to independent design issues, two independent control systems, a system stability, and a easy implementation. The disadvantages are a double conversion, an overall efficiency, a reliability and costs. In spite of this facts, it is the most popular type of configuration in an industrial and commercial share [39].

2.1.2 Single Stage Converters

The conventional approach of the PF regulation is inserting of the APFC between a rectifier and a downstream DC/DC converter. It occurs the double conversion which is not an energy efficient. A single-stage APFC integrates both converters into one which is usually Flyback. The converter offers an output voltage regulation, galvanic isolation and PF correction [39], [33].

A component count reduction and an efficiency improvement are the main advantages. A bulk capacitor is connected only on the secondary side of the transformer contrary to the conventional Flyback converter. There is only a small $1nF$ capacitor on the rectifier output so that it does not cause a PF degradation. Single-stage correctors are able to operate under DCM, CrM and CCM modes.

The PF correction is disturbed due to the compensation of input voltage fluctuations. The feedback bandwidth is in range from 10 to $30Hz$ for the correctors. As a result, a response to the load changes is slow. If the POL converter on the output is used, the slow response is not a crucial problem. APFCs do not also need the bulk capacitor with great capacitance when the POL converter is used. The output voltage ripple can be reduced by the POL converter.

If the line voltage goes up or the load goes down, it worsens PF due to the fact that it is dependent on a duty cycle of the corrector and a non-linear characteristic of the transformer

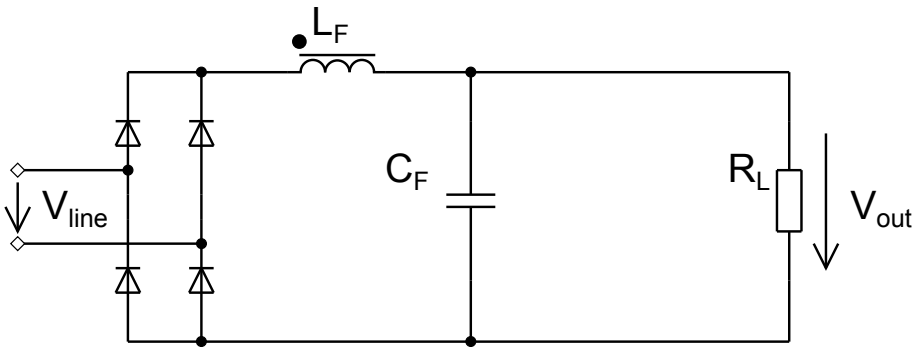


Fig. 2.3 Schematic diagram of the passive power factor corrector.

magnetic core. After all, the PF factor can be kept above 0.9. The single-stage topology based on Flyback converter is suitable solution for low power converters, LED power supplies and small NTB adapters [33], [30], [31], [28].

2.1.3 Parallel Stage Converters

The main drawback of the two stage converters is a double conversion of the power during a full period of the line voltage. Conventional two-stage converters use an one power path. In the case of parallel ones, the power paths are two. The main converter process an average energy from a line to the load. The APFC stage operates only during 32% of the line period. This stage is capable of accumulating the excessive energy and releasing the stored energy in the appropriate moment. The advantage is a high efficiency of the system due to the fact that only 32% of the input power is processed twice. The main disadvantage is a complex design and construction of the correctors. [39]

2.2 Passive Power Factor Correctors

Passive power factor correctors consist of passive components as the name suggest. Basically, they are simple low pass filters. The passive correctors are most frequently placed between a rectifier and a downstream converter. Unfortunately, they have a poor ability of the correction, large weight and volume, a dependence the output voltage on the input voltage, slow dynamic response and difficult design optimization. The most popular passive power factor corrector schematic diagram is shown in the picture (2.3) [39], [33]. Its transfer function and input impedance is below:

$$H(s) = \frac{1}{s^2 \cdot L_F \cdot C_F + s\frac{L_F}{R_L} + 1} \tag{2.1}$$

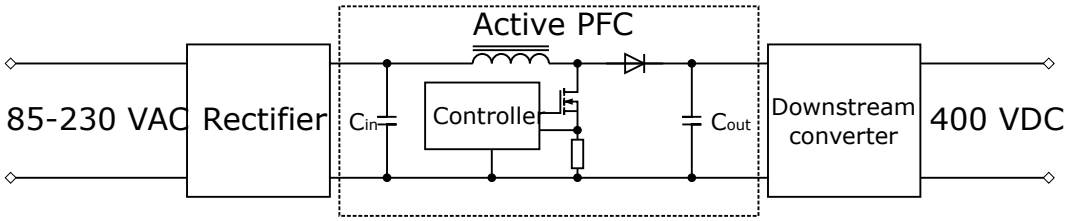


Fig. 2.4 Block diagram of the active power factor corrector.

$$Z_{in}(s) = R_L \cdot \frac{s^2 \cdot L_F \cdot C_F + s \cdot \frac{L_F}{R_L} + 1}{s \cdot R_L \cdot C_F + 1} \tag{2.2}$$

The inductor can be in front of or behind the rectifier. The second case is preferable due to a higher frequency of the current an inductor weight can be radically reduced. Passive power factor correctors are used to correct a poor PF in the low cost and the low power applications [39], [33], [36].

2.3 Active Power Factor Correctors

APFCs emulate pure resistive electric loads, i.e. the input current and voltage are sinusoidal and in phase. The basic principle is based on a PWM modulation of the line current which changes an input impedance of the corrector by a storing and a releasing the energy of accumulative components. Basically, every switch mode power topology can be used to correct the power factor but only few are suitable. The most widely used topology is a Boost converter (2.4). The Boost converter has a minimal component count, a grounded power switch, a good efficiency, a power factor correction ability, a constant output voltage and a wide input voltage range. These features are eligible for many power systems in the world. The second most used converter is Flyback which is used for low power application (lighting, NTB adapters, etc.) [39], [33], [36].

2.4 Boost Converter

Various topologies can be used for power factor correctors. The Boost converter is preferred due to the variable input voltage. Generally, these converters are designed for the $85-265$ VAC input range. The output voltage of the converter is usually set to 390 VDC. Other advantages of the Boost converter are a grounded power switch, less EMI, and lower power

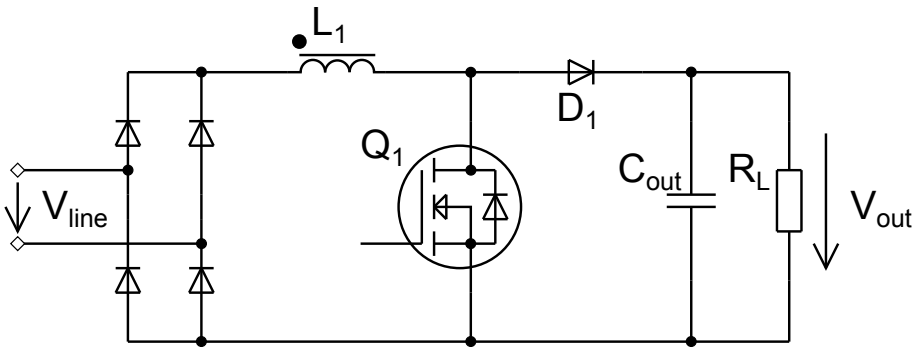


Fig. 2.5 Schematic diagram of the Boost converter.

switch current [39], [33]. The equation (2.3) [39] represents a transfer function.

$$H(s) = \frac{\frac{1}{d'}}{s^2 \cdot \frac{L_1}{d'^2} \cdot C_{OUT} + s \cdot \frac{\frac{L_1}{d'^2}}{R_L} + 1} \tag{2.3}$$

The input impedance is given by the expression 2.4 [39].

$$Z_{in}(s) = d'^2 \cdot R_L \cdot \frac{s^2 \cdot \frac{L_1}{d'^2} \cdot C_{OUT} + s \cdot \frac{\frac{L_1}{d'^2}}{R_L} + 1}{s \cdot R_L \cdot C_{OUT} + 1} \tag{2.4}$$

Other APFC topologies are also based on the Boost converter. They are called interleaved and bridgeless topologies which are discussed in other chapters. These topologies have an improved efficiency, smaller dimensions, and better heat dissipation due to a distribution of the losses into more components.

Chapter 3

Current Conduction Modes

This chapter is devoted current modes which are used in APFCs. The modes decide about features of the corrector. These modes are divided according to current waveform as well as in the case of conventional power converters. The figures 3.1 provide a better understanding of the different modes. All of them have one limitation due to the better graphical illustration. The frequencies are not consistent with the reality. Whereas, the ratio between a real line frequency and a switching frequency of the corrector is for example 4000. The ratio in the figures with the waveforms is $10 - 14$.

There are four basic modes which are Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Critical Conduction Mode (CrM), and Frequency Clamped Critical Conduction Mode (FCCrM). The next sections describes all these modes and their features [33], [45].

3.1 Continuous Conduction Mode

CCM is the most common mode in APFCs. CCM is characterized by an absence of the decrease current to zero within one switching cycle. As a result, the line current swings around the sinusoidal average value. The switching frequency is fixed. This feature simplifies an EMI design and a setting of the compensation network. CCM reduces effectively an input current ripple and an input current peak. Thanks to this feature the mode is suitable in the wide power range. In the other hand, a power transistor and a diode rectifier have to withstand a greater current stress due to the hard-switching conditions. It puts a great demands on the parameters of the power stage. As a consequence, Boost diodes shall be provided by SiC Schottky Barrier Diodes due to their advantageous properties. The mode requires also a higher value of the inductance than other ones. It has an impact on the costs [33], [45].

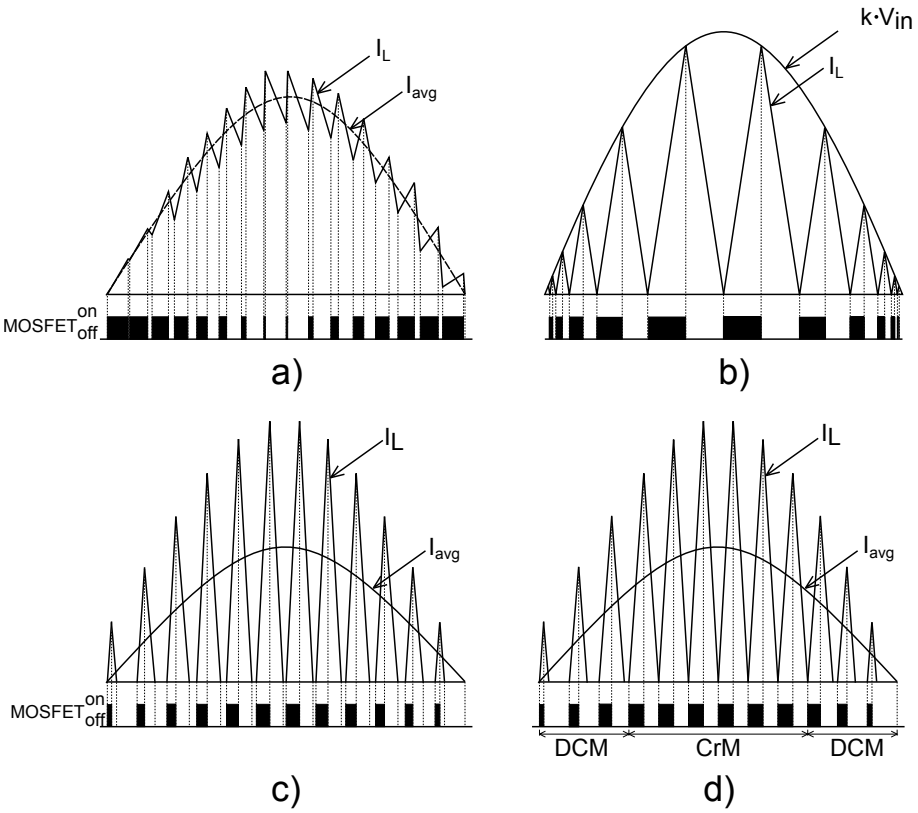


Fig. 3.1 Typical waveforms of current modes, a) CCM, b) CrM, c) DCM, d) FCCrM.

3.2 Discontinuous Conduction Mode

DCM use is limited to the special cases and as a part of FCCrM. When the converter operates under DCM, a waveform of the current can be splitted into three parts. The first part is characterized by the rising of the current , the second one by the falling to zero and last by the dead time. Due to the short rise times the correctors are a higher input ripple and peak current, a significant THD, and EMI. Therefore DCM is usually used in the cases which require constant switching frequency. It is especially in FCCrM when the line voltage drops to a low voltage close zero where CrM causes an unacceptably high switching frequency. The most frequently use is in FCCrM mode which combines DCM with CrM [33].

3.3 Critical Conduction Mode

CrM plays an important role in modern APFCs. The mode is suitable especially for low power and low cost correctors. The switching frequency is variable in a comparison to CCM. The critical conduction mode is a special case of DCM. This mode is characterized by an activation of the power switch when the inductor current drops to zero (quasi-resonant mode). It allows to use lower quality and cheaper power components (Boost diode, transistors, etc.). The main disadvantages are variable switching frequency, greater input peak and ripple current, and high switching frequency at the low voltage on the input [33], [45].

$$I_{in(avg)} = \frac{I_L(t)}{2} \tag{3.1}$$

The switching frequency depends on the input voltage and input power. Two relations are important for this kind of control. The first one (3.1) [33] is derived from the triangular shape of the inductor current. As a result, the on-time depends only on the line voltage and load. The second one (3.2) [33] defines the on-time.

$$t_{on} = \frac{2 \cdot P_{in} \cdot L}{V_{ac}^2} \tag{3.2}$$

Advantages of CrM include simple control circuits, easy design, low price, good power factor, total harmonic distortion, small switching losses, good efficiency in the low power devices, and no silicon carbide diode due to a soft switching. On the other hand, the corrector has higher peak current, higher electromagnetic interference, and variable switching frequency. The Critical Conduction Mode is suitable for application up to 250 Watts [33], [45], [22].

3.4 Frequency Clamped Critical Conduction Mode

As the name suggests, the mode is based on the CrM. Due to the fact that the switching frequency of the CrM is inversely proportional to the instantaneous line voltage this mode is inconvenient at the low voltage conditions. Theoretically, when the input voltage is zero the switching frequency reaches infinite value. Practically, the switching frequency can increase to $1MHz$ therefore the switching frequency shall be clamped at an appropriate functional limit.

The practical limits are clamped between 50 and $500kHz$. The lowest limit is set at a peak value of the line voltage and light load conditions. The $50kHz$ value is usually selected due to an audible noise restrictions. The top limit $500kHz$ is selected with respect to hardware limitations. The figure 3.1 illustrates the borders between CrM and DCM. When the voltage is low the corrector works under DCM and its switching frequency is kept at constant value $500kHz$. Conversely, at the top voltage region the corrector operates at CrM. The switching frequency is variable at this operation conditions [33].

Chapter 4

Control Methods

This chapter is devoted to control methods of APFCs. APFCs are a kind of SMPSs which include two control loops. A voltage loop provides an output voltage regulation. A current loop is used for a line current shaping. The control system is complex and includes often multiplier which causes a higher manufacturing costs. Due to this fact there are some methods which do not include a multiplier. Next sections describe several common control techniques and their main features.

4.1 Average Current Control

Average Current Control is the most widely used control technique. The control circuit contains two control loops 4.2. An input current is shaped by the feed forward loop, which is wideband. An output voltage is regulated by a voltage feedback loop. It is narrowband contrary to the feed forward loop. The error amplifier OA_2 keeps constant output voltage and reduces harmonic distortion. The I_{cp} current signal is created by the block "Multiplier and Divider" and it is equivalent to the line voltage. The voltage drop of resistor R_{sh} is almost the same as the resistor R_{cp} voltage drop. The current flowing through the resistor R_{sh} is proportional to the input current. This signal is a sum of the current flowing through the transistor Q_1 and the diode D_5 when the transistor is in the off-state. This signal forces the resistor R_{sh} current to offset a voltage increase of the resistor R_{cp}. This technique keeps the input current and voltage in the same shape and phase [39], [36], [21], [33].

The block "Squared" solves the main problem of the average current control. The problem is a compensation of the line voltage increment. When the voltage goes up, the voltage divider gives an increased voltage reference for the feed forward loop. This increment must be compensated by the feed forward loop because the voltage feedback loop has a too slow response. When the line voltage goes up, the current must goes down. If both go up, the input

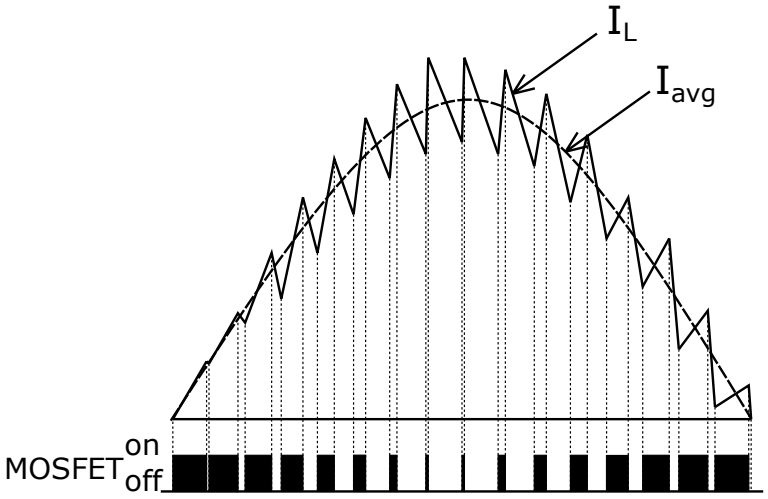


Fig. 4.1 CCM waveform.

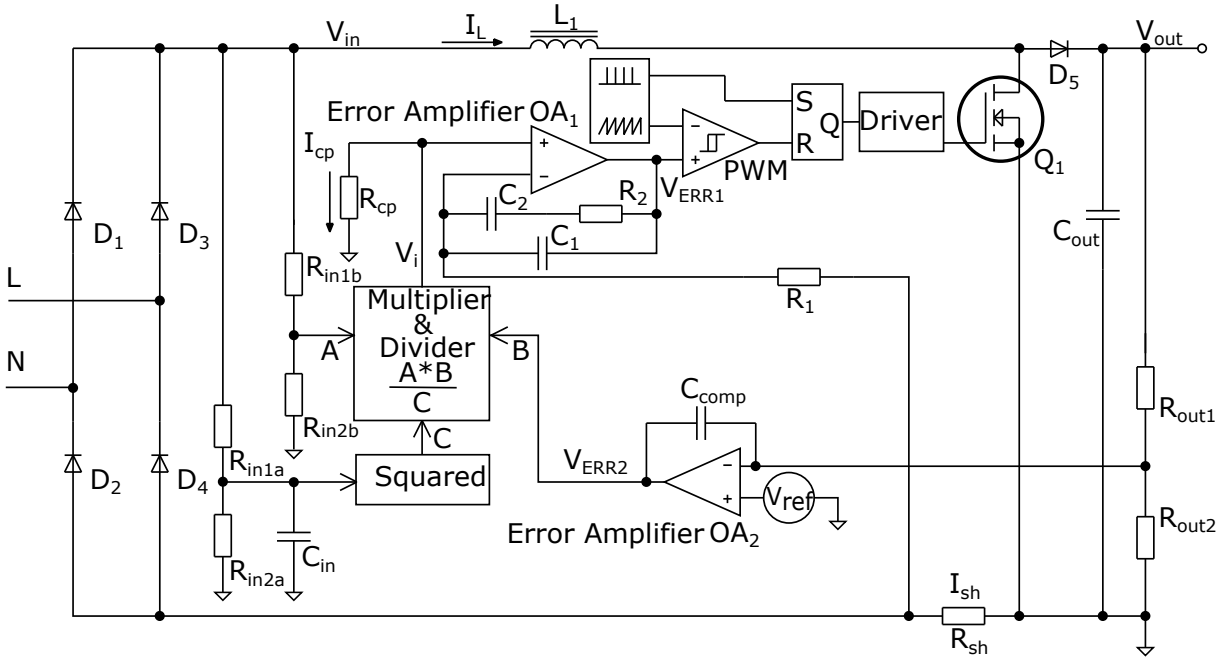


Fig. 4.2 Block diagram of the average current control.

power increases too. As a result, the output voltage can overshoot the right value. The block "Squared" multiplies the output signal of the low pass filter by itself. It is proportional to the amplitude of the line voltage. It creates a signal for the denominator of the block "Multiplier and Divider". As a result, the reference V_i signal is negatively proportional to the line voltage, i.e. when the line voltage increases, the current decreases and vice versa.

4.1.1 Signal Creating for Transistor

The saw-tooth generator determines the switching frequency of the power transistor. The switching frequency range is usually selected from 60 to 200kHz. The generator has two outputs. The first one generates the saw-tooth signal, the second one creates short pulses for the flip-flop setting. The signal activates a power transistor at the beginning of an every cycle of the saw-tooth generator. The power transistor is turned off when the saw-tooth signal crosses the error voltage from the error amplifier OA_1. The technique forces the right current shape through the resistor R_{sh}. The negative feedback of the error amplifier OA_1 keeps the voltage between inputs at the same value. The amplifier OA_1 integrates the difference between the voltage drops across the R_{cp} and R_{sh} resistors. The resistor R_{cp} voltage drop is always bigger than the R_{sh} resistor voltage drop in spite of the feedback, which regulates these voltages. The difference between the voltage drops creates the error voltage signal which has a positive convex shape. This signal is compared with the saw-tooth signal.

The signals are illustrated in the figure 4.3. At points A and C the saw-tooth signal crosses the error voltage from OA_1 when it has a higher value. Therefore an on-time of the transistor is longer than the on-time at point B when the error voltage reaches the lower value. The on-time of the transistor depends on the input voltage; the longest on-time is around the regions A and C, the shortest on-time is placed around region B. This technique creates the PWM signal for the transistor, which is amplified by the power driver. As a result, it forces the input current to follow the input sinusoidal voltage [39], [36], [21], [33], [8].

4.1.2 Output Voltage Regulation

The output voltage regulation is based on the feedback which compares the output voltage with the reference voltage. The output signal from the multiplier is an undistorted rectified sinusoidal signal with an offset. Its amplitude is proportional to the output voltage of the amplifier OA_2. If the output voltage goes up, the error voltage V_{ERR2} goes down. As a result, the error voltage V_{ERR1} decreases as well. Consequently, the saw-tooth signal crosses the error voltage V_{ERR1} earlier in every duty cycle. Thus, the output voltage V_{out} reaches the right

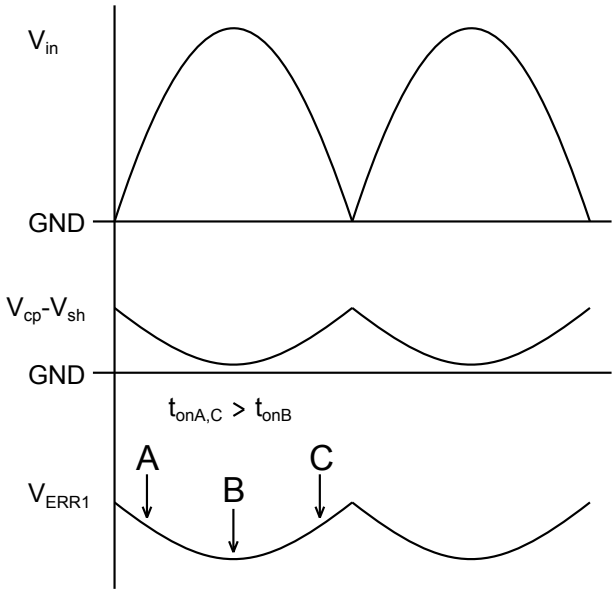


Fig. 4.3 Error signal.

value. The V_i signal contains information for keeping the output voltage at the constant value as well as information for the input current shaping [39], [36], [21], [33].

4.2 CrM with Current Control

This section describes a control method which is used for the correctors operating under CrM. The current mode control block diagram is shown in the figure 4.4. The error amplifier OA_1 compares the output voltage with the voltage reference (V_{ref}). The error signal gives information about the output voltage and it is connected to the first input of the multiplier [33], [57].

The second input is connected to the transducer of the rectified input voltage. The multiplier output provides a rectified sinusoidal signal; its amplitude is influenced by the error signal from the error amplifier. The signal is a reference for the input current modification.

Its amplitude depends on the output power; it keeps the right value of the output voltage. If the transistor is switched on, the inductor current increases as long as the voltage drop across the R_{sh} resistor does not reach the boundary of the reference signal. Once the voltage drop across the resistor reaches the reference boundary, the comparator will flip and the transistor is switched off . Consequently, the current falls to zero and the cycle starts again [33], [57].

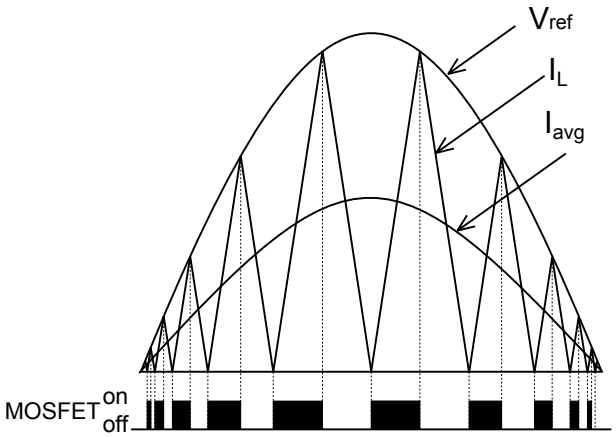


Fig. 4.4 CrM with the current control.

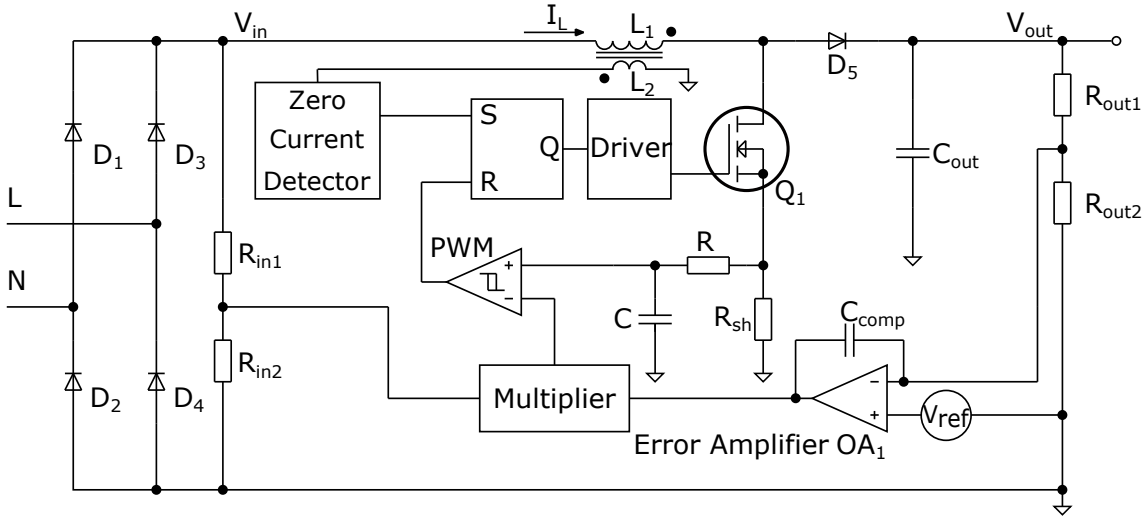


Fig. 4.5 Block diagram of the current control.

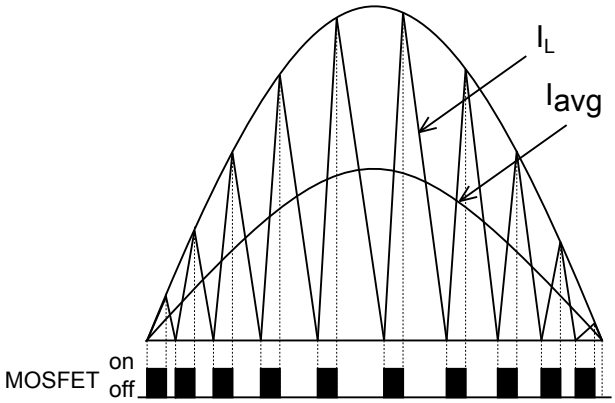


Fig. 4.6 CrM with the voltage control.

The current sensing is realized by the measuring of the inductor voltage. If the inductor voltage is zero, the current stops flowing. The transistor turns on again thus the current begins to increase again.

Basically, the control technique keeps the inductor current at the boundary between continuous and discontinuous modes as it shows the figure (4.4). Due to knowledge of the exact waveform shape the average line current equals to the half value of the peak current. The voltage drop across the shunt resistor (R_{sh}) equals to the multiplier output signal divided by the factor 2.

The frequency is variable, it is proportional to the line voltage and load. If the line voltage is high and the output power is low, the switching frequency has a maximum value. The switching frequency is variable during the half period of the line frequency. It is the highest at a low voltage, the smallest at peak [33], [57], [22].

4.3 CrM with Voltage Control

The voltage mode control is a newer approach for the correctors with CrM, which does not need a multiplier. The block diagram is shown in the figure 4.7. A waveform of the inductor current increases from zero to the reference signal; then it falls back to zero. The waveform is similar to the current mode control (4.6) [33], [9], [22]. The reference signal is a scaled-down version of the rectified line voltage. It is a product of the input voltage and the k constant , which is the constant of the voltage divider. The following two equations for the peak current are based on the knowledge of the line current waveform [33], [9], [22].

$$I_{pk} = k \cdot V_{in}(t) \tag{4.1}$$

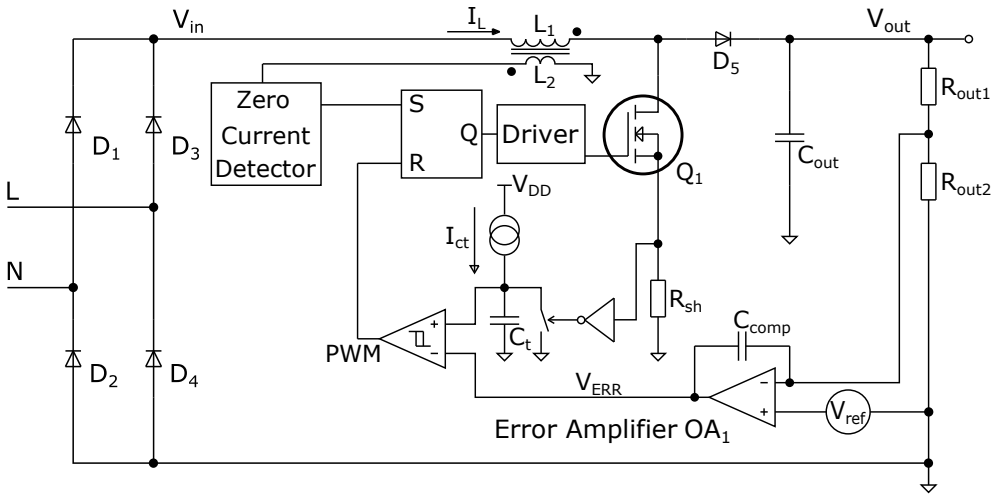


Fig. 4.7 Block diagram of the voltage control.

$$I_{pk} = \Delta I = \frac{V(t)}{L} \cdot t_{on} \tag{4.2}$$

It regards following equations.

$$k \cdot V_{in} = \frac{V_{in}(t)}{L} \cdot t_{on} \tag{4.3}$$

$$t_{on} = k \cdot L \tag{4.4}$$

The equation 4.4 shows that the transistor on-time (t_{on}) is constant for the product of the k constant and the inductance L. Whereas the off-time is variable within a half period of the mains. As a result, the transistor switching frequency is variable.

The transistor on-time depends on the line voltage amplitude and the load. An advantage of the voltage control technique is that it does not need the multiplier. The voltage drop across the R_sh resistor needs to be detected only for an over current protection. The CrM mode is provided by the constant on-time of the transistor [33], [57], [27], [29], [22].

$$I_L(t) = \frac{V_{in}}{L} \cdot t \tag{4.5}$$

The peak inductor current ($I_{L_{pk}}$) [57] depends on the input voltage. The constant k is variable within a half period of the line voltage.

$$I_{L_{pk}} = \frac{V_{in}}{L} \cdot t_{on} \tag{4.6}$$

Thus, the on-time is defined in the next equations (4.7) [57].

$$t_{on} = \frac{L \cdot I_{L_{pk}}}{V_{in}} \tag{4.7}$$

If the transistor is open, the current flows via the boost diode into the bulk capacitor and the load. The transistor off-time depends on the peak current $I_{L_{pk}}$, the output voltage V_{out} and the input voltage V_{in}. The off-time is derived from the equation 4.8 [3], [22].

$$I_L(t) = I_{L_{pk}} - \left(\frac{V_{out} - V_{in}}{L} \cdot t_{off} \right) \tag{4.8}$$

Finally, the off-time is determined by the equations (4.9) and (4.10) [57], [22].

$$0 = I_{L_{pk}} - \frac{V_{out} - V_{in}}{L} \cdot t_{off} \tag{4.9}$$

$$t_{off} = \frac{L \cdot I_{L_{pk}}}{V_{out} - V_{in}} \tag{4.10}$$

The cycle period is provided by a summing (4.7) and (4.10) [57], [22].

$$T = L \cdot I_{L_{pk}} \cdot \frac{V_{out}}{V_{in}(V_{out} - V_{in})} \tag{4.11}$$

Then there are defined the following dependencies.

$$i_{in}(t) = \frac{I_{L_{pk}}}{2} = \sqrt{2} \cdot I_{ac} \cdot \sin \omega t \tag{4.12}$$

$$v_{in}(t) = \sqrt{2} \cdot V_{ac} \cdot \sin \omega t \tag{4.13}$$

$$I_{L_{pk}} = 2 \cdot \sqrt{2} \cdot I_{ac} \cdot \sin \omega t \tag{4.14}$$

$$I_{L_{pk}} = 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{ac}} \cdot \sin \omega t \tag{4.15}$$

The cycle period (equation 4.16) can be redefined by an inserting (4.13) and (4.15) into (4.11) [57], [22].

$$T = L \cdot 2 \cdot \sqrt{2} \cdot \frac{P_{in}}{V_{ac}} \cdot \sin \omega t \cdot \frac{V_{out}}{\sqrt{2} \cdot V_{ac} \cdot \sin \omega t \cdot (V_{out} - V_{in})} \tag{4.16}$$

If the equation (4.16) [57] is simplified, the expression 4.17 is obtained [22].

$$T = \frac{2 \cdot L \cdot P_{in} \cdot V_{out}}{V_{ac}^2 \cdot (V_{out} - V_{in})} \tag{4.17}$$

As is clear from (4.17), the frequency is derived from the next equation.

$$f = \frac{V_{ac}^2 \cdot (V_{out} - V_{in})}{2 \cdot L \cdot P_{in} \cdot V_{out}} \tag{4.18}$$

Similarly, for the frequency it is also valid the following relation (4.19) [57].

$$f = \frac{V_{ac}^2}{2 \cdot L \cdot P_{in}} \cdot \frac{V_{out} - \sqrt{2} \cdot V_{ac} \cdot \sin \omega t}{V_{out}} \tag{4.19}$$

It can be written as the next equation (4.20), where are two factors. The first one depends on the line voltage and the load, the second one can be called as a modulating factor. It affects the switching frequency during the half period of the line frequency [57], [22].

$$f = \frac{V_{ac}^2}{2 \cdot L \cdot P_{in}} \left(1 - \frac{\sqrt{2} \cdot V_{ac} \cdot \sin \omega t}{V_{out}} \right) \tag{4.20}$$

4.4 Variable Frequency Peak Current Control

A variable frequency peak current control is not a widespread control strategy. Its main benefits are an improved efficiency and an simple control circuit. The figure 4.8 depicts a basic block diagram. The output voltage error signal $v_{err}(t)$ is connected to the multiplier where it is multiplied by the $\alpha v_1(t)$ signal which represents an instantaneous input voltage. As a result, the i_{cmd} command is provided by the multiplier output. The command signal can be expressed by the following equation [39].

$$i_{cmd} = \alpha v_1(t) \cdot v_{err}(t) \tag{4.21}$$

The command signal is compared with a sensed current ($\beta i_1(t)$). In other words, the result signal ensures a timing of the transistor so that the line current waveform would be equivalent to the line voltage. The current sensing is provided by the shunt resistor (R_{sh}). The current feedback signal keeps the line current waveform so that the signals from the shunt resistor ($\beta i_1(t)$) and multiplier output (i_{cmd}) would be equivalent. The control strategy is available with a fixed on-time or off-time of the transistor [39].

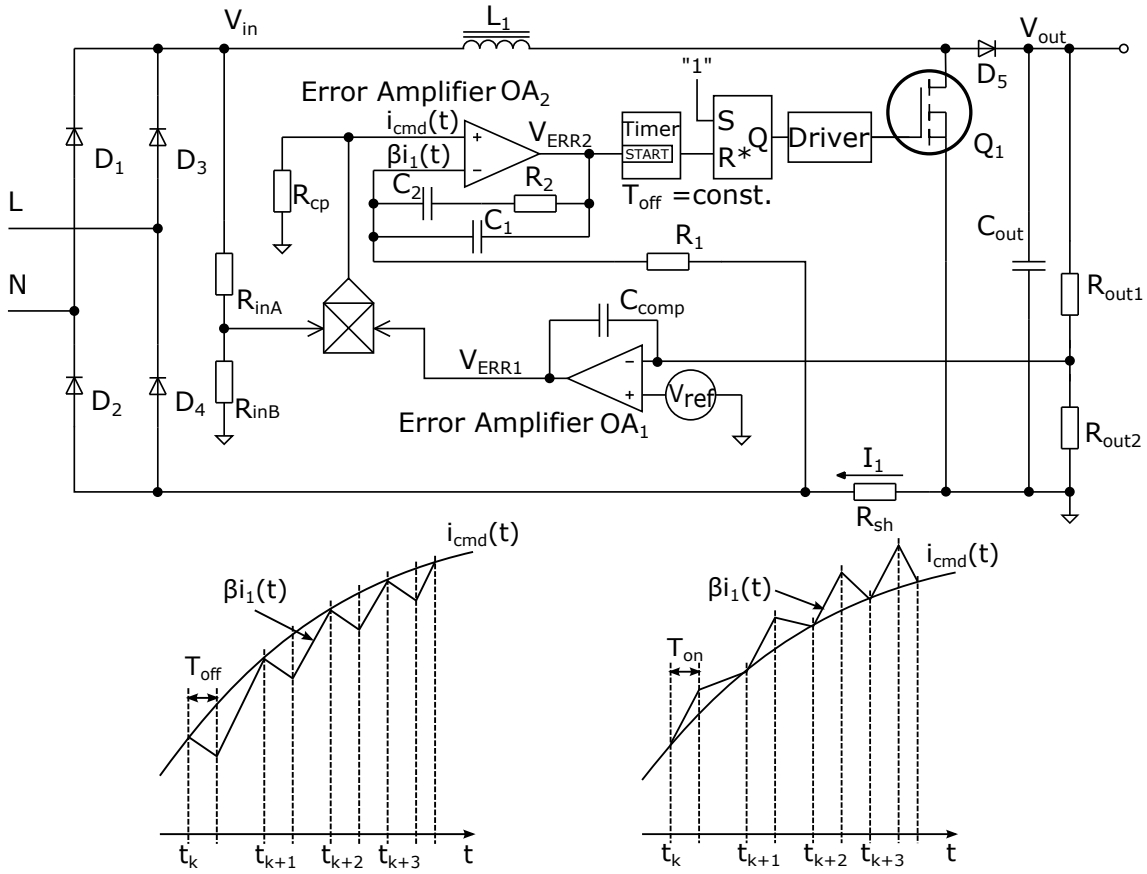


Fig. 4.8 Block diagram of the variable frequency peak current control.

The constant on-time control is characterized by the command signal which creates a bottom envelope of the line current. The transistor is switched on at $t = t_k$ if the line current drops to the command signal. It is determined by the expression ($\beta i_1(t_k) = i_{cmd}(t_k)$). The transistor is released at $t = t_k + T_{on}$. The waveform is described in the figure 4.8.

The second alternative is the constant off-time control which makes a top envelope of the line current. At $t = t_k$ if the $i_{cmd}(t_k)$ command signal equals to $\beta i_1(t_k)$, the the transistor is turned off. The transistor is reactivated after the T_{off} time expires ($t = t_k + T_{off}$) [39].

4.5 Constant Frequency Peak Current Control

The variable frequency peak current control makes complicate a design of the EMI filters due to its variable switching frequency. The constant switching frequency has an impact also on the harmonics reduction. The block diagram (4.9) shows a basic principle of the control technique. The technique is similar as the variable frequency peak current control besides a saw-tooth generator which stabilizes the command signal.

The transistor is activated at time $t = n \cdot T_s$. At time stamp $t = t_n$ the sensed current $\beta i_1(t_n)$ equals to $i_{cmd}(t_n)$ due to the transistor is opened. The line current decreases until the switching cycle expires. Then the new cycle $(n+1)$ starts and the process continue the same way.

These rules are applied by the block diagram. The backbone part consists a R-S flip-flop with constant clock pulses. The R-S flip-flop plays crucial role for a realization of the control technique. On the other hand, the circuit causes unstable behaviour if the duty cycle overcome 50% which shall be solved by a stabilizing signal of the generator. The solution is based on the subtracting of the stabilizing signal from the raw command signal.

Due to the strategy is capable regulating the input current and the switch current as well. The control strategy can be used for buck type topologies. This definition is also valid for the previous control technique.

The advantages are ability to control average current through the transistor, improved switching noise immunity, enhanced dynamic response, elimination of the current compensator which is necessary in the average current control, improved stability and reliability due to low gain in the feed forward loop and pulse-by-pulse current limitation.

Unfortunately, the strategy still requires three sensed signals (input voltage, peak current ,and output voltage). The multiplier is an essential part of the control method. In the comparison with average current control it is characterized by a higher input current ripple at the high line or light load condition. As a consequence, the distortion of the line current is significant at this condition [39].

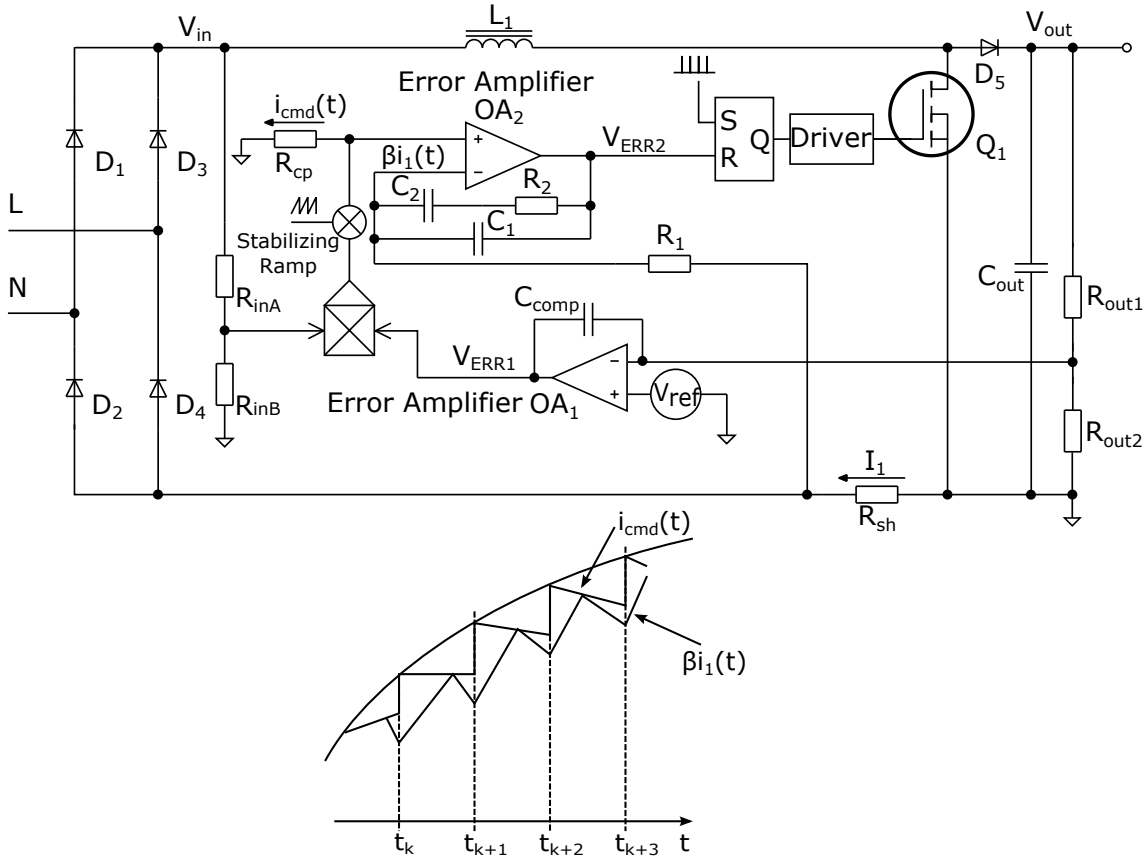


Fig. 4.9 Block diagram of the constant frequency peak current control.

4.6 Hysteresis Control

The hysteresis control belongs into the current control techniques. This control (4.10) requires two reference signals i_{hcmd} and i_{lcmd} which form up and down envelopes of the inductor current. A narrow hysteresis zone causes a small input ripple current and a high switching frequency. The variable switching frequency is proportional to the hysteresis zone and the input voltage changes due to it causes design issues with the EMI filter. The contradictory requirements determine that the hysteresis band shall be designed by a respecting of the component parameters and low line ripple current.

The method is based on a comparison of the sensed line current with the top and bottom reference limits. If the sensed current $\beta i_1(t) \geq i_{hcmd}(t)$, the comparator $C1$ resets the R-S flip-flop. Conversely if the $\beta i_1(t)$ signal is equal or smaller than $i_{lcmd}(t)$, the comparator $C2$ sets the R-S flip-flop. The switching cycles are described in the figure 4.10. The cycle starts at time t_k which is characterized by the equation $\beta i_1(t) = i_{lcmd}(t)$. The power MOSFET is activated and current goes up. At the time $t_k + 1$ the line current reaches to top envelope which is determined by the $i_{hcmd}(t)$ reference signal. Than the transistor is switched off.

The hysteresis control is characterized by several advantages as easy implementation, improved stability, speed of response, and system reliability. The main drawback is the wide switching frequency range which can be eliminated by a control technique based on the constant switching frequency. Unfortunately, the improvement leads to increase a complexity of the control system [39].

4.7 Charge Control

A charge control technique can be used for buck-delivered topologies which are distinguished by a sensing of the switch current instead of the total current in the case of boost-derived topologies. In this control method is used the fact that the average switch current during a switching cycle corresponds to the total charge through the transistor. The charge gauge is provided by the capacitor-switch network. The current transformer ensures a current sense function. The secondary side of the transformer charges a capacitor. If the transistor current rises, the charge of the capacitor increases as well. Generally, the capacitor voltage is proportional to the charge.

The transistor is switched off when the capacitor voltage equals to the command signal. Simultaneously, the capacitor is reset by a switch and the process can start again. Accordingly the power transistor is closed and the switch which reset the capacitor is opened by the clock pulse.

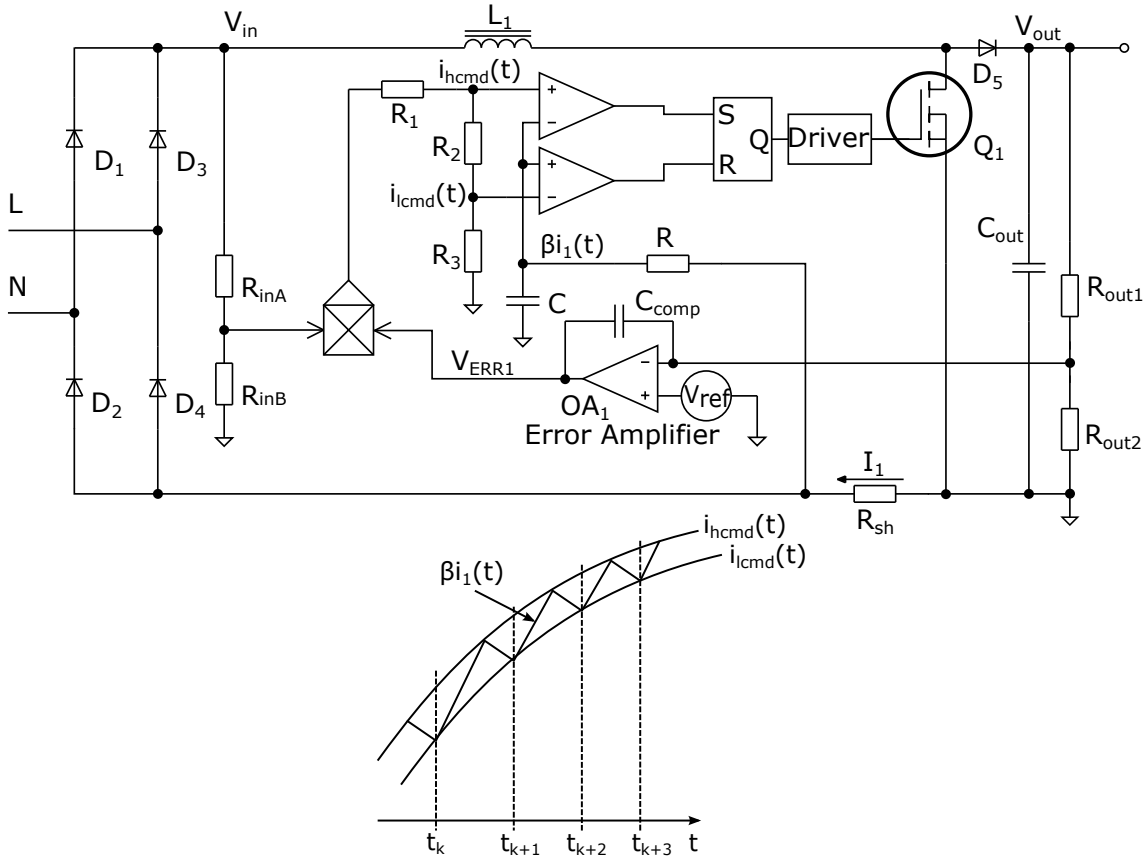


Fig. 4.10 Block diagram of the hysteresis control.

The advantages are average transistor current control capability, improved switching noise immunity, enhanced dynamic response, and current limitation. The disadvantages are sensing input and output voltages which synthesize the command signal. After than the multiplier is still a principal unit of the control system and also potential occurrence of the sub-harmonic oscillation [39].

4.8 Non-linear Carrier Control

This control technique is characterized by a sensing of the output voltage. Through the conversion ratio between the input and output voltages it possible to recover the input voltage. As a consequence, information is used for the current shaping. The main reason why this control method was developed due to it does not need a multiplier. As a result, the control circuitry can be significantly simplified [39].

4.9 Capacitor Voltage Control

This control method uses the fact that the phase shift between the line current and capacitor voltage is proportional to peak values of line current and voltage. Unfortunately, the realization of the delta control system is not simple due to the phase shift is negligible. As a consequence, the small variation of the capacitor voltage causes a enormous variation of the inductor voltage and simultaneously of the line current. Therefore the control technique is influenced to the parameters drift and fluctuations [39].

4.10 Inductor Voltage Control

An inductor voltage control strategy uses the fixed ideally 90° phase shift between the line voltage and the inductor voltage. The strategy is simpler than the Capacitor Voltage Control as well as the final implementation. The inductor voltage is influenced by the perturbation of the phase shift. Whereas the fluctuation of the magnitude of the reference plays negligible role. As a result, the control strategy has a strong ability to keeping line voltage and current in the same shape and phase [39].

Chapter 5

Perspective Topologies and Control Strategies

This chapter describes a perspective solution of APFCs. The standard correctors use a boost converter due to great efficiency and simple design. Correctors require low serial resistance and high quality Q inductors which are generally used in conventional SMPSs. Power transistors used in correctors shall be selected according to a high output voltage of the correctors. The reliability of the transistors is improved by a voltage margin which is usually one half of the output voltage. The high voltage and current rating cause an enhanced gate capacity of the transistor. Therefore the controllers include frequently a power driver which is able to feed the gate capacity by a high current. Consequently, the switching time is minimized and losses as well. Correctors requires a fast rectifier "Boost" diodes which take advantage of the silicone carbide Schottky barrier diodes. The power range of the single boost topology is approximately limited to 2 kW due to this fact the new perspective topologies were developed. The correctors are called bridgeless and interleaved [33].

The control loop should be optimized for a performance of the PF correction. There are many control techniques but the most widely used technique is the average current control which was described in the previous chapter. A development of new sophisticated control methods can bring a better correction performance. An optimization of the control loop during voltage and load changes is the next challenge which can be provided by the digital adaptable control. The compensation of the control loop shall be adjusted on the fly for a maximal performance at various conditions (light load, high line or low line). Modern digital control circuits allow to set several digital filters for an optimization of the control loops [33].

The chapter is divided into three sections. The first section is devoted to bridgeless correctors. The second one describes a principle of interleaved topology. Finally, the last one is dedicated to the differences between analog and digital controllers.

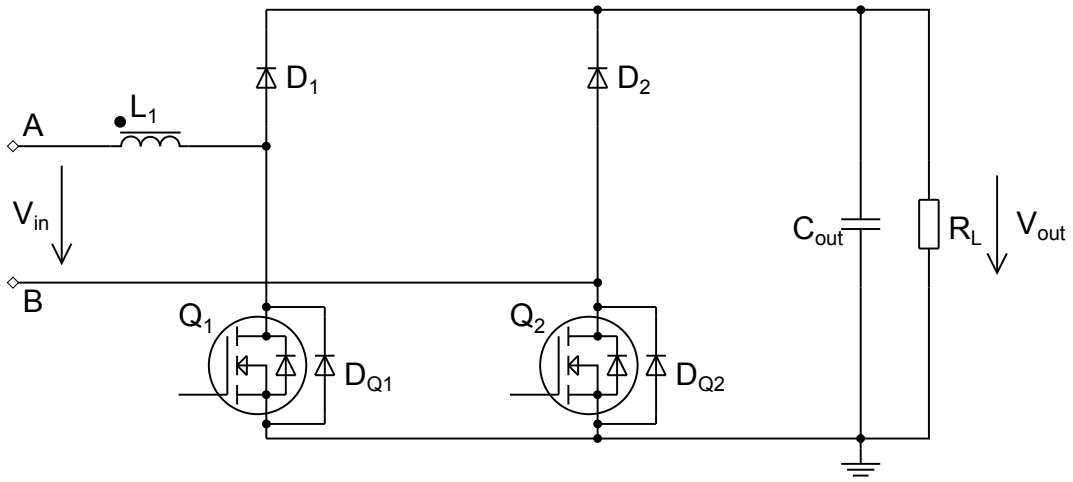


Fig. 5.1 Basic schematic diagram of the bridgeless corrector.

5.1 Bridgeless Topology

The drawback of the simple boost topology is losses in the rectifier which form approximately 50% of the overall corrector losses. The bridgeless topology reduces the rectifier losses to a minimum. The bridge rectifier is removed. Two diodes are replaced by transistors for efficiency improving. The efficiency of the APFC increases by $1-2\%$. The optimization is based on the two-phase utilization of the bridge rectifier [33], [32], [26].

The input current is given by the expression (5.1) [33].

$$I_{in} = \frac{P_{out}}{\eta \cdot V_{in}} \tag{5.1}$$

The average current through the diodes is defined in the equation 5.2 [33].

$$I_D = \frac{2}{\pi} \cdot I_{in_{max}} = \frac{2}{\pi} \cdot \sqrt{2} \cdot I_{in} \tag{5.2}$$

The rectifier losses are derived from the equation 5.3 [33].

$$P_M = 2 \cdot V_f \cdot \frac{2 \cdot \sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in}} \tag{5.3}$$

The basic schematic diagram is shown in the figure 5.1. If the positive voltage is present, the first cell is active. The second cell is active during negative part of the sinusoidal waveform. MOSFET transistor of the inactive cell stays switched off whereas the current flows to the voltage source through the body diode. This diagram shows a principle of the converter. The practical using is limited by some drawbacks. The first one is a floating supply

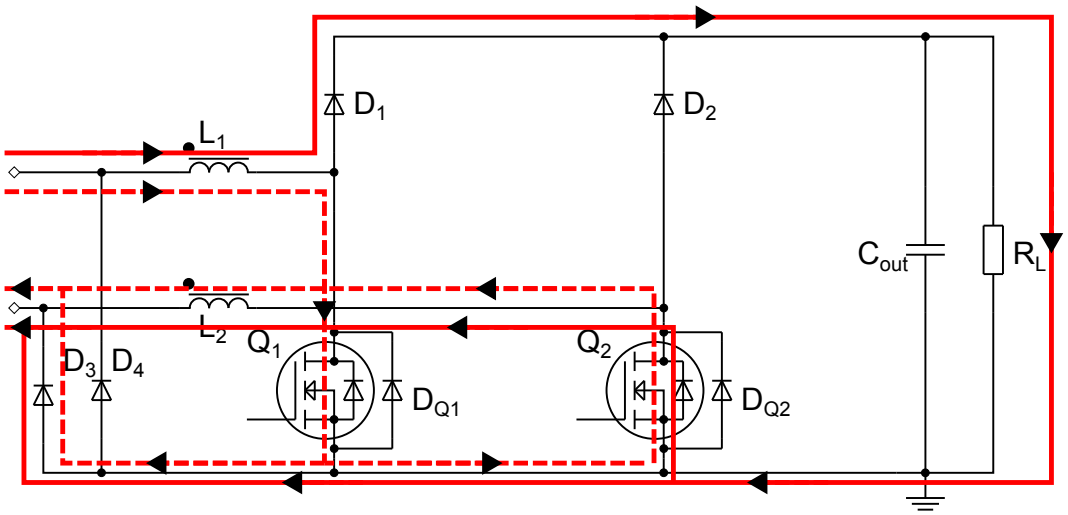


Fig. 5.2 Two-phase bridgeless corrector (cell 1 - active).

voltage. It is not suitable for the most of the APFC control circuits which need to measure the input voltage to the reference ground. The second one is a measuring of the inductor current. The last one is generation of the excessive noise due to the high dV/dt. It is caused by the voltage change from 0 volts, when the transistor Q_2 is switched on, to $V_{(in,max)}$, when the transistor Q_1 is switched on [33], [18].

The bridgeless corrector with two identical cells solves all issues. Each cell includes inductor, diode,and grounded transistor. If the positive voltage on terminal A is present (5.2), the diode D_4 is closed, the diode D_3 conducts and connects the B terminal to the common ground. The first cell is active, the second one is inactive. If the negative voltage on terminal A is present, the situation is vice versa.

A considerable amount of the current flows through the $D_{Q1,2}$ diodes that complicates a sensing of the current through the converter. It is caused by a low impedance of the inductor and body diodes of the transistors at line frequency. The current sensing is solved by a combination of the resistor connected between the common ground and anodes of the diodes D_3, D_4 and a couple of the current sense transformers which is connected between the drain of the transistors and the boost inductors. Three current sense transformers are other possibility. The bridgeless topology is suitable for medium and high power APFCs [33], [32], [26], [18].

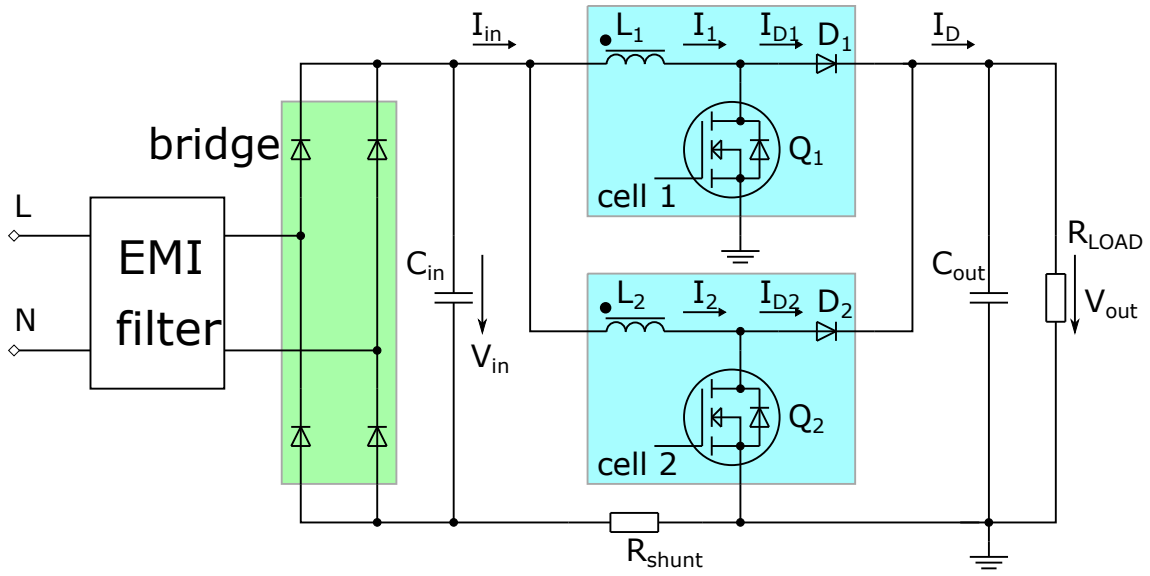


Fig. 5.3 Schematic diagram of the two-phase interleaved corrector.

5.2 Interleaved Topology

The interleaved corrector connects two or more single correctors into one. Each branch operates out of the phase of other one. This topology is often used in the cases where it is required a flat profile of the designed APFC. Therefore the interleaved correctors are suitable for notebook adapters and LCD televisions or monitors. The simple boost corrector operates under frequency clamped critical conduction mode (FCCrM) is used up to $300W$. Two-phase interleaved converters expand the operation range up to $600W$. The correctors which operate under CCM enhance the operation range to more than $2kW$ of the input power. Two-phase interleaved correctors decrease significantly input ripple current and input peak current which is half in comparison to single phase correctors. Total losses of the interleaved and single phase correctors are almost identical [33].

An interleaving improves a dissipation of the losses into more power components. Other advantage is using smaller or less powerful components. Interleaved correctors extend significantly an utility range of the FCCrM. An advantage of FCCrM is good efficiency of the corrector and lower costs due to no expensive SiC boost diode, smaller inductor and cheaper transistor [33], [12], [58], [24], [19].

If the corrector cells operate out of phase, the input ripple current is dramatically reduced (the figure 5.4). The line current waveform is similar to the CCM waveform. An output capacitor current is reduced as well. Thanks to this feature the capacitor can be replaced by another one with a smaller capacitance, volume, and price [33].

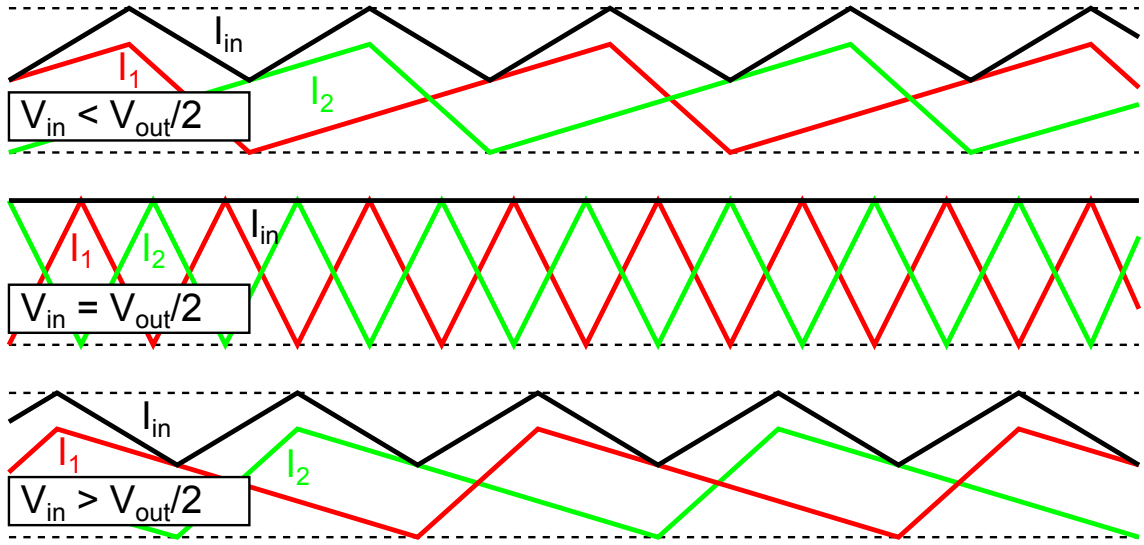


Fig. 5.4 Input ripple current cancellation.

Each corrector cell is phase shifted by 180° to each other for a reducing of the ripple current. An out-of-phase switching is crucial for the ripple current cancellation of correctors operated under CrM or FCCrM modes. The interleaving requires a precise timing of the control system. The "Master-slave" control technique is one possible solution. The master branch works normally as a single corrector, the slave one is phase shifted by 180°.

Another solution is described in the figures 5.5 and 5.6. Both corrector branches work independently under CrM or FCCrM respectively. A control of the switching is based on a tracking of the triangular V_{osc} signal. If the signal crosses the V_{TH} threshold value during the falling edge, the signal $CLK1$ or $CLK2$ is generated [33], [12], [58], [19].

Discontinuous Conduction Mode

The ferromagnetic core is demagnetized during the signals $CLK1$ and $CLK2$. The inductor current drop to zero and the new switching cycle can immediately begin [33].

Critical Conduction Mode

In this mode, the ferromagnetic core is not demagnetized during clock signals. If the signal $CLK1$ or $CLK2$ respectively is high, the inductor current is still flowing. The continuous conduction mode is characterized by a closing of the transistor when the clock signals are high. Under critical conduction mode, the transistors get close when the CLK signals are changed from high to low, that is when the inductor current goes to zero. The pulse duration is identical for each branch. The demagnetization period t_{demag} (5.4) [33] is dependent on

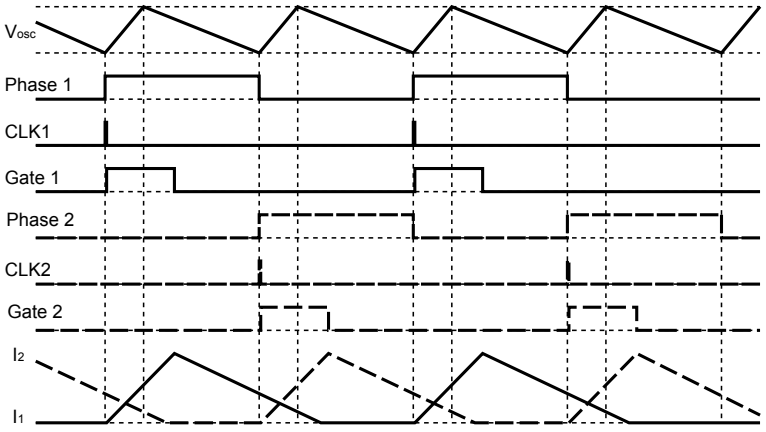


Fig. 5.5 Diagram of the discontinuous conduction mode.

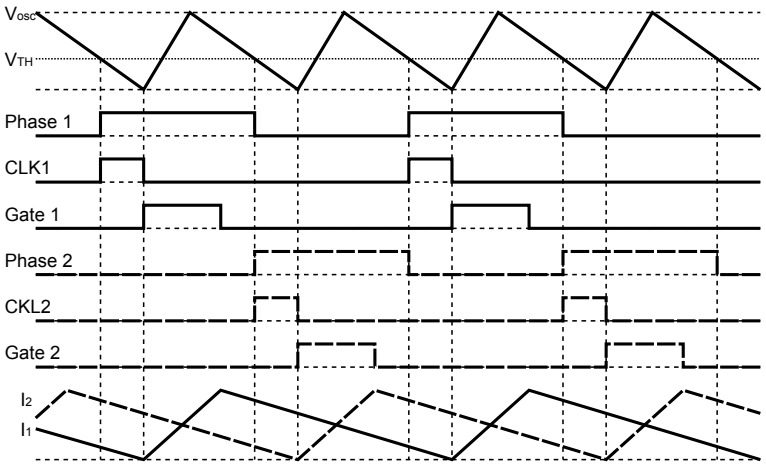


Fig. 5.6 Diagram of the critical conduction mode.

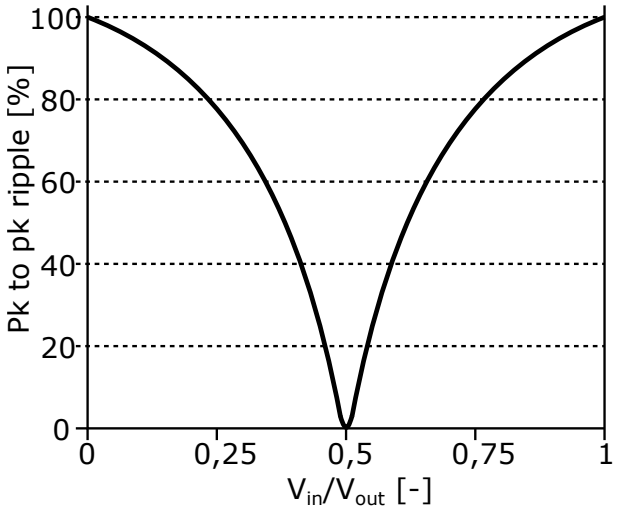


Fig. 5.7 Input current ripple.

the t_{on} pulse duration, input voltage, and output voltage [33].

$$t_{demag} = t_{on} \cdot \frac{V_{in}}{V_{out} - V_{in}} \tag{5.4}$$

The inductor currents are same in the case of a neglecting of the induction and time tolerances but they are phase shifted by 180°. A possible imbalance is determined by the equation (5.5) [33]:

$$\frac{I_1}{I_2} = \frac{L_2}{L_1} \tag{5.5}$$

The basic schematic diagram shows a parallel connection of two single phase correctors (5.3). I_1, I_2, I_{D1}, and I_{D2} current waveforms are same as the single phase corrector current waveforms. Each individual branch creates a same ripple current which is equivalent to the ripple current of single phase correctors. However, a total input ripple current and a diode ripple current are substantially suppressed due to the out of phase operation [33].

A principle of the ripple current cancellation is shown in the figure 5.4. If the input voltage equals to one half of the output voltage, the ripple current equals to zero. An opposite situation occurs when the input voltage is zero or when it reaches the output voltage value [33], [11], [19].

When the phase shift between branches is 180° and $\frac{V_{in}}{V_{out}} > 0.5$, the next equation determines the input ripple current.

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{2 \cdot \frac{V_{in}}{V_{out}} - 1}{\frac{V_{in}}{V_{out}}} \tag{5.6}$$

If the expression $\frac{V_{in}}{V_{out}} < 0.5$ is valid, the equation 5.7 [33] defines the input ripple current.

$$\frac{\Delta I_{in(pk-pk)}}{I_{in}} = \frac{1 - 2 \cdot \frac{V_{in}}{V_{out}}}{1 - \frac{V_{in}}{V_{out}}} \tag{5.7}$$

If both branch intervals are not overlaid, the maximal value of the line current (when the line voltage is minimal) can be computed by the following relation (5.8) [33], [19].

$$I_{line} = \sqrt{\frac{16\sqrt{2} \cdot P_{out}^2}{9\pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2}} \tag{5.8}$$

The I_{line} current value goes down by 30% in comparison with the single phase corrector. The output capacitor current drops even by 50%. The output capacitor current is derived by the equation 5.9 [33], [19].

$$I_{Cout} = \sqrt{\frac{16\sqrt{2} \cdot P_{out}^2}{9\pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}^2\right)} \tag{5.9}$$

For conventional single phase converter it is defined by the next equation (5.10) [33], [19].

$$I_{Cout} = \sqrt{\frac{32\sqrt{2} \cdot P_{out}^2}{9\pi \cdot V_{acLL} \cdot V_{out} \cdot \eta^2} - \left(\frac{P_{out}}{V_{out}}^2\right)} \tag{5.10}$$

The interleaved correctors are perspective type of APFC. They can be used for correctors with a flat profile, NTB adapters, and LCD power supplies [33], [19].

5.3 Analog vs Digital Control

Analog control circuits offer a simply compact solution for the power factor correction 5.8. Analog control circuits require a minimal count of external components. A design of the correctors is simple and features are quite good. The main drawbacks of the analog control circuits are fixed control technique and parameters, no data logging capability, and limited adaptability to power line variations and load changes.

The vast majority of analog circuits use the average current control. Advantages are small outline package of the control circuits, minimal number of the external components, low cost, and fast application development. The $UCC28180$ is a typical analog control circuit which has a 8-pin outline package and integrated $1.5A$ peak gate output. Therefore the circuit does not need any external power driver. The controller operates under the average current control

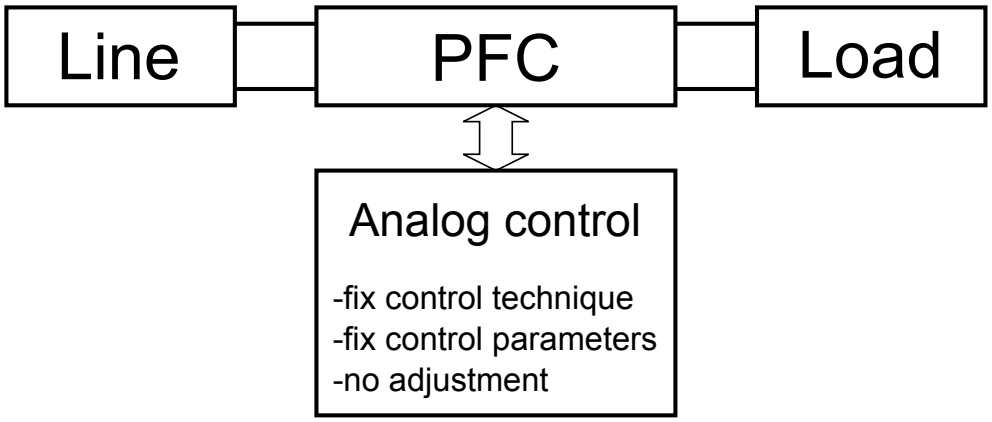


Fig. 5.8 Block diagram of the analog control.

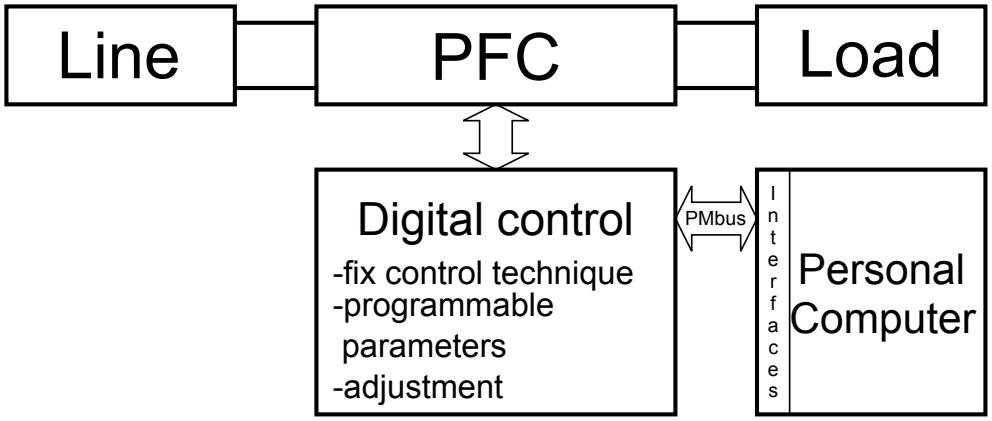


Fig. 5.9 Block diagram of the digital control.

without an input voltage sensing which reduces a count of external components. The current sensing requires only a small-value shunt resistor [54].

Consequently, the power dissipation is very low which is important for high power correctors. The switching frequency is variable from $18kHz$ to $250kHz$. Additionally, the controller contains over current and over voltage protection, under voltage lock out and open loop detection [54].

Digital control circuits customize correctors to the specific application. A compensation can be adjusted depending on power line or load conditions. Digital control circuits are usually equipped by communication interfaces. They offer calibration features, trimming, fault monitoring, etc.

Digital control circuit representatives are *ADP*1047 and enhanced version *ADP*1048. The *ADP*1047 allows to work in single phase operation, *ADP*1048 is designed for interleaved or bridgeless operation. Both versions have an advanced input power metering capability, inrush current control, frequency range from $30kHz$ to $400kHz$, output voltage adjustment,

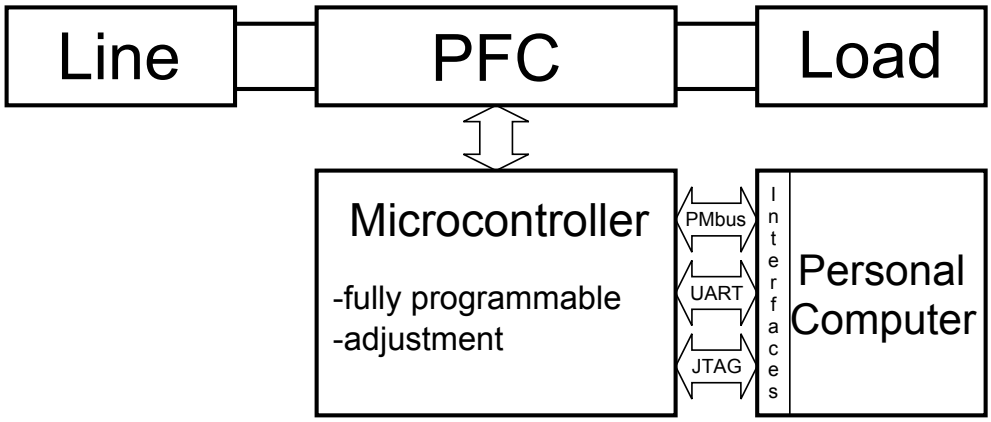


Fig. 5.10 Microcontroller control system.

switching frequency spread spectrum for improved EMI. The average current control is used for a controlling PF correction [2].

The control technique is not changeable. A programming is carried out by a graphical user interface. APFCs are usually based on the conventional single boost topology which has a programmable loop compensators for the optimum harmonics reduction. Analog signals are converted into digital number via internal ADCs. Parameters can be adjusted and reported by PMbus. This feature improves performance across a wide range of loads and input line voltages [2].

Digital control provided by programmable microcontrollers allow to design an user control program which can be more innovative and optimize a corrector performance. There are special microcontrollers which are designed for the power converter control. They are equipped by lots of peripherals, timers, comparators, ADCs, communication interfaces, and digital power peripherals. Advantages of these microcontrollers are fully programmable digital controller, data logging capability, control loop optimization, communication interfaces, multi-channel controller, password protected control program, program debugging. Disadvantages are complex control system, expensive, higher power consumption of the control circuits, longer implementation time [2].

The $UCD3138$ microcontroller is a suitable candidate for the fully programmable APFC. It is a digital controller which is appropriate for lots of topologies. Supported topologies are active clamp forward converters, two switch forward converters, hard switched full bridge and half bridge converters, single APFCs, interleaved APFCs, bridgeless APFCs and LLC half and full bridge converters. The microcontroller is based on a 32-bit $ARM7TDMI-S$ RISC architecture [55], [49].

The major controller equipment are digital power peripherals. They provide high speed control loops. These peripherals consist of dedicated error analog to digital converters, digital

compensation filters and digital PWM outputs. The controller includes a 12-bit general purpose ADC with 14 channels, several timers, communication ports and interrupt subsystem [55], [49].

The microcontroller includes several special features as a light load burst mode, synchronous rectification, LLC and phase shifted full bridge switching mode, input voltage feed forward, copper trace current sense, ideal diode emulation, constant current and power control, peak current mode control, flux balancing, current sharing, soft start, and others [55], [49].

Chapter 6

Prototypes and Measurement Setup

6.1 Design of Prototypes

This chapter consists of basic functional subsystems which are used in all designed correctors. These subsystems provide power supply, soft-start, and discharge of the output bulk capacitor. Other part of the chapter is devoted to measurements which were performed on corrector prototypes. The part includes general information, connection description, standards, etc. Experimental result are presented in following chapters.

6.2 Power Supply Subsystem

The power supply circuitry is usually provided by an auxiliary winding of the downstream converter. Due to the absence of this converter, it was used an additional power supply. In this cases there are three possible solutions. First of them is auxiliary winding on the power inductor of the corrector. This solution is combined with suitable current control which also use current transformer. This choice is cheapest one due to the minimal component count. However, the circuitry reaches only limited accuracy of the supply voltage regulation. Next two possibilities are intended especially for laboratory correctors which are stand alone (without downstream converter). First one uses isolated Flyback converter and second one uses Buck converter which can be supplied directly from rectified AC line or from the output of the corrector, i.e. from a bulk capacitor voltage. It was chosen the non-isolated Buck converter which is powered directly from AC line by a separate bridge rectifier 6.1 [35].

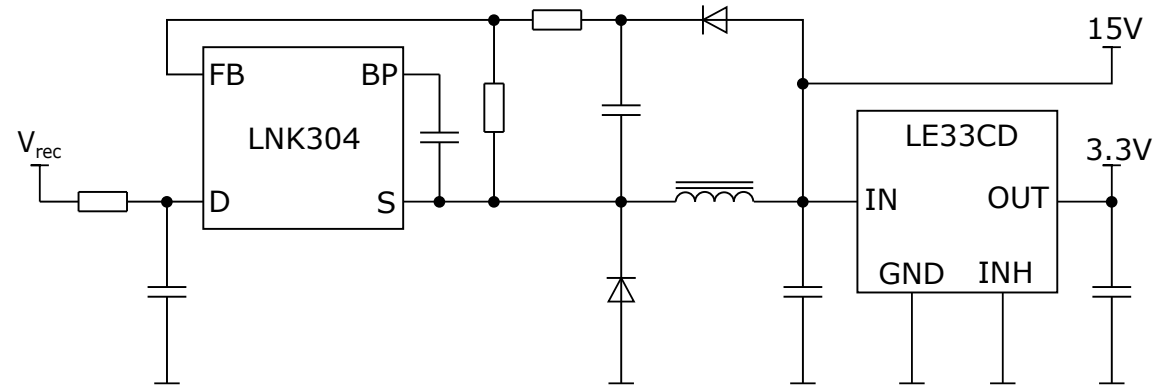


Fig. 6.1 Schematic diagram of the power supply.

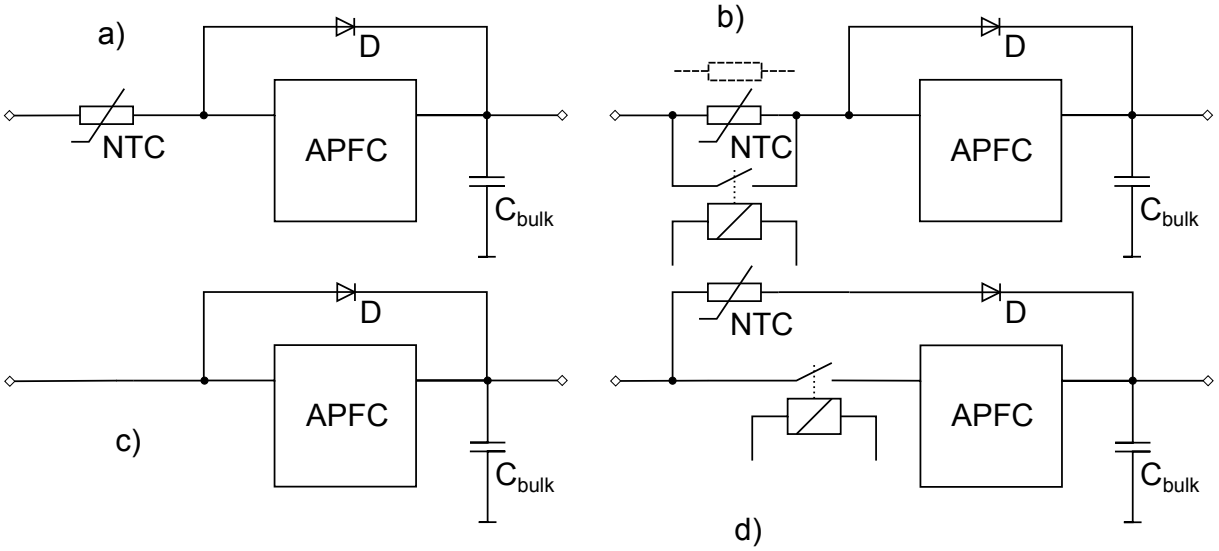


Fig. 6.2 Schematic diagrams of the inrush current limiters.

6.3 Soft-start Subsystem

If the corrector is connected to the line, the bulk capacitor is charged by significant inrush current. Its value exceeds several times the nominal current value. There are several inrush current limitation methods. The easiest way is using a NTC thermistor which is characterized by a high resistance when it is in cold state and low resistance at the hot condition. When the corrector is connected to the mains, the inrush current is significantly reduced due to the high resistance of the thermistor. The high resistance of the thermistor leads to increase the thermistor temperature. The resistance drops to a low value and a negative feedback stabilizes the temperature of the thermistor [54]. There are several connections one of them uses a classical wire-wound resistor with a timer relay, NTC thermistor with a timer relay and a standalone NTC thermistor.

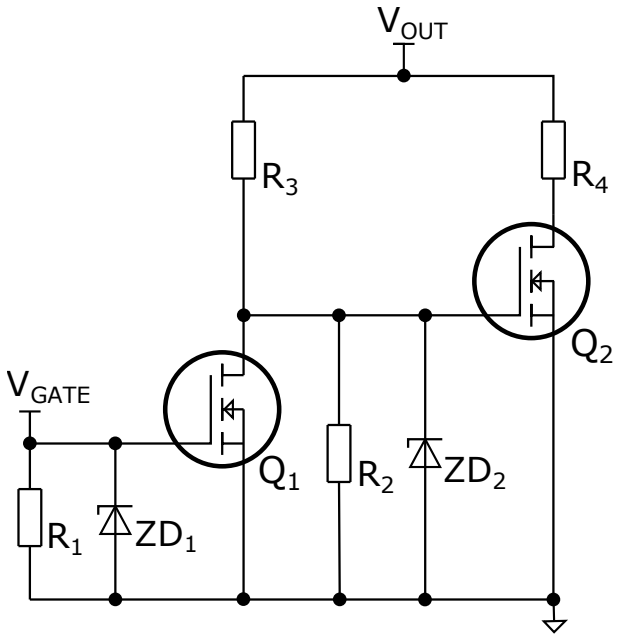


Fig. 6.3 Schematic diagram of the bulk capacitor discharge circuitry.

6.4 Bulk Capacitor Discharge Circuitry

The bulk capacitors represents a massive energy storage which is essential for proper function of the APFC. The bulk capacitors are charged during operation of the corrector at 390 VDC. This high voltage conditions is life dangerous, for safety and legal reasons the energy stored in the capacitors shall be discharged in determined time. The time is specified in the regulations which are subject to set important features of the switching converters.

There are several discharging circuits. The simplest solution is made of resistor or resistors which is connected in parallel with bulk capacitor. This solution is simple, cheap and reliable. However, the disadvantage is high power losses at the normal operation and long discharging time. The value of the resistors shall be selected as a compromise between fast discharging time and acceptable losses. In the practise the discharging resistor is still the most favourite solution.

In spite of this fact, an active discharge circuit brings many advantages. The schematic diagram of the active discharge circuit is shown on the figure 6.3. The circuit is deactivated when the line voltage is present ($V_{GATE} = 15V$), i.e. when the corrector is in the normal operational conditions. Therefore the losses are during the normal operation significantly reduced.

When the line voltage is not present the Q_1 transistor is opened. Thanks to this condition the current flows through the R_3 and R_2 resistors and ZD_2 diode. The current creates a

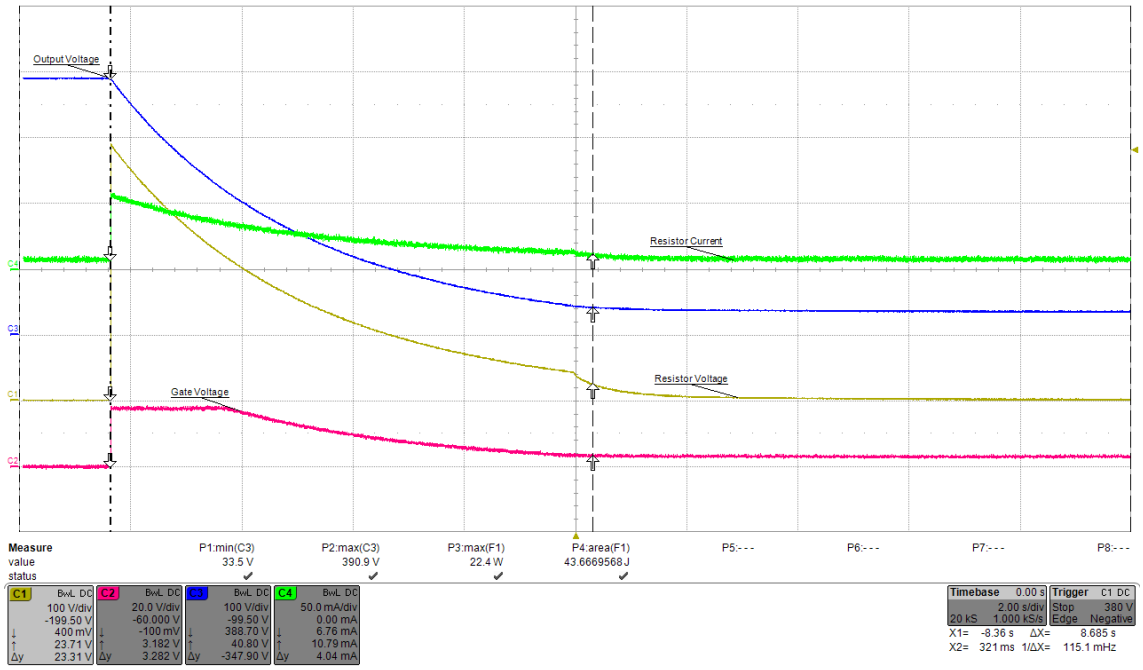


Fig. 6.4 Waveforms of the discharge transient (blue: output voltage, green: resistor current, yellow: resistor voltage, pink: gate voltage of Q_2).

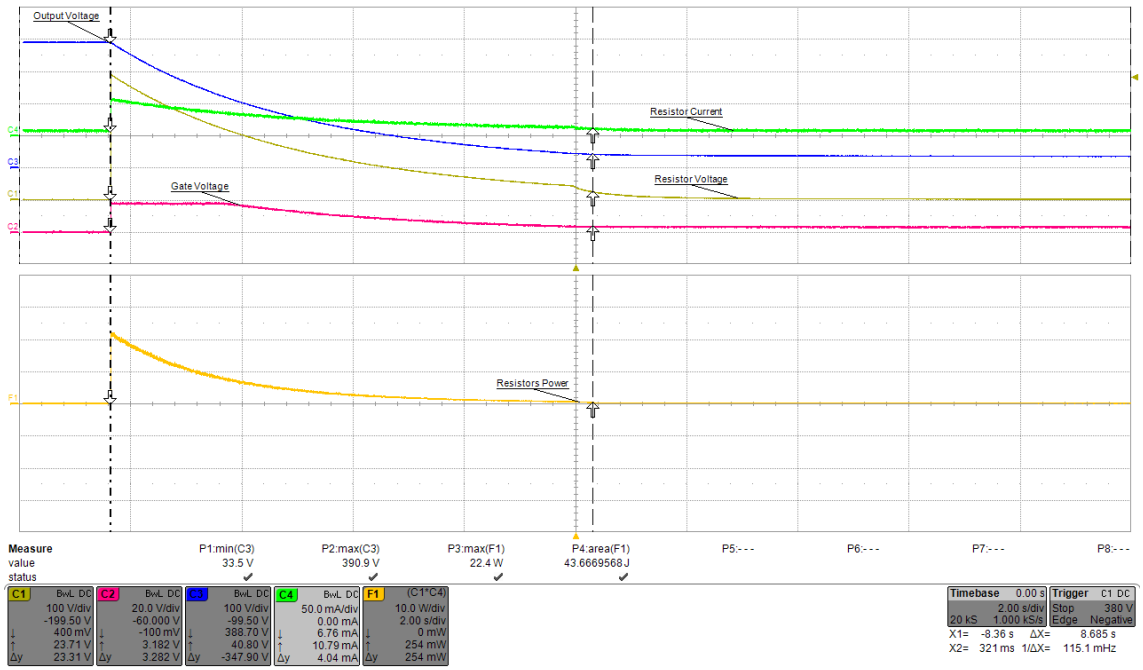


Fig. 6.5 Waveforms of the discharge transient (blue: output voltage, green: resistor current, yellow: resistor voltage, pink: gate voltage of Q_2), orange: resistor power.

sufficient voltage drop across the R_2 resistor for a opening of the Q_2 transistor. The ratio between resistors is set so that a final voltage on the capacitors after a remission of the transient condition would be $50V$ which is a life safe value. The advantages are a faster discharging time and minimal losses during normal operation of the corrector.

The experimental results were obtained from a single Boost corrector. As 6.4 and 6.5 figures show that the discharging time is approximately $10s$ which is a sufficient result. The figures give information about final output voltage which is $33.5V$. A maximal dissipative power of the resistors was measured $22.4W$. The dissipative energy during transient was $43.66J$. As dissipative components were used four parallel resistors with $5W$ power rating which is sufficient due to short discharging duration.

6.5 Performance Measurement

A performance measurement was carried out according to the block diagram 6.6. An input voltage for the corrector is provided by variable transformer with galvanic isolation. The variable transformer allows change the line voltage to $110V$. The APFC was tested at $110V$ and $230V$ due to the line voltages of the different countries [33].

The power quality analyser $HIOKY3198$ was connected between the variac transformer and APFC. The power quality analyser supports measurement of the individual harmonic amplitudes, power measurement and also PF, THD, etc. APFC was loaded by a resistive load which was created from serio-parallel connection of resistors with $10W$ rating. Each branch consists of 6 resistors, the number of branches is 18.

As a result the maximal power of the load was limited to $910W$. The switching of the individual branches was provided by a relay box. The resistive load requires an active cooling by the ventilator with a $240m^3/h$ air flow.

The measurement begins to set the input voltage to $110V$. After then, the resistor load was increased step by step to a rated output power of the corrector. The same approach was applied also for $230V$ input voltage. The input power was measured by the harmonic analyser as well as PF. The output voltage and current were measured by the digital multi-meters.

The efficiency of the corrector was calculated by the equation 6.1. PF data was obtained directly from the $HIOKY3198$ harmonic analyser.

$$\eta = \frac{V_{OUT} \cdot I_{OUT}}{P_{IN}} \cdot 100[\%] \tag{6.1}$$

The data obtained during the measurement was post-processed into two graphs. The first one depicts the dependence between efficiency and input power. The second one shows the

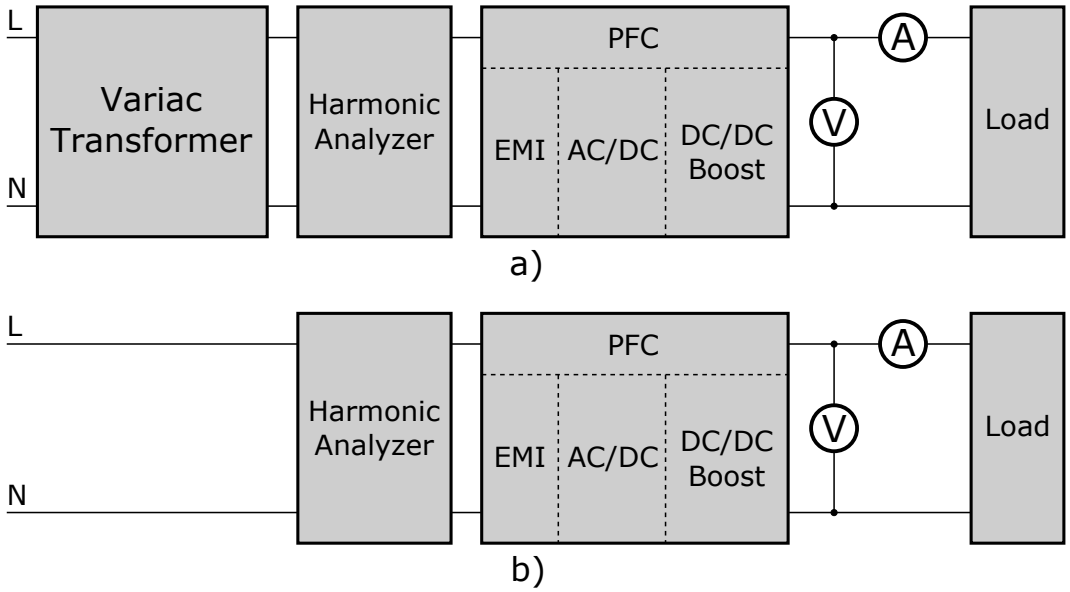


Fig. 6.6 Block diagram of the performance measurement.

PF correction performance during the measurement. Each curve is for different input voltage thereby the two line conditions were emulated.

6.6 Harmonic Content According to ČSN EN 61000-3-2 Standard

As part of the performance measurement is a harmonic content of the input current. The harmonic content of the line current was measured by the power quality analyser *HIOKY*3198. The analyser provides a table of current amplitudes of the harmonic order. The investigation was applied for three different power levels $100W$, $300W$ and $500W$. The power levels was used for each examined corrector. The measurement process started a setting the resistive load to an appropriate value for the examined power. Comparable data was provided by a launch of the analysis on the power quality analyser. Measured data includes a table of amplitudes which were compared with permissible current limits.

The standard defines four classes for electrical equipment. The experimental results were compared with limits defined in a *D* class which includes personal computers, televisions, etc. The *D* class has the most strict current limits. The class defines two limits for a line current. First one is permissible current per watt which was used for comparison with measured data due to this value reflects the power. In other words, the limit is dependent on the power [42].

Second limit defines a maximal permissible harmonic current which is constantly greater than the previous one. As a result, the column graph with the limits was compiled. The amplitudes of the current is summed in the table 6.1 [42].

Table 6.1 Table of the limits defined according to EN 61000-3-2 2006 standard.

Harmonic order Current limit n	Permissible current per watt [mA/W]	Permissible harmonic current [A]
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13	0.296	0.2100
15	0.257	0.1500
17	0.226	0.1324
19	0.203	0.1184
21	0.183	0.1071
23	0.167	0.0978
25	0.154	0.0900
27	0.143	0.0833
29	0.133	0.0776
31	0.124	0.0726
33	0.117	0.0682
35	0.110	0.0643
37	0.104	0.0608
39	0.099	0.0577

6.7 EMI Conductive Measurement

Electronic device have to meet EMI limits which are defined in the ČSN EN 61000-6-4 [44] or ČSN EN 61000-6-3 [43] standards. The standards define quasi peak and average limits for commercial and industry devices as well. The measurement was performed in the certified EMC laboratory. LISN was connected to the line. The artificial network provides a power output for DUT and measuring output which is connected to the spectrometer.

As a measuring equipment was used Rohde and Schwarz spectrometer. DUT was placed on the wooden table, the input was connected EMI filter and the output to a resistive load. The load was set to $500W$ output power. The Schaffner filter [40] terminals was connected to

the artificial network. The chassis of the filter was pressed on the copper sheet as well. This connection emulates a conductive connection between them inside a case.

The grounding issue of the measurement plays a crucial role on the experimental results. A grounding between the artificial network, filter and DUT can be provided several ways. The grounding solved by the flexible cable are suitable for testing devices which has no additional grounding point on the chassis. The grounding only via flexible cable bring worse emission result at the highest frequencies due to a high impedance of the cable copper core. When the device has dedicated grounding point on the chassis, the connection shall be provided by a wide conductor which represents a lower impedance for high frequency currents. The grounding between the artificial network and DUT was provided for all measurement by the flexible cable.

6.8 Thermal Measurement

An evaluation of the prototypes contain a thermal analysis which helps to determine a maximal available output power. The thermal images were performed by a *FLIR* infra-camera. The thermal images of each APFC include 4 figures when the active cooling is enabled and the same number of pictures at the passive cooling.

The process is composed of two levels of the scanning. Overall view of the prototype helps to recognise a source of the heat. The particular thermal images are focused on the components which have a higher temperature and power losses as well. An attention was paid to a bridge rectifier, NTC thermistor, power MOSFETs, boost diodes and power inductors.

Chapter 7

Single Boost Active PFC

The first prototype is based on the single Boost topology which is controlled by a specialized control circuit $UCC28180$.

The controller $UCC28180$ is a power factor controller with Average Mode Control technique. The current shaping is provided without an AC sensing network. This solution eliminates a count of external components. The controller contains two control loops. The first one is wide band and provides the input current regulation. The current loop does not use the reference source derived from the AC line voltage. The shaping reference source uses a harmonic oscillator. The compensation network shall be connected to the $ICOMP$ pin [54].

The second one serves the output voltage regulation. It has a slower response due to it has to be resistant to the line frequency ripple of the output voltage. As a reference it is used the $5V$ inner voltage source. The controller operates under CCM with the fixed switching frequency which can be set in a wide range from 18 to $250kHz$. The frequency depends on a value of the resistor connected to the $FREQ$ pin [54].

7.1 Power Stage Design

The selection of the power stage components is determined by a design requirements which are summarized in table 7.1.

First calculation 7.1 [54] find out the output current of the corrector at the nominal output power.

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}} = \frac{500}{390} = 1.282A \tag{7.1}$$

Table 7.1 Requirements for a prototype based on the UCC28180 controller.

Design Parameter	Min	Typ	Max	Unit
Line Voltage $[V_{line}]$	85	-	265	V
Output Voltage $[V_{OUT}]$	-	390	-	V
Line Frequency $[f_{line}]$	47	-	63	Hz
Switching Frequency $[f_{sw}]$	-	200	-	kHz
Output Power $[P_{OUT}]$	-	500	-	W
Efficiency at nominal power $[\eta]$	92	-	-	%

The input RMS current of the corrector is defined by next equation 7.2 [54] at the nominal output power $P_{OUT(max)}$, minimal line voltage $V_{IN(min)}$ and assumed power factor PF.

$$I_{INrms(max)} = \frac{P_{OUT(max)}}{\eta \cdot V_{IN(min)} \cdot PF} = \frac{500}{0.92 \cdot 85 \cdot 0.99} = 6.458A \tag{7.2}$$

In case of the inductor current ration should be used the peak value of the line current 7.3 [54].

$$I_{IN(max)} = \sqrt{2} \cdot I_{INrms(max)} = \sqrt{2} \cdot 6.458 = 9.133A \tag{7.3}$$

The average value of the input current is determined due to the sinus wave by following equation 7.4 [54].

$$I_{INavg(max)} = \frac{2}{\pi} \cdot I_{IN(max)} = \frac{2}{\pi} \cdot 9.133 = 5.814A \tag{7.4}$$

7.1.1 Bridge Rectifier

The bridge rectifier blocking voltage must overcome the maximal input voltage with voltage margin $100V$ at least. The maximal repetitive current of the rectifier have to handle inrush current during starting sequence. The dissipation power in the bridge rectifier is defined by equation 7.5 [54].

$$P_{BRIDGE} = 2 \cdot V_{F(bridge)} \cdot I_{INavg(max)} = 2 \cdot 0.95 \cdot 5.814 = 11.047W \tag{7.5}$$

7.1.2 Input Capacitor

Assuming of the input capacitor requires to define the input current ripple and high frequency input voltage ripple. The input current ripple ΔI_{ripple} is determined as 40% of the peak input

current value 7.6 [54].

$$I_{ripple} = \Delta I_{ripple} \cdot I_{IN(max)} = 0.4 \cdot 9.133 = 3.653A \tag{7.6}$$

The calculation of the high frequency voltage ripple requires the amplitude of the minimal line voltage which is defined as follows.

$$V_{INrectified} = \sqrt{2} \cdot 85 = 120.208V \tag{7.7}$$

The acceptable high voltage ripple is determined as 7% of the minimal line voltage amplitude [54].

$$V_{INripple} = \Delta V_{INripple} \cdot V_{INrectified(min)} = \Delta 0.07 \cdot 120.208 = 8.415V \tag{7.8}$$

The estimated capacitance of the input capacitor is based upon input current ripple I_{ripple}, high frequency voltage ripple $V_{INripple}$ and switching frequency as well.

$$C_{IN} = \frac{I_{ripple}}{8 \cdot f_{SW} \cdot V_{INripple}} = \frac{3.653}{8 \cdot 2e^5 \cdot 8.415} = 271.316nF \approx 270nF \tag{7.9}$$

The $270nF$ standard film capacitor was used with $275VAC$ voltage rating.

7.1.3 Boost Inductor

The inductor current rating is determined by a summing of the peak input current and the input current ripple divided by the factor 2 due to the input current ripple is superimposed onto the sinusoidal rectified input current. The equation 7.10 [54] defines the peak inductor current.

$$I_{Lpeak(max)} = I_{IN(max)} \cdot \frac{I_{ripple}}{2} = 9.133 + \frac{3.653}{2} = 10.95A \tag{7.10}$$

When the peak inductor current is defined, the minimal inductance can be found out by the next equation 7.11 [54].

$$L_{min} >= \frac{V_{OUT} \cdot D \cdot (1-D)}{f_{SW} \cdot I_{ripple}} >= \frac{390 \cdot 0.5 \cdot (1-0.5)}{2e^5 \cdot 3.653} = 133.452\mu H \tag{7.11}$$

If It is assumed the minimal inductance to $200\mu H$, the maximal inductor ripple current can calculated as follows [54].

$$I_{ripple(real)} = \frac{V_{OUT} \cdot D \cdot (1-D)}{f_{SW} \cdot L_{min}} = \frac{390 \cdot 0.5 \cdot (1-0.5)}{2e^5 \cdot 2e^{-4}} = 2.438A \tag{7.12}$$

The duty cycle is dependent on the instantaneous value of the line voltage and the nominal output voltage [54].

$$D_{MAX} = \frac{V_{OUT} \cdot V_{INrectified(min)}}{V_{OUT}} = \frac{390 \cdot 120.208}{390} = 0.692 \tag{7.13}$$

Based on the previous calculations it was selected the power inductor with $500\mu H$ maximal inductance. The current rating of the inductor reaches $12A$. The inductor is built on the $ETD44$ ferite core with a multicore copper winding.

7.1.4 Switching Element

The selection of the power transistor plays crucial role on the overall efficiency. The converter trend prefers MOSFET transistors for their fast switching times. The main parameters which have to be taken into account are a breakdown voltage, forward current, gate capacity, and maximal dissipative power. The breakdown voltage must be selected based on the maximal output voltage and voltage margin for the higher reliability. The margin reaches $100V$ at least but appropriate value is half of the nominal output voltage therefore are suitable transistors with 500 or $600V$ breakdown voltage. The higher breakdown voltages are also inappropriately due to higher R_{DSon} parameter. The second important parameter is a drain current through the transistor which is defined in the equation 7.14 [54].

$$I_D = \frac{P_{OUT(max)}}{V_{INrectified(min)}} \cdot \sqrt{2 - \frac{16 \cdot V_{INrectified(min)}}{3\pi \cdot V_{OUT}}} \tag{7.14}$$

When the numbers are inserted into previous equation, it is obtained particular drain current 7.15 [54].

$$I_D = \frac{500}{120.208} \cdot \sqrt{2 - \frac{16 \cdot 120.208}{3\pi \cdot 390}} = 5.053A \tag{7.15}$$

Based on the calculation was selected a $SPP20N60C3$ MOSFET transistor. The dissipative power of the transistor generates conductive and switching losses. The conduction losses 7.16 are determined by the multiplication of the $R_{DS(on)}$ at 125 °Cand the squared RMS drain current of the transistor [54].

$$P_{COND} = I_D^2 \cdot R_{DS(on)125} = 5.053^2 \cdot 0.4 = 10.213W \tag{7.16}$$

Equation 7.17 [54] shows an estimation of the switching losses based on rise time, fall time and output capacitance of the transistor [54].

$$P_{SW} = f_{SW} \cdot [0.5 \cdot V_{OUT} \cdot I_{IN(max)} \cdot (t_r + t_f) + 0.5 \cdot C_{OSS} \cdot V_{OUT}^2] \tag{7.17}$$

The estimation is based on the known parameters and transient waveform between the switching states. The dissipation energy has triangular shape [54].

$$P_{SW} = 2e^5 \cdot [0.5 \cdot 390 \cdot 9.133 \cdot (5e^{-9} + 4.5e^{-9}) + 0.5 \cdot 780e^{-12} \cdot 390^2] = 15.25W \tag{7.18}$$

Total losses are found by summing of conductive and switching losses 7.19 [54].

$$P_{TOTAL} = P_{COND} + P_{SW} = 10.213 + 15.25 = 25.463W \tag{7.19}$$

The parasitic parameters of the connection can cause an inappropriately behaviour of the corrector. The parasitic parameters should be eliminated by proper layout design. However, there is a gate resistor which provides a reduction of the ringing and decreases the switching losses in the driver. A resistivity is usually selected from 1 to 22Ω.

7.1.5 Boost Diode

An estimation of the boost diode losses 7.20 [54] are based on the same principles which were used in the switching transistor calculations. As a Boost diode it was used SiC diode ($C3D04060A$).

$$P_{DIODE} = V_{F125C} \cdot I_{OUT(max)} + 0.5 \cdot f_{SW} \cdot V_{OUT} \cdot Q_{RR} \tag{7.20}$$

$$P_{DIODE} = 0.9 \cdot 1.282 + 0.5 \cdot 2e^5 \cdot 390 \cdot 24e^{-9} = 2.0898W \tag{7.21}$$

7.1.6 Output Capacitor

A selection of the capacitor is characterized by an output power, allowed voltage ripple and hold up requirements. The capacitor hold up time is defined as follows $t_{HOLDUP} = 1/f_{linemin}$ and the hold up voltage is determined to $300V$ [54].

$$C_{OUT} = \frac{2 \cdot P_{OUT(max)} \cdot t_{HOLDUP}}{V_{OUT}^2 - V_{OUTHOLDUP(min)}^2} = \frac{2 \cdot 500 \cdot 21.28e^{-3}}{390^2 - 300^2} = 342.673\mu F \approx 470\mu F \tag{7.22}$$

The suitable current ripple of the corrector is determined as 5% of the output voltage.

$$V_{OUTRIPPLE} < 0.05 \cdot V_{OUT} = 0.05 \cdot 390 = 19.5V \tag{7.23}$$

The next calculation shows that the chosen capacitor with $470\mu F$ capacity fulfil the 5% requirement of the voltage ripple. The equation 7.24 verifies the value of the output voltage ripple [54].

$$V_{OUTRIPPLE} < \frac{I_{OUT}}{2\pi \cdot 2 \cdot f_{LINE(min)} \cdot C_{OUT}} = \frac{1.282}{2\pi \cdot 2 \cdot 47 \cdot 470e{-}6} = 4.618V \tag{7.24}$$

Besides the capacity of the capacitor is also important current rating of the capacitor. The current rating of capacitors is usually defined as low frequency and high frequency current rating. The low frequency current requirement is defined by the following equation 7.25 [54]. The current rating gives information about a filtering capability of the rectified line frequency [54].

$$I_{COUTLF} = \frac{I_{OUT(max)}}{\sqrt{2}} = \frac{1.282}{\sqrt{2}} = 0.907A \tag{7.25}$$

The high frequency current rating specify the high frequency filtering performance.

$$I_{COUTHF} = I_{OUT(max)} \cdot \sqrt{\frac{16 \cdot V_{OUT}}{3\pi \cdot \sqrt{2} V_{IN(min)}}} = 1.282 \cdot \sqrt{\frac{16 \cdot 390}{3\pi \cdot \sqrt{2} \cdot 85}} = 3.009A \tag{7.26}$$

The rating is sometimes defined as one parameter. The total RMS current is determined by next expression 7.27 [54].

$$I_{COUTRMSTOTAL} = \sqrt{I_{COUTLF}^2 + I_{COUTHF}^2} = \sqrt{0.907^2 + 3.009^2} = 3.143A \tag{7.27}$$

7.2 Timing

A choice of the suitable timing plays crucial role for the selection of other components. The selected switching frequency has influence on efficiency of the corrector and electromagnetic emissions interference. A equation for calculation of the R_{FREQ} timing resistor has a non-linear character which is shown in the equation 7.28 [54].

$$R_{FREQ} = \frac{f_{TYP} \cdot R_{TYP} \cdot R_{INT}}{f_{SW} \cdot R_{INT} + R_{TYP} \cdot f_{SW} - R_{TYP} \cdot f_{TYP}} \tag{7.28}$$

Inserting numbers and required switching frequency it is assumed the frequency setting resistor 7.29. The resistor value can be estimated also by a using of the graph from the datasheet [54].

$$R_{FREQ} = \frac{6.5e^4 \cdot 3.27e^4 \cdot 1e^6}{(2e^5 \cdot 1e^6) + (3.27e^4 \cdot 2e^5) - (3.27e^4 \cdot 6.5e^4)} = 10.397k\Omega \approx 10k\Omega \qquad (7.29)$$

7.3 Soft-start Circuitry

The controller includes also a soft start circuitry which handles a ramping function for a smooth increasing of the duty cycle. When the one fault condition or standby mode is present, the $VCOMP$ pin is pulled low.

The releasing of this conditions leads to a rapid driving of the $VCOMP$ pin to $1.5V$. After the this initial process, the driving is provided by a constant current source $40\mu A$ which provides the start-up ramp.

The ramp signal grows linearly up to 85%. The soft-start duration can be parametrized by the compensation network at the $VCOMP$ pin. The soft-start source is deactivated when the $VSENSE$ voltage reaches to of the 98% nominal value [54].

7.4 Protection Circuits

The controller contains several internal protection circuits. The protection circuits cover a supply under voltage lock-out, output over voltage protection, open loop protection at the voltage loop and current loop, open loop protection of the $ICOMP$ pin, under voltage protection at the output, and cycle-by-cycle over current protection [54].

7.4.1 Under Voltage Lockout

The under voltage lockout protects the device to low voltage supply voltage conditions. The protection is activated at the supply voltage drop to $9.5V$. The hysteresis gap is around two volts therefore the device is enabled at $11.5V$ [54].

7.4.2 Over Voltage Protection

The over voltage protection distinguishes two levels of protection. The first is activated when the voltage on the $VCOMP$ pin overcomes 107% of the nominal value. In this case, the

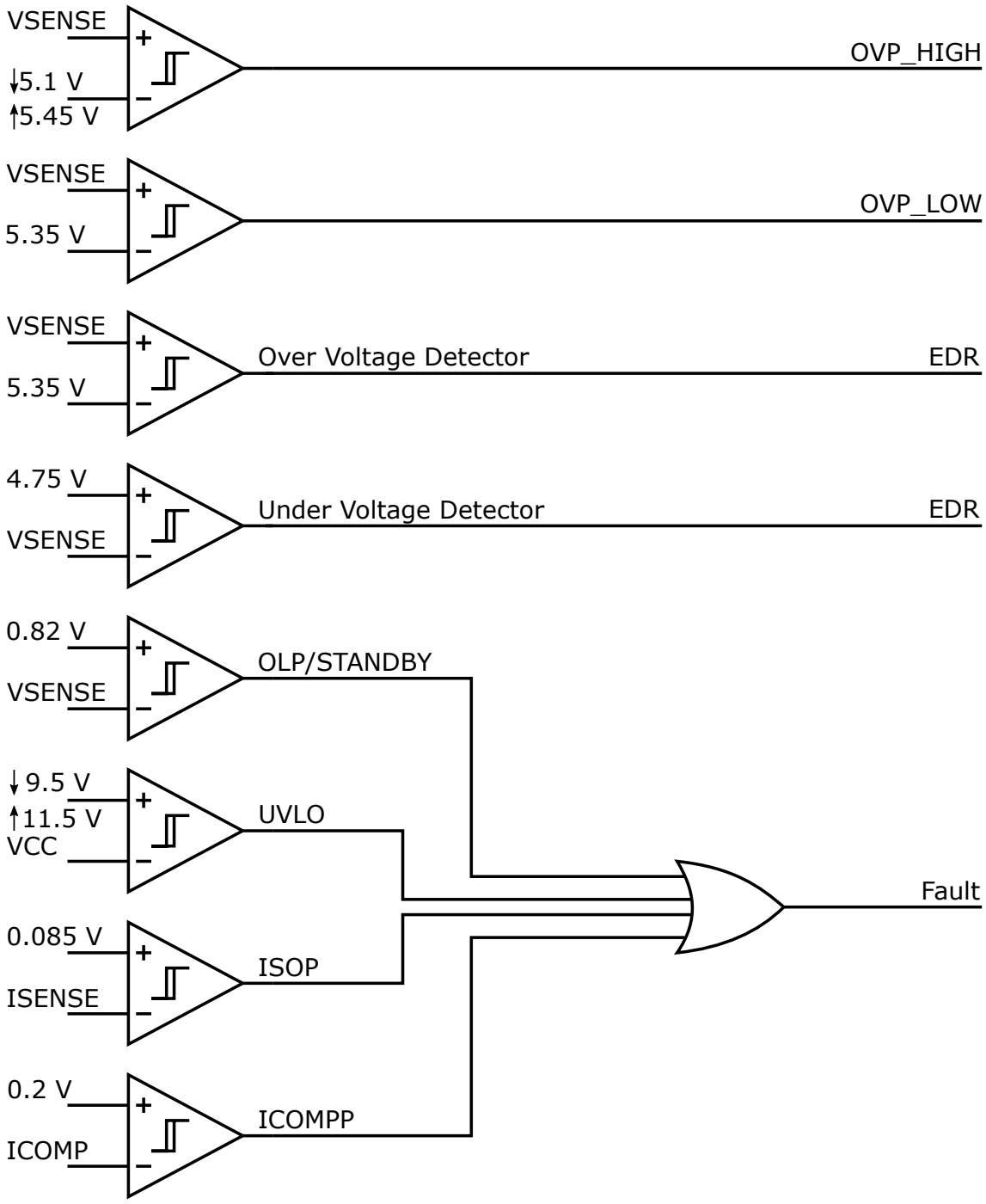


Fig. 7.1 Schematic diagram of controller protections.

VCOMP pin is pulled low. The second is enabled when the V_{SENSE} reaches 109% of the nominal value, the *GD* output is promptly disabled. Once the *VSENSE* voltage decreases to 102%, the *GD* output is enabled [54].

7.4.3 Open Voltage Loop Protection

When the voltage on the *VSENSE* pin is not present, the voltage error amplifier produces a maximal value of the error voltage. As a result, the *GD* output creates the PWM signal with maximal duty cycle. Therefore the controller is equipped by the open loop protection which protects the device against this situation. If the *VSENSE* voltage drops below $0.82V$, the controller is pulled to standby mode. The PWM generation is stopped and the current consumption decreases to $2.95mA$. This feature can be enabled also by an external switch which pulls the *VSENSE* pin to low [54].

7.4.4 Open Current Loop Protection

Similar situation exists at the *ISENSE* pin. When the voltage on the *ISENSE* pin is not present the internal pull-up resistor provides $0.085V$. This voltage causes a transition the device into standby mode. The *ICOMP* pin is also protected when the voltage drops below $0.2V$. The controller includes over voltage and under voltage protection of the output. If the output perturbation exceeds 5% of the nominal value, under voltage or over voltage are detected. Due to the slow response of the output voltage regulation EDR is activated and it speeds up the regular response. During the EDR the transconductance is increased by factor five and charging or discharging of the compensation network get faster. The EDR is disabled during a soft-start and fault conditions [54].

7.4.5 Over Current Protection

The over current protection uses a sensing of the inductor current by the R_{ISENSE} resistor which is connected between bridge rectifier and system ground. As a result, the voltage is negative. The signal is internally amplified by factor -2.5. Thanks to this the signal becomes positive and more suitable for the next processing. There are two levels of the protection which are a soft over current protection and cycle-by-cycle peak current limiter. The soft over current protection protects the corrector against an overloading. The soft over current does not disable the PWM output. When a voltage on the *ISENSE* pin exceeds the $-0.285V$ border, the error voltage amplifier output is pulled low by the $4-k\Omega$ resistor. As a consequence, the voltage loop setting is changed so that the duty cycle decreases.

The cycle-by-cycle peak current limiter allows to avoid the saturation of the power inductor. The hard protection is activated when the voltage on the *ISENSE* pin overcomes $-0.4V$. The activation of the peak current limiting causes the turn off the PWM output. An enhanced noise immunity is provided by the feature of the protection which is leading edge blanking [54].

The value of the current sense resistor must correspond to the soft over current protection threshold. Whereas, the triggering of the protection under normal operation is permissible. The resistor has to withstand the 10% overloading of peak current [54].

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{Lpeak(max)} \cdot 1.1} = \frac{0.259}{10.96 \cdot 1.1} = 0.021\Omega \approx 22m\Omega \tag{7.30}$$

The power rating of the current sense resistor is computed at the low line by the next equation 7.31 [54].

$$P_{RSENSE} = I^2_{INrms(max)} \cdot R_{SENSE} = 6.458^2 \cdot 0.022 = 0.918W \tag{7.31}$$

If the voltage across the current sense resistor increases over the peak current limit, the peak current limitation is activated and it is given by next equation 7.32 [54].

$$I_{PCL} = \frac{V_{PCL(max)}}{R_{SENSE}} = \frac{0.438}{0.022} = 19.9A \tag{7.32}$$

The voltage on the pin *ISENSE* is limited by the clamp diode to the range 0 to -1.1 volts. The clap diode provides the protection of the *ISENSE* input during the non-standard operation (inrush current) [54].

7.5 Gate Driver

The gate driver 7.2 should have a capability of the driving of a source-gate capacitance of the power MOSFETs or IGBTs owing to short transition times. Due to the fact that the most of the power MOSFETs have the maximal source-gate voltage limited to $20V$, the gate drivers are clamped typically at $15.2V$. If UVLO is activated, the gate driver is disabled.

The connected gate resistor helps for a ringing reduction which is caused by the parasitic inductance of the traces and the source-gate capacity of power transistors. The resistor is used for rise and fall time limitation. As a consequence, EMI is also reduced. The resistor allows to eliminate losses in the driver. The gate of the transistor is recommended to pull down by the $10k\Omega$ resistor [54].

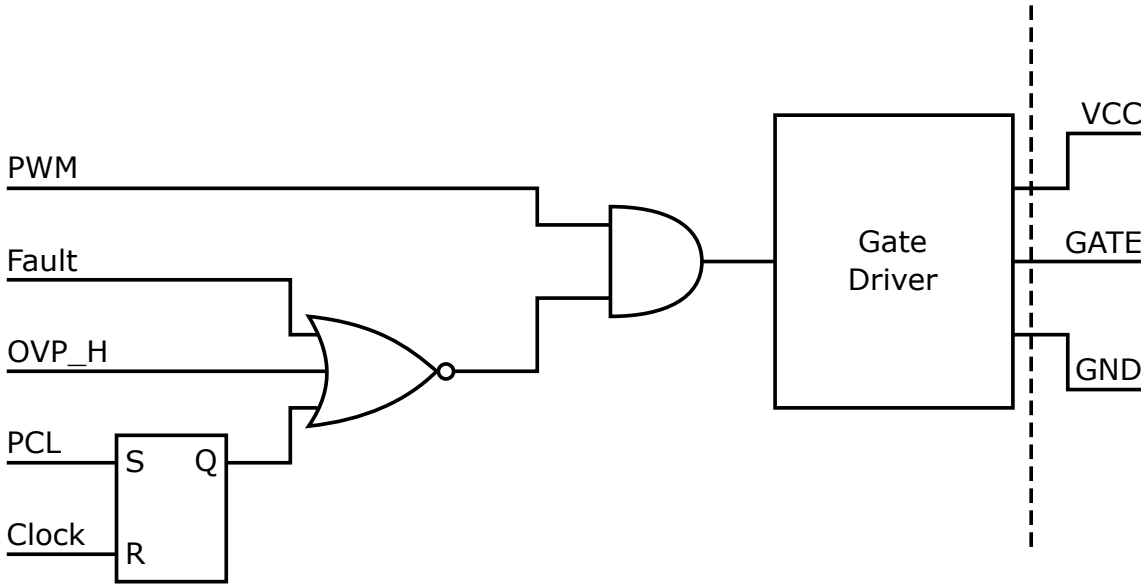


Fig. 7.2 Schematic diagram of the gate driver.

7.6 Output Voltage Set Point

The output voltage is set to $390V$ according to the next equation 7.33 [54].

$$R_{FB2} = \frac{V_{REF} \cdot R_{FB1}}{V_{OUT} - V_{REF}} = \frac{5 \cdot 1e^6}{390 - 5} = 13.04k\Omega \approx 13k\Omega \tag{7.33}$$

When the output voltage overcomes by 5% of the nominal value, the over current protection is activated. The transconductance of the amplifier is immediately increased. It causes fast decreasing of the output voltage under the regulated value. The threshold for sensing pin can be computed by the following equation 7.34 [54].

$$V_{OVD} = 1.05 \cdot V_{REF} = 1.05 \cdot 5 = 5.25V \tag{7.34}$$

The output voltage has to reach the voltage specified in the equation 7.35 [54] so that the soft over voltage protection can be activated.

$$V_{OUTovd} = V_{OVD} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = 5.25 \cdot \frac{1e^6 + 1.3e^4}{1.3e^4} = 410.7V \tag{7.35}$$

If the transient event causes the output voltage overshoot which exceed by 9% of the nominal voltage level, the hard over voltage protection will be activated. A voltage threshold of the hard over voltage protection is estimated as follows (the equation 7.36 [54]).

$$V_{OUTovp} = 1.09 \cdot V_{REF} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = 1.09 \cdot 5 \cdot \frac{1e^6 + 1.3e^4}{1.3e^4} = 426.4V \tag{7.36}$$

The under voltage protection is computed by the following equation 7.37 [54].

$$V_{OUTuvp} = 0.95 \cdot V_{REF} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = 0.95 \cdot 5 \cdot \frac{1e^6 + 1.3e^4}{1.3e^4} = 371.6V \tag{7.37}$$

A voltage of the divider is affected by a noise therefore it should be applied an appropriate filter capacitor. The filter should have up to $10\mu s$ time constant which does not crucial affect on a response time of the voltage control loop. It was selected a standard capacitor with $680pF$ value which was estimated by the expression 7.38 [54].

$$C_{VSENSE} = \frac{\tau}{R_{FB2}} = \frac{1e^{-5}}{1.3e^4} = 769pF \approx 680pF \tag{7.38}$$

7.7 Current Loop

The current loop includes three main parts which are power stage with current sense resistor, current error amplifier stage, and pulse width modulator 7.3.

A voltage drop across the current sense resistor has a negative value. The signal is internally inverted and averaged by a current error amplifier. The *ICOMP* pin is connected to the output of the error current amplifier. The signal at this output represents the average inductor current.

The compensation is provided by the external capacitor connected to the *ICOMP* pin. A gain of the transconductance amplifier is not linear. It is controlled by the *VCOMP* voltage. When one of the inadequate mode is activated the $3V$ voltage source is connected to the input of the amplifier [54].

A PWM modulator is responsible for PWM generation which is amplified by the gate driver. A main aim of the modulator is a creation of the PWM signal for the transistor. The modulator compares the *ICOMP* voltage with the periodic ramp signal.

As a result, the leading edge of the modulated signal is produced which is high in case of the ramp signal overcomes the voltage on the *ICOMP* pin. The slope of the ramp signal depends on the *VCOMP* voltage and it is non-linear.

The PWM signal begins always at low, the internal clock is used as a trigger. The signal remains low at least a minimum off-time. After, the off-time period of the ramp signal grows

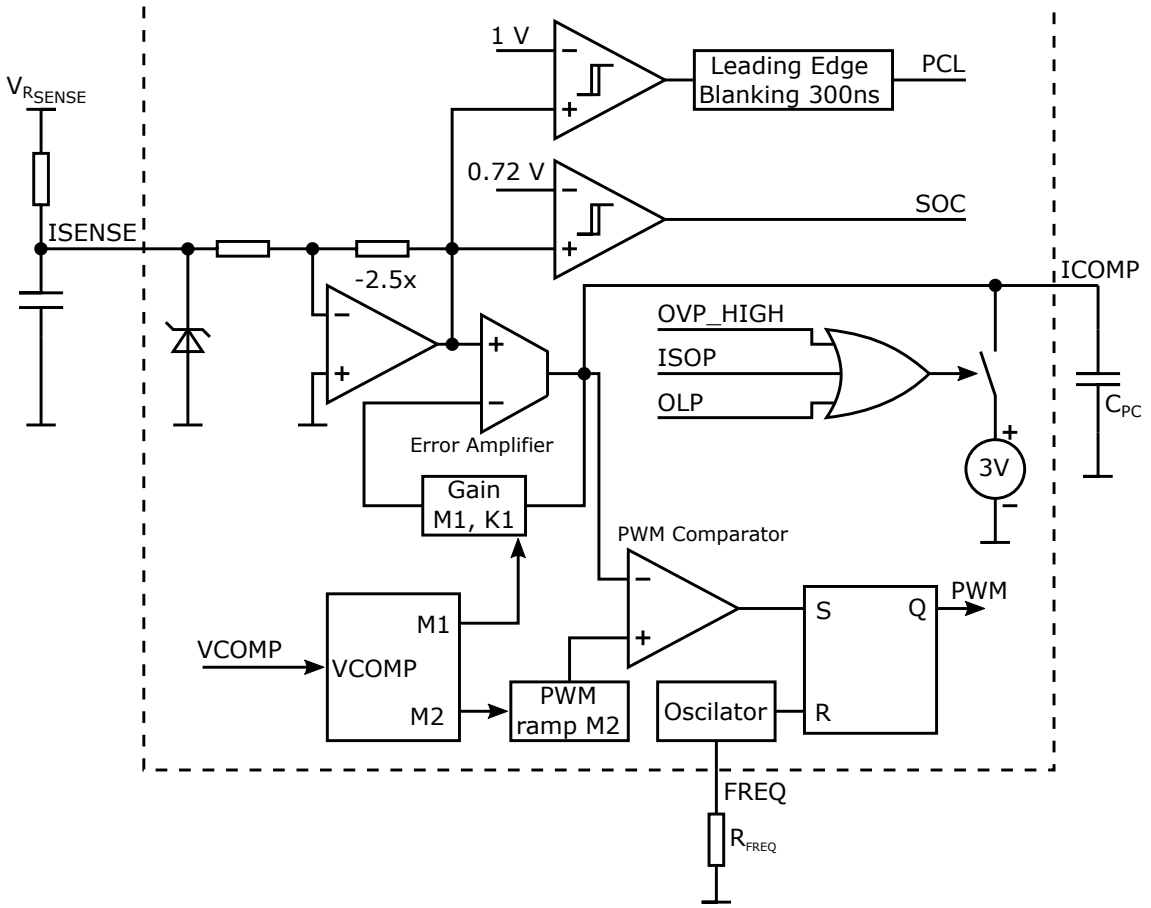


Fig. 7.3 Block diagram of the current loop circuit.

linearly. When the signal equals to the voltage on the *ICOMP* pin, the on-time pulse is generated. The on-time interval is terminated at the end of the switching cycle.

The *ICOMP* signal is proportional to the inductor current. The control loop regulates the *ICOMP* signal to reproduce the sinusoidal reference voltage. As a consequence, the average line current will be also sinusoidal.

The output of the modulator is connected to the gate driver. The gate drive is capable of amplifying the PWM signal for suitable voltage and current level for power transistor. The driver is able to shut down as well if the protections are activated [54].

The compensation process begins with a current loop, afterwards it focused to a voltage loop. The current loop compensation is influenced by a inner loop variables. The inner loop variables (M_1, M_2) depend on the power stage setting and controller constants K_1 and K_{FQ}. The K_1 constant equals to 7 and the K_{FQ} is inversely proportional to the frequency 7.39 [54].

$$K_{FQ} = \frac{1}{f_{SW}} = \frac{1}{2e^5} = 5e^{-6} \tag{7.39}$$

The calculation of the inner loop variables (equation 7.40 [54]) is performed at the nominal input voltage and output power.

$$M_1 \cdot M2 = \frac{I_{OUT_{max}} \cdot V_{OUT}^2 \cdot 2.5 \cdot R_{SENSE} \cdot K_1}{\eta V_{IN}^2 \cdot K_{FQ}} = \frac{1.282 \cdot 390^2 \cdot 2.5 \cdot 0.022 \cdot 7}{0.92 \cdot 230^2 \cdot 5e^{-6}} = 0.182 \frac{V}{\mu s} \tag{7.40}$$

When the multiplication of M_1 and M_2 is known, the value is compared with a graph of dependence of the *VCOMP* on the factor. The graph can be found in the documentation of the controller. In the graph can be found an operational point of the controller [54].

$$M_1 \cdot M2 = \frac{1.282 \cdot 390^2 \cdot 2.5 \cdot 0.022 \cdot 7}{0.92 \cdot 230^2 \cdot 5e^{-6}} = 0.182 \frac{V}{\mu s} \tag{7.41}$$

The operational point is determined at the intersection of the value 0.182 and the curve which represents dependence between $M_1 M_2$ and *VCOMP*. From this investigation it is obtained that the *VCOMP* voltage is approximately $2.2V$. Based on this finding can be derived the individual value of the M_1 and M_2. The calculation of the loop factor is dependent on the *VCOMP* operational point [54].

The non-linear current loop gain factor M_1 is particular solution at the $2.2V$ *VCOMP* calculated by the equation 7.42 [54].

$$M_1 = 0.313 \cdot VCOMP - 0.401 = 0.313 \cdot 2.2 - 0.401 = 0.288 \tag{7.42}$$

The non-linear PWM ramp slope factor M_2 at $2.2V$ $VCOMP$ is determined by the equation 7.43 [54].

$$M_2 = \frac{f_{SW}}{6.5e^4} \cdot 0.1223 \cdot (VCOMP - 0.5)^2 = \frac{2e^5}{6.5e^4} \cdot 0.1223 \cdot (2.2 - 0.5)^2 = 0.64 \frac{V}{\mu s} \quad (7.43)$$

If the individual loop factor M_1 are multiplied by M_2, the product is comparable to the number derived from the equation 7.44. The difference is caused by an inaccuracy during identification process from the chart. For more accurate result is necessary provide an additional iteration loops [54].

$$M_1 \cdot M_2 = 0.288 \cdot 0.64 = 0.184 \frac{V}{\mu s} \quad (7.44)$$

The selection of the C_{ICOMP} capacitor plays crucial role on the stability of the current loop, phase lag, and final THD of the line current. The capacitor creates a current averaging pole which is placed at $5kHz$. The capacity determined according to the equation 7.45 [54].

$$C_{ICOMP} = \frac{g_{mi} \cdot M_1}{K_1 \cdot 2\pi f_{IAVG}} = \frac{0.95e^{-3} \cdot 0.288}{7 \cdot 2\pi 3e^3} = 1.24 \approx 1.2nF \quad (7.45)$$

It was chosen a standard capacitor value $1.2nF$. Due to the f_{IAVG} is determined to $5183.9Hz$ as is shown in the equation 7.46 [54].

$$f_{IAVG} = \frac{g_{mi} \cdot M_1}{K_1 \cdot 2\pi C_{ICOMP}} = \frac{0.95e^{-3} \cdot 0.288}{7 \cdot 2\pi 1.2e^{-9}} = 5183.9Hz \quad (7.46)$$

The total transfer function, which includes power stage, modulator gain, and error amplifier gain, is determined by the next representation 7.47 [54].

$$G_{CL}(f) = \frac{K_1 \cdot 2.5 \cdot R_{SENSE} \cdot V_{OUT}}{K_{FQ} \cdot M_1 \cdot M_2 \cdot L_{BST}} \cdot \frac{1}{s(f) \cdot \frac{s(f)^2 \cdot K_1 \cdot C_{ICOMP}}{g_{mi} \cdot M_1}} \quad (7.47)$$

$$G_{CL}(f) = \frac{7 \cdot 2.5 \cdot 0.022 \cdot 390}{5 \cdot 0.288 \cdot 0.64 \cdot 2e^{-4}} \cdot \frac{1}{s(f) \cdot \frac{s(f)^2 \cdot 7 \cdot 1.2e^{-9}}{0.95e^{-3} \cdot 0.288}} \quad (7.48)$$

For the graphical verification of the current loop setting is used Bode plots (figure 7.4 [54]).

$$G_{CLdB}(f) = 20 \cdot log(|G_{CL}(f)|) \quad (7.49)$$

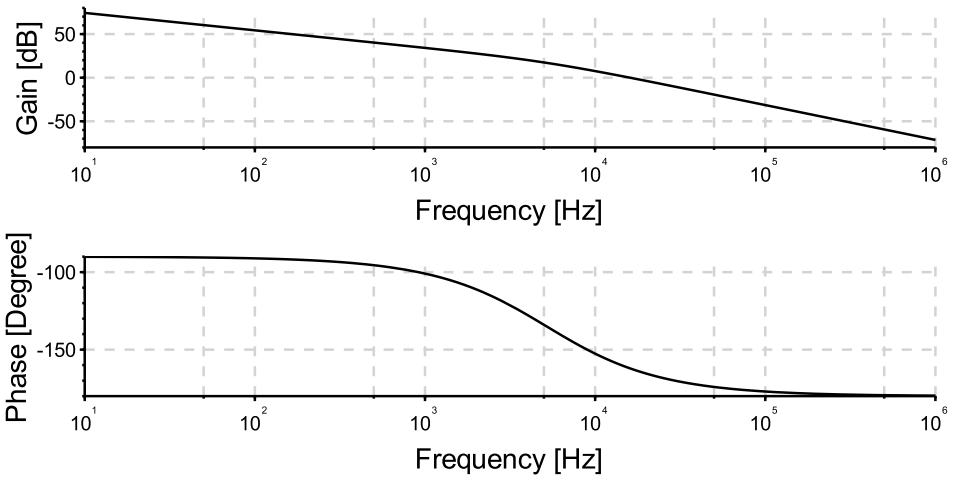


Fig. 7.4 Bode plots of the total open current loop gain with compensation.

7.8 Voltage Loop

The voltage loop is responsible for the output voltage regulation. The output voltage is sensed by the voltage divider. The voltage drop across the low resistor matches the internal reference voltage. The low bias current at the *VSENSE* pin allows to apply a high impedance sensing of the output voltage which reduces a power dissipation of the voltage divider. In a high-noise environment the filter capacitor should be connected to the down resistor in parallel [54].

The transconductance error voltage amplifier creates an error voltage based on the comparison of the feedback voltage on the *VSENSE* pin and internal 5V-reference voltage source. The amplifier output serves the current to the compensation network so that the output of the error amplifier matches the correct *VCOMP* voltage for the system. Due to the amplifier is a transconductance type, the impedance of the resistor-capacitor network creates the output impedance of the error amplifier. The network component selection plays a crucial role for the regulation in the full operation range of the APFC. The total capacity connected to the *VCOMP* pin determines the soft-start duration [54].

If the fault or standby conditions are present, the output of the error amplifier is pulled low. The capacitors of the compensation network are discharged to the initial value. The delay depends on the time constant of the compensation network. The controller enables several discharging paths which do not need a presence of the supply voltage. It takes advantage, if the supply voltage is removed quickly. It allows to avoid the inappropriate behaviour of the corrector [54].

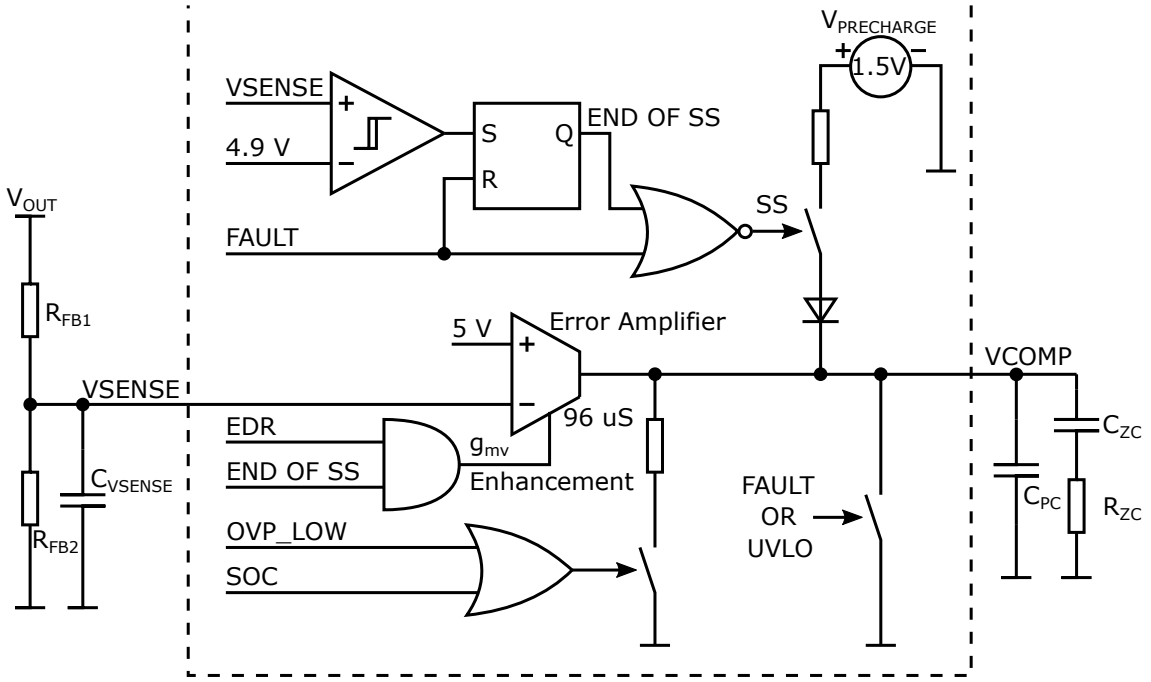


Fig. 7.5 Block diagram of the voltage loop circuit.

The error amplifier stage includes also EDR function which is capable of changing the transconductance parameter to $280\mu S$. The function will be activated if the perturbation at the output reaches 5% value of the nominal voltage. The increased gain helps to improve the speed of the feedback response of the loop. When the perturbations exceed 107% of the nominal value, the $4k\Omega$ resistor is connected to the $VCOMP$ pin. The resistor pulls the pin to low. If the output voltage grows above the 109% of the nominal value, the gate driver is shutting down. The gate driver is released when the output voltage decreases below the 102%-border of nominal voltage [54].

The voltage feedback attenuation G_{FB} is determined by the next equation 7.50 [54].

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \frac{1.3e^5}{1e^6 + 1.3e^5} = 0.013 \tag{7.50}$$

The non-linear gain variable M_3 is determined as follows 7.51 [54]. The M_3 variable is dependent on the $VCOMP$ voltage as well as M_1 and M_2 variables. The equation 7.51 [54] is valid for $VCOMP$ voltage in range $2V$ to $4.6V$.

$$M_3 = \frac{2e^5}{6.5e^4} \cdot (0.1148 \cdot VCOMP^2 - 0.1746 \cdot VCOMP + 0.0586) \tag{7.51}$$

After insertion all variables into the equation 7.51 [54] it is derived a value of the M_3 gain variable.

$$M_3 = \frac{2e^5}{6.5e^4} \cdot (0.1148 \cdot 2.2^2 - 0.1746 \cdot 2.2 + 0.0586) = 0.71 \frac{V}{\mu s} \tag{7.52}$$

The power stage is characterized by the frequency pole f_{PWMPS}. The equation 7.53 [54] shows a definition of the power stage pole.

$$f_{PWMPS} = \frac{1}{2\pi \cdot \frac{K_1 \cdot 2.5 \cdot R_{SENSE} \cdot V_{OUT}^3 \cdot C_{OUT}}{K_{FQ} \cdot M_1 \cdot M_2 \cdot V_{IN(nom)}^2}} = \frac{1}{2\pi \frac{7 \cdot 2.5 \cdot 0.022 \cdot 390^3 \cdot 470e^{-6}}{5 \cdot 0.288 \cdot 0.64 \cdot 230}} = 1.226Hz \tag{7.53}$$

The transfer function of the power stage is defined in the equation 7.54 [54].

$$G_{PWMPS}(f) = \frac{\frac{M_3 \cdot V_{OUT}}{M_1 \cdot M_2 \cdot 1}}{1 + \frac{s(f)}{2\pi \cdot f_{PWMPS}}} = \frac{\frac{0.71 \cdot 390}{0.288 \cdot 0.64 \cdot 1}}{1 + \frac{s(f)}{2\pi \cdot 1.226}} = \frac{1502.279}{1 + \frac{s(f)}{7.703}} \tag{7.54}$$

Where M_1 and M_2 was defined in the previous chapter and V_{OUT} equals $390V$. The equation 7.55 [54] shows a determining of the voltage loop transfer function which consists of the voltage feedback gain and the gain of the modulator with power stage.

$$G_{VL}(f) = G_{FB} \cdot G_{PWMPS}(f) \tag{7.55}$$

Finally, the open loop gain without the error amplifier gain is graphically represented by Bode plot (figure 7.6). The figure shows that the gain of the loop is $7.5dB$ at $10Hz$. This value is used for the next calculations and for final compensation of the error amplifier.

$$G_{VLdB}(f) = 20log(|G_{VL}(f)|) \tag{7.56}$$

The voltage error amplifier compensation network includes zero at f_{zero} and pole at f_{pole}. The zero is placed at the pole frequency f_{PWMPS} of the modulator with the power stage gain. The calculation of the zero is shown in the equation 7.57 [54].

$$f_{zero} = \frac{1}{2\pi \cdot R_{VCOMP} \cdot C_{VCOMP}} \tag{7.57}$$

The pole of the compensation network is estimated to $20Hz$. It is used for rejecting high frequency noise and compensating of the gain amplitude roll off. The equation 7.58 expresses

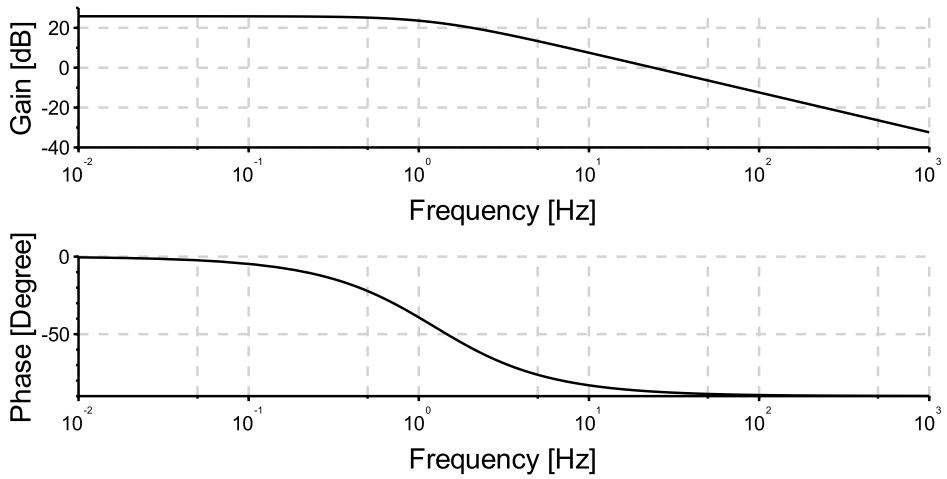


Fig. 7.6 Bode plots of the total open loop gain of the voltage loop without compensation.

the definition of the compensation network pole.

$$f_{pole} = \frac{1}{2\pi \cdot \frac{R_{VCOMP} \cdot C_{VCOMP} \cdot C_{VCOMP\_P}}{C_{VCOMP} \cdot C_{VCOMP\_P}}} \tag{7.58}$$

The final transfer function of the voltage loop error amplifier is calculated according the next expression 7.59 [54]. The transfer function is adjusted by a selection of the components connected to the error amplifier output.

$$G_{EA}(f) = \frac{g_{mv} \cdot (1 + s(f) \cdot R_{VCOMP} \cdot C_{VCOMP})}{(C_{VCOMP} + C_{VCOMP\_P}) \cdot s(f) \cdot \left(1 + s(f) \cdot \left(\frac{R_{VCOMP} \cdot C_{VCOMP} \cdot C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}}\right)\right)} \tag{7.59}$$

The selection of the components is related to the figure 7.6 [54]. The investigation of the graph shows that the gain of the transfer function at $10Hz$ equals to $7.5dB$. Generally, there are two capacitors. When it assumed that the parallel capacitor (C_{VCOMP_P}) is significantly smaller than the series one (C_{VCOMP}). The capacitor is calculated by the next equation 7.60 [54]. The calculation is based on the fact that the gain reaches to unity value at f_V. The zero of the transfer function is placed at f_{PWMPS}.

$$C_{VCOMP} = \frac{g_{mv} \cdot \frac{f_V}{f_{PWMPS}}}{10^{\frac{0 - G_{VLdb}(f)}{20}} \cdot 2\pi \cdot f_V} = \frac{56e^{-6} \cdot \frac{10}{1.226}}{10^{\frac{0-7.5}{20}} \cdot 2\pi \cdot 10} = 17.85\mu F \tag{7.60}$$

The calculated value of the C_{VCOMP} capacitor is suitable for the real component due to the size of the component. The capacitor has to withstand a maximum acceptable voltage at

the $VCOMP$ pin, which is $7V$. The selected capacitor has to fulfill the $10V$ voltage rating, large capacitance and the smallest package as possible. The final selection is based on the trade-off. The choice is the capacitor with $4.7\mu F$, $10V$ voltage rating and 0603 package size [54].

The calculation of the R_{VCOMP} resistor is based on the equation 7.57 [54] for the zero calculation and its modification into the next one 7.61. It was selected the $27k\Omega$ standard resistor.

$$R_{VCOMP} = \frac{1}{2\pi \cdot f_{zero} \cdot C_{VCOMP}} = \frac{1}{2\pi \cdot 1.226 \cdot 4.7e^{-6}} = 27.62k\Omega \approx 27k\Omega \tag{7.61}$$

Similarly, the parallel capacitor C_{VCOMP_P} can be found by modification of the pole calculation 7.58 [54].

$$C_{VCOMP\_P} = \frac{C_{VCOMP}}{2\pi \cdot f_{pole} \cdot R_{VCOMP} \cdot C_{VCOMP} - 1} \tag{7.62}$$

$$C_{VCOMP\_P} = \frac{4.7e^{-6}}{2\pi \cdot 20 \cdot 2.7e^{4} \cdot 4.7e^{-6} - 1} = 294.73nF \approx 330nF \tag{7.63}$$

Finally, the total closed loop transfer function can be defined as a multiplication of three factors. First factor is related to the gain of the voltage divider, second one defines the parameters of the power stage, and last one is determined by the error amplifier stage [54].

$$G_{VLtotal}(f) = G_{FB}(f) \cdot G_{PWMPS}(f) \cdot G_{EA}(f) \tag{7.64}$$

The graphical interpretation of the closed loop transfer function is provided by the next representation 7.65. As a result, it can be compiled the Bode plots (figure 7.65) for evaluation a stability criterion. From Bode plots it can be found that the crossover frequency of the corrector and phase margin. The crossover frequency is placed at approximately $20Hz$ and the phase margin reaches 60 degrees. However, the final tuning of the loop compensation is based on the behaviour of the prototype [54].

$$G_{VLtotaldB}(f) = 20log(|G_{VLtotal}(f)|) \tag{7.65}$$

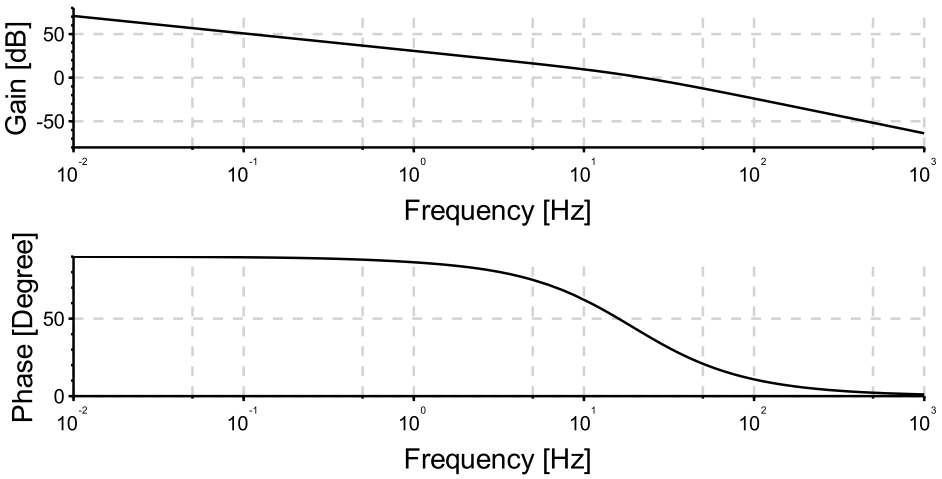


Fig. 7.7 Bode plots of the total closed loop gain and phase of the voltage loop.

7.9 Layout and Visualisation

The prototype board is made from a two layer PCB with dimensions $114x106mm$. The top and bottom layout patterns are shown in the figures 7.8 and 7.9. The next two figures are devoted to 3D models of the board. The last figure shows a photo of the hardware realization.

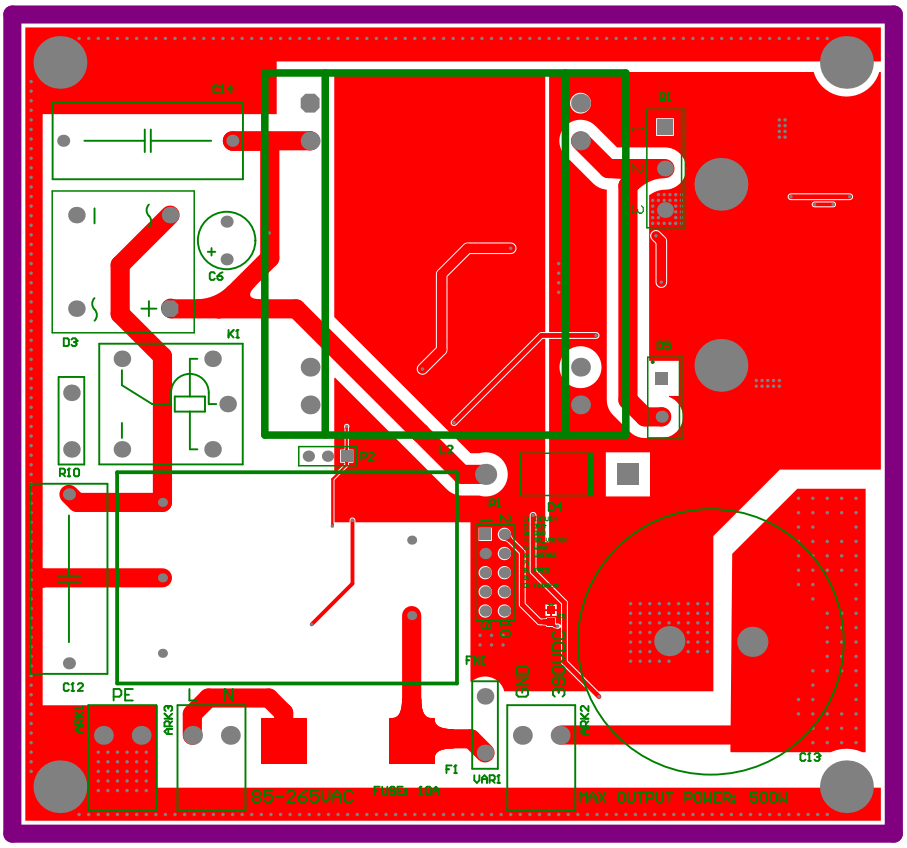


Fig. 7.8 Layout of the corrector - top view (1:1 scale).

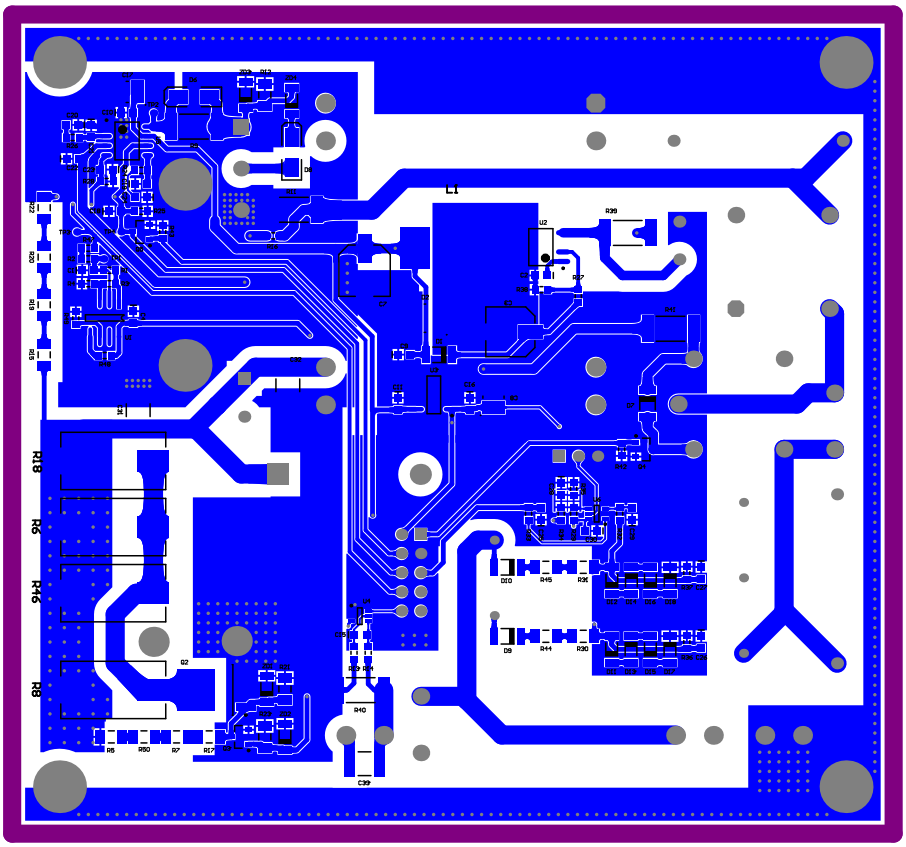


Fig. 7.9 Layout of the corrector - bottom view (1:1 scale).

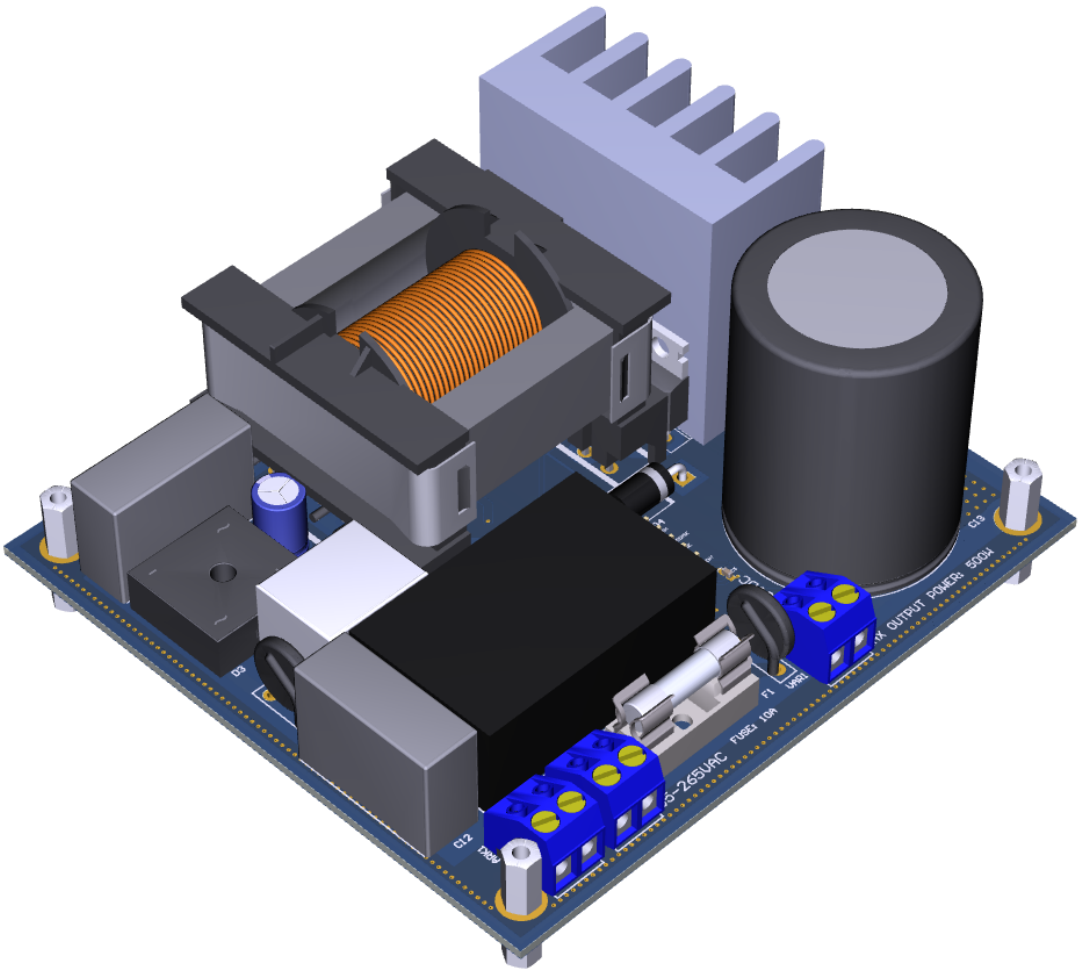


Fig. 7.10 3D model - top view.

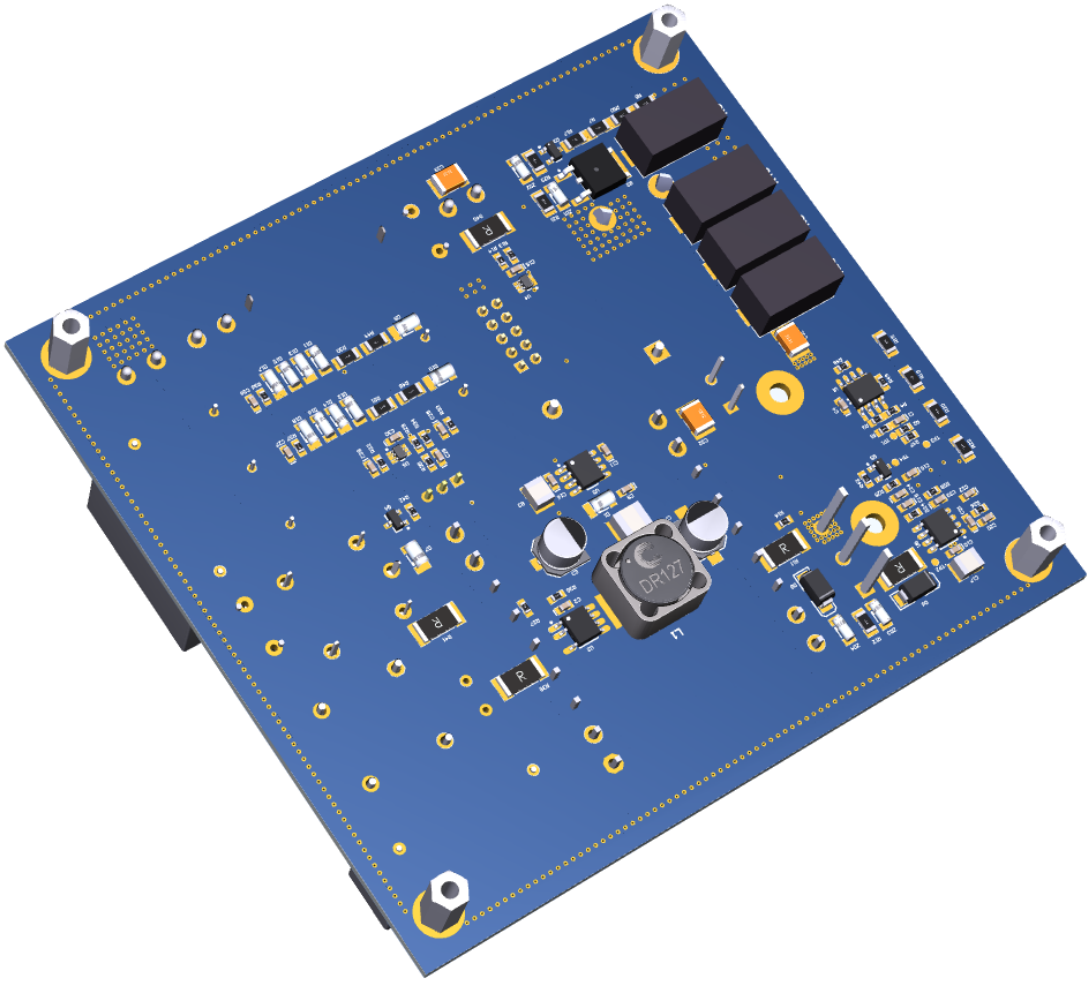


Fig. 7.11 3D model - bottom view.

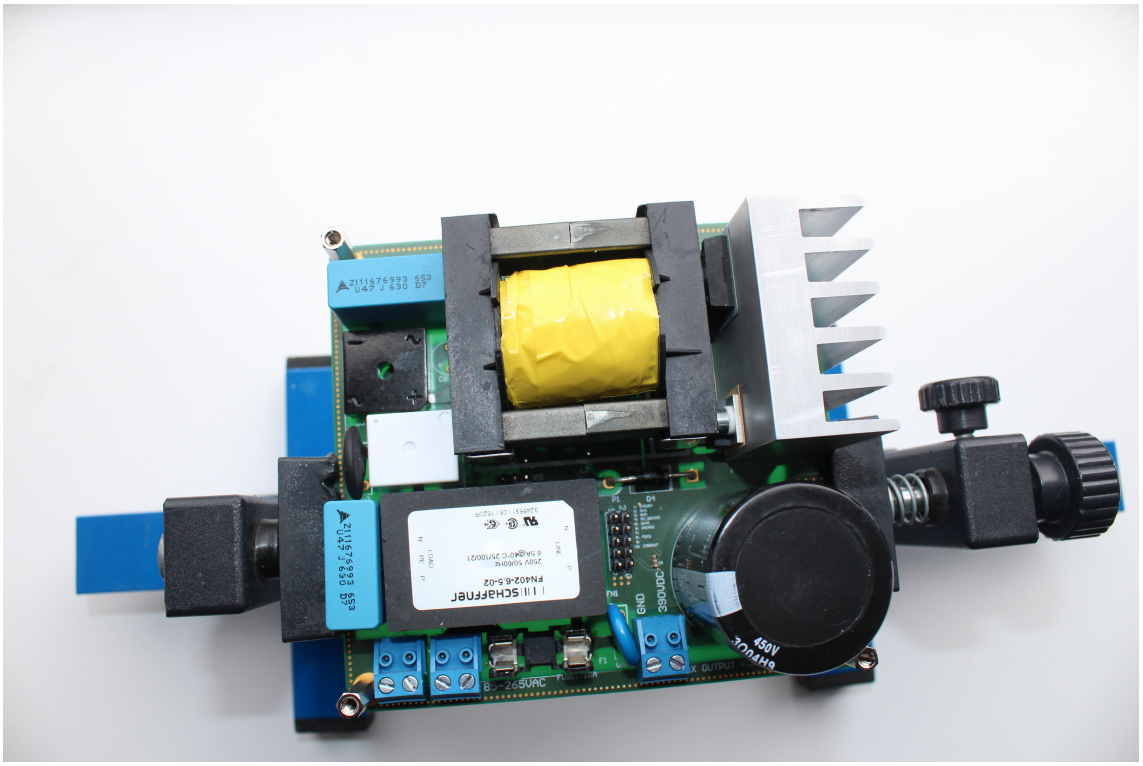


Fig. 7.12 Single boost corrector.

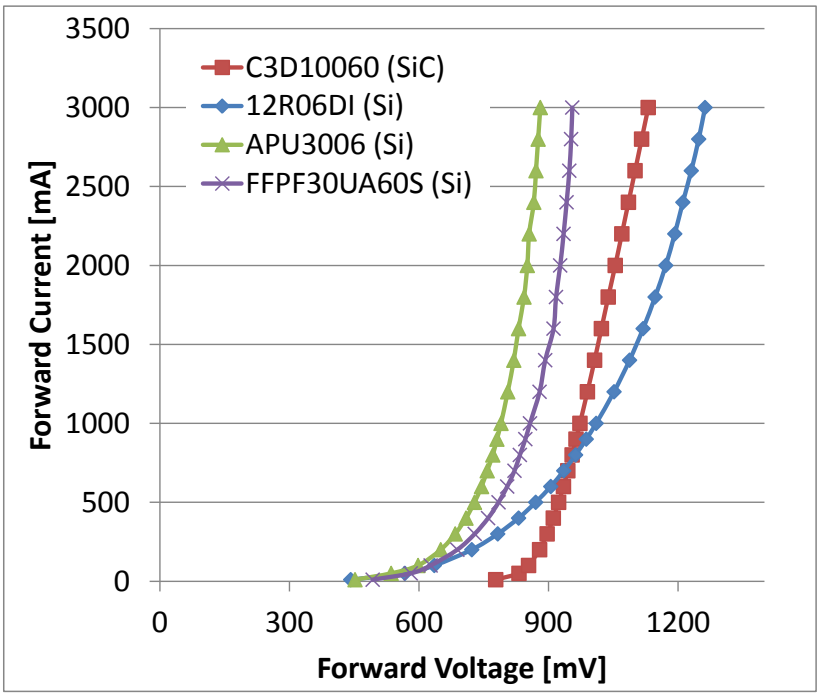


Fig. 7.13 Forward characteristics of the diodes.

7.10 Impact of Boost Diode Selection on Overall Efficiency of Active Power Factor Correctors

The chapter focuses on a selection process of boost diodes for APFC based on the Boost converter. The choice of the suitable boost diode plays crucial role for an efficiency of APFC. The main aim of the chapter is devoted to theoretical and experimental comparison of the diodes. It was compared two ultra fast silicon diodes optimized for CCM, soft-switching ultra fast rectifier and silicon carbide Schottky Barrier Diode (SBD).

This chapter focuses on performance various boost diodes working under CCM which is a common mode in APFCs. The instantaneous inductor current does not drop to zero within an one half period of the line voltage. This behavior, in other words hard-switching, requires very fast boost diodes. Regardless of this fact, the mode has several advantageous properties which are smaller peak line current, low line current ripple, constant switching frequency and simplified design of the EMI filter associated with it. The theory of the correctors operate under CCM is described in the chapter 3.1 [20].

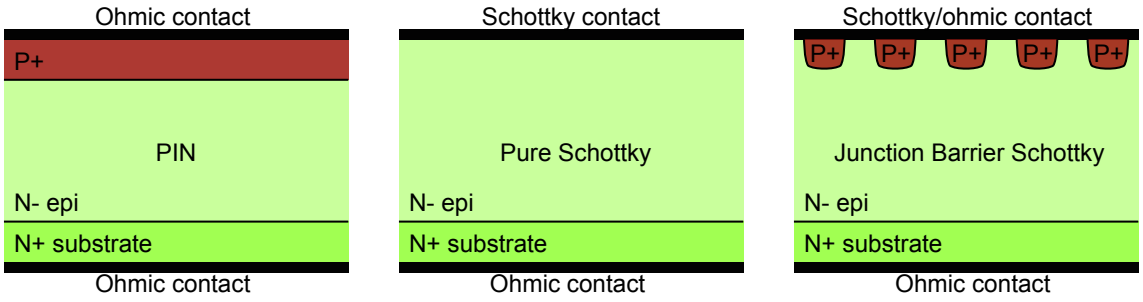


Fig. 7.14 Structural layout of the diodes, a) PIN ultra fast diode, b) pure Schottky, c) Junction Barrier Schottky.

7.10.1 Boost Diodes Comparison

APFCs based on the boost converter are usually designed for a high output voltage. The switching frequency of the commercial APFCs are frequently around $60kHz$. The shrinking trends force producers to develop APFCs with switching frequencies over $200kHz$. This application requires fast switching diodes with low reverse recovery charge and high blocking voltage. Schottky diodes based on the silicone substrate reach maximal $250V$ blocking voltage therefore they are not suitable for this application. For this application are usually used ultra fast silicon PIN diodes. Unlikely, these diodes are characterized by worse dynamic parameters than silicon Schottky diodes and their forward voltages are large. A silicon carbide substrate offers excellent thermal conductance, high breakdown electric field, and wide band gap [15], [4].

In the PIN ultra fast Si diodes, the diode structure 7.14 a) is organized as a sandwich structure with very poorly doped semiconductor region between the p-type semiconductor and the n-type semiconductor regions. The heavily doped regions allow construct ohmic contacts. The thickness of the poorly doped region affects a maximal reverse voltage of the diodes. Unfortunately, on-state resistance and reverse recovery charge grow hand in hand with the thickness of the intrinsic region. Advantage of the PIN diodes is their low leakage current. The leakage current strongly depends on the die temperature [15], [7], [20].

Due to the high leakage current of the pure Si Schottky diodes they can be apply up to $250V$ reverse voltage. The Schottky barrier is created by merger of the metal contact and the n-type region. The structure is shown on the picture 7.14 b). These diodes have extraordinary dynamic features and low forward voltage drop.

Owing to very low intrinsic concentration of carriers in the SiC substrate, silicon carbide devices allow operate under high temperature conditions (experimentally up to $600°C$, theoretically up to $800°C$). Unfortunately the current polymer packages are not able to overcome the $200°C$ temperature. This situation may be changed by Ceramic packages

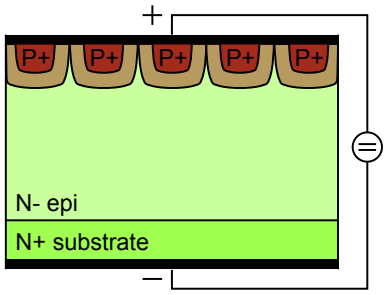


Fig. 7.15 Structural cross section of the Junction Barrier Schottky under reverse voltage.

called LTCC (Low Temperature Co-fired Ceramics) in the future. The excellent thermal conductivity of the substrate improves the heat transfer to the case. The high breakdown electric field strength of the SiC substrate opens a possibility of the construction of the high voltage diodes with a flat profile [15].

The main benefit of the SiC Schottky Barrier Diodes is excellent dynamic performance and mainly their negligible thermal drift. SiC SBDs have the ultra low junction charge Q_c. Thanks to this fact the switching losses are significantly suppressed [41].

The combination of the pure Schottky and PIN diode structures brings forth Junction Schottky Barrier Diodes. The structure on the picture (7.14 c) creates an adding of the p-type wells into n-type semiconductor of the “pure Schottky diode structure”.

The hybrid structure obtains the forward properties of the pure Schottky diodes and the reverse characteristics of the PIN diodes. Consequently, the structure behaves like pure Schottky diodes when the forward voltage is present and like PIN diodes when the reverse voltage is present. Thanks to this, the structure has low forward voltage drop and very low total junction charge Q_c. Detail of phenomenon at the reverse voltage is on the figure (7.15. The presence of depletion regions around p-type wells considerably reduces the leakage current [15].

The application of the SiC Schottky Barrier Diodes in the APFC operates under CCM leads to increasing of the efficiency regardless of the growing switching frequency which allows to shrink the passive components of APFCs. Consequently, the total costs of the APFC with SiC Schottky diodes can be similar maybe even lower. They have the high voltage blocking capability and the low leakage current. A crucial advantage is that the parameters are almost independent on the steepness of the forward current and the temperature of the die [1], [17].

Junction Schottky Barrier Diodes merge advantageous properties of both PIN and pure Schottky structures. Junction Schottky Barrier Diodes based on the SiC substrate are suitable for high voltage and high switching frequency. The worthwhile application sectors are

several. One feasible application can be APFCs with high output voltage ($400V$) and switching frequencies above $200kHz$ [17], [10], [20].

7.10.2 Conduction losses

Conduction losses depend on the forward voltage drop and the forward current. These losses can be computed by the following expression 7.66 [54], [20].

$$P_{D\_cond} = I_{out} \cdot V_F \tag{7.66}$$

Where I_{out} is the output current, which is adequate to the average diode current; V_F is the forward voltage drop across the diode. Specifically for the $C3D10060$ (equation 7.67) (SiC) at $230VAC$ input voltage, $400VDC$ output voltage and $500W$ output power thus the output current is $1.25A$. The computation gives the most accurate estimation of the losses. Any other estimation based on the power loss integration are not so suitable owing to the variable duty ratio within one half cycle period of the AC line [20].

$$P_{D\_cond} = 1.25 \cdot 1.006 = 1.2575W \tag{7.67}$$

Similarly for next diodes 12R06DI (7.68), APU3006 (7.69) and FFPF30UA60S (7.70)

$$P_{D\_cond} = 1.25 \cdot 1.088 = 1.36W \tag{7.68}$$

$$P_{D\_cond} = 1.25 \cdot 0.82 = 1.025W \tag{7.69}$$

$$P_{D\_cond} = 1.25 \cdot 0.892 = 1.115W \tag{7.70}$$

Table 7.2 Diode Parameters

%	$C3D10060$	$12R06DI$	$APU3006$	$FFPF30UA60S$
$V_R[V]$	600	600	600	600
$I_F[A]$	10	7	30	30
$Q_{rr}/Q_c[nC]$	25	180	580	360

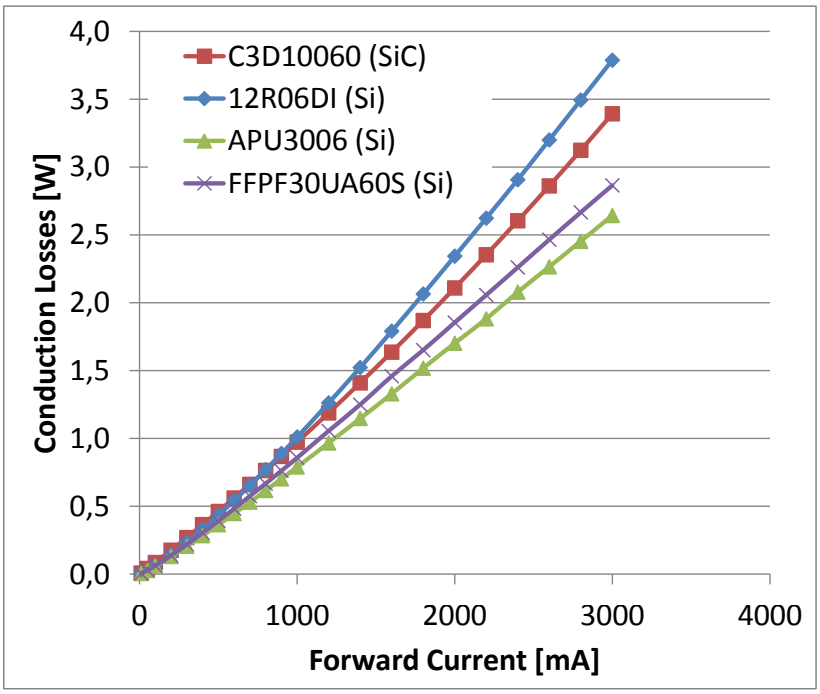


Fig. 7.16 Graph of the conduction losses.

Switching losses

Equation (7.71 [54], [20]) represents the switching losses in the diodes. Where Q_{rr} is reverse recovery charge, V_{OUT} is output voltage and f_{SW} is switching frequency.

$$P_{D\_sw} = 0.5 \cdot Q_{rr} \cdot V_{OUT} \cdot f_{SW} \tag{7.71}$$

$$P_{D\_sw} = 0.5 \cdot 25 \cdot 10^{-9} \cdot 400 \cdot 2 \cdot 10^{5} = 1W \tag{7.72}$$

$$P_{D\_sw} = 0.5 \cdot 180 \cdot 10^{-9} \cdot 400 \cdot 2 \cdot 10^{5} = 7.2W \tag{7.73}$$

$$P_{D\_sw} = 0.5 \cdot 580 \cdot 10^{-9} \cdot 400 \cdot 2 \cdot 10^{5} = 23.2W \tag{7.74}$$

$$P_{D\_sw} = 0.5 \cdot 360 \cdot 10^{-9} \cdot 400 \cdot 2 \cdot 10^{5} = 14.4W \tag{7.75}$$

Total losses can be acquired by sum of conduction and switching losses.

$$P_{total} = P_{D\_cond} + P_{D\_sw} = 2.2575W \tag{7.76}$$

$$P_{total} = P_{D\_cond} + P_{D\_sw} = 8.56W \tag{7.77}$$

$$P_{total} = P_{D\_cond} + P_{D\_sw} = 24.225W \tag{7.78}$$

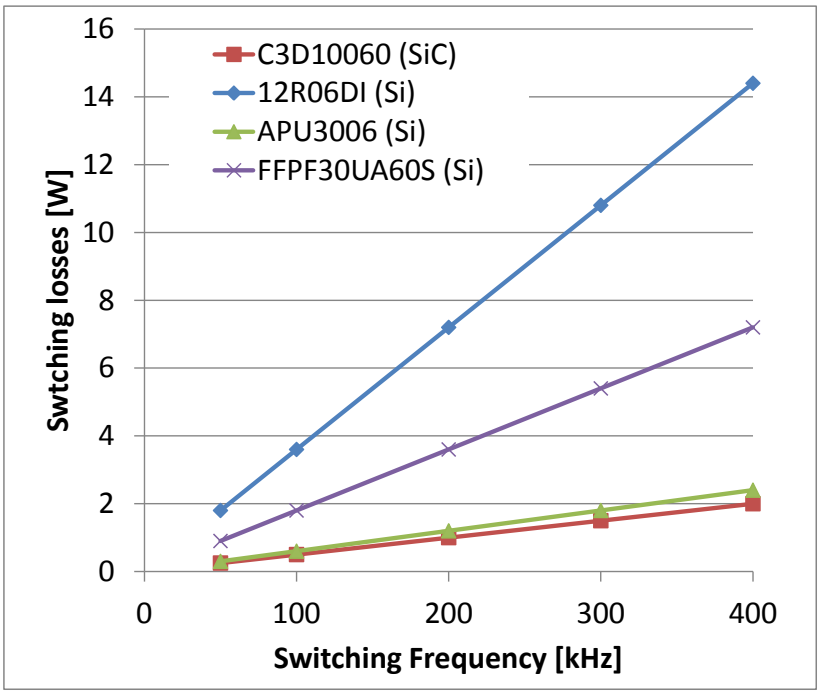


Fig. 7.17 Graph of the switching losses.

$$P_{total} = P_{D\_cond} + P_{D\_sw} = 15.515W \tag{7.79}$$

7.10.3 Experimental Results

The measurement was carried out on two different APFCs. Both of them worked under CCM. First APFC uses $UCC28180$ control circuit and their switching frequency was $200kHz$. Second APFC is controlled by $UCC28019$. The switching frequency of this circuit was $65kHz$. The selected diodes for the measurements are shown in the table 7.2. These diodes were deliberately chosen due to their different parameters. The $C3D10060$ diode is SiC Schottky Barrier Diode. Two diodes ($12R06DI$ and $FFPF30UA60S$) are ultra fast diodes suitable for hard-switching. The last diode (type $APU3006$) is soft-switching ultra fast rectifier optimized for APFCs worked under discontinuous or critical conduction mode. APFCs were powered by an isolated variable transformer. An input voltage was kept at $230V$. The measured data demonstrates that the diode selection plays crucial role in case that the switching frequency is more than $200kHz$. The diode selection for lower frequencies up to $100kHz$ is advisable to select mainly by the costs of the diodes due to negligible dependence on the overall performance [20].

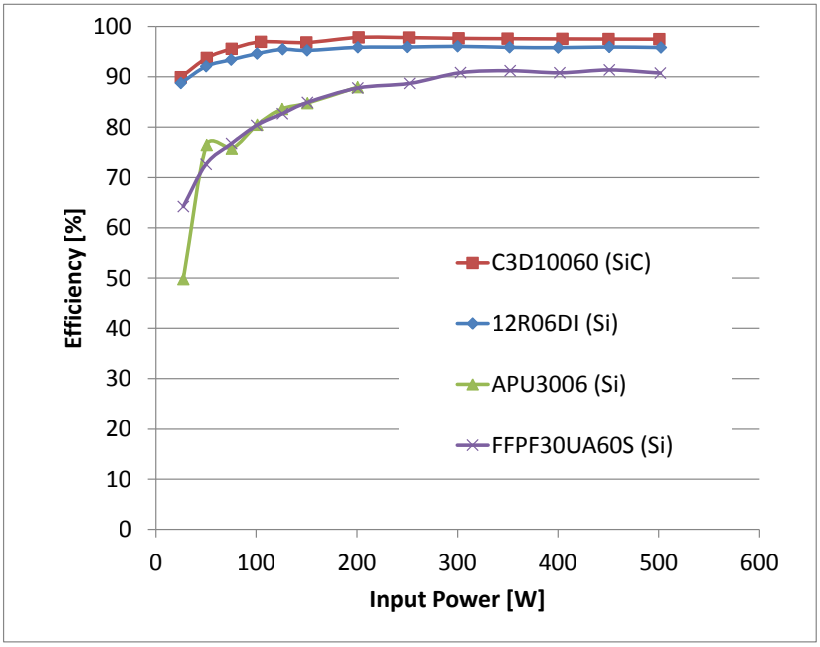


Fig. 7.18 Plot with the efficiency comparison at $200kHz$.

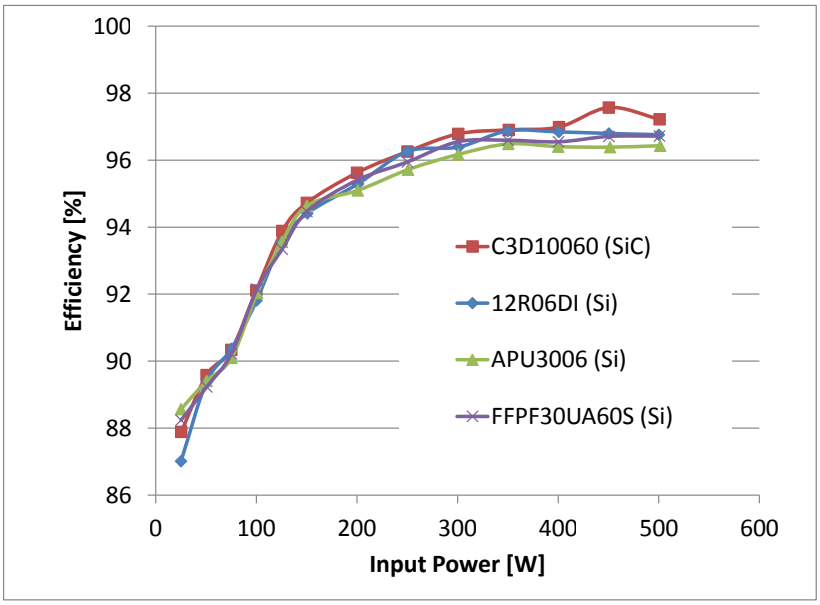


Fig. 7.19 Plot with the efficiency comparison at $70kHz$.

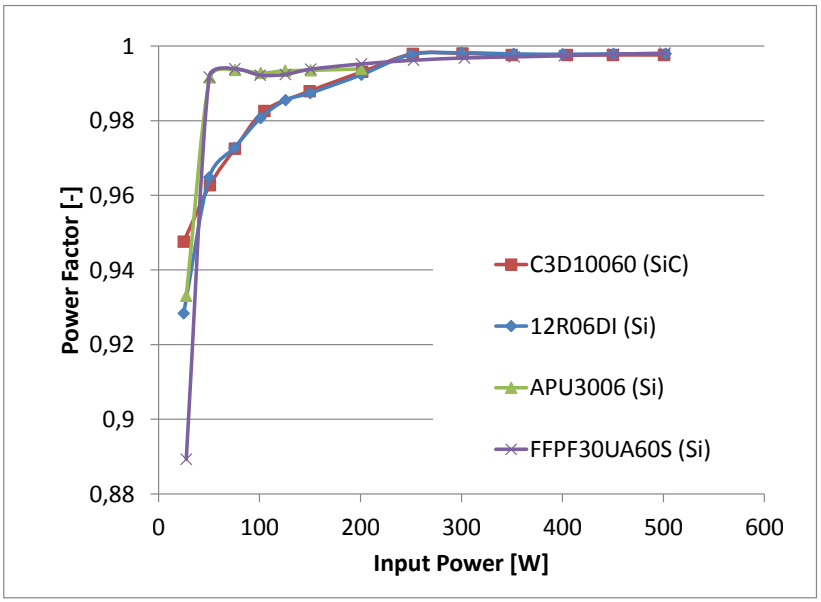


Fig. 7.20 Plot with the Power Factor correction comparison at 200kHz.

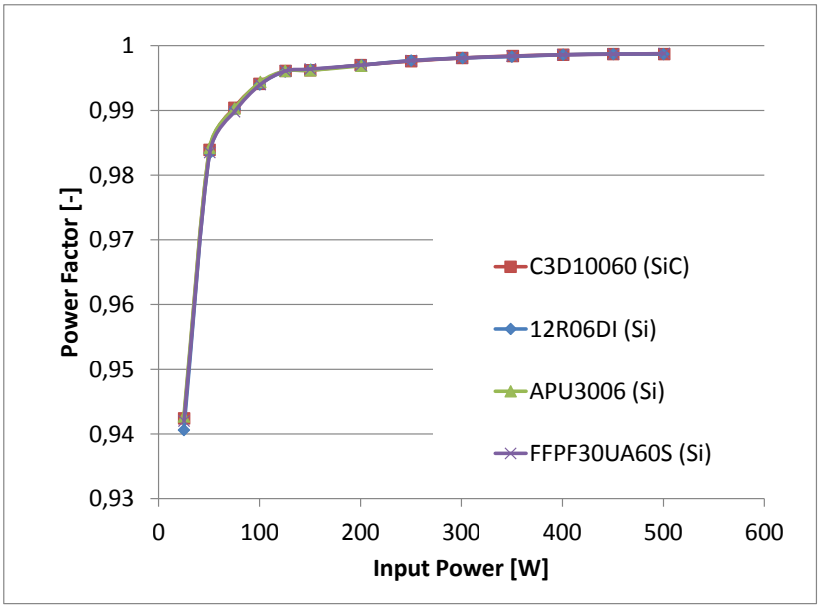


Fig. 7.21 Plot with the Power Factor correction comparison at 70kHz.

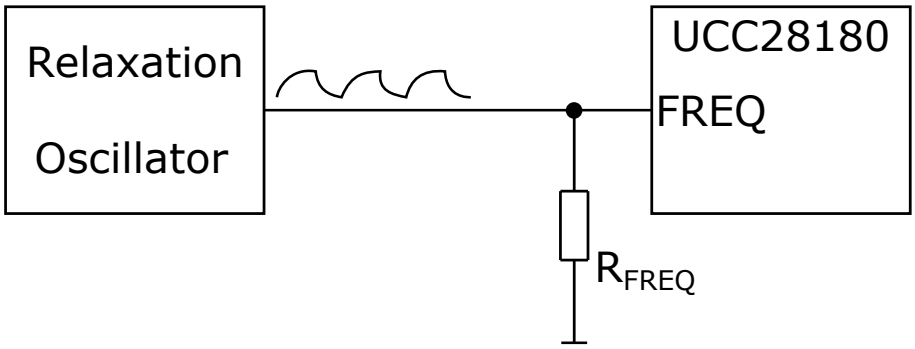


Fig. 7.22 Block diagram of the frequency dithering.

7.10.4 Discussion

This chapter demonstrates the advantages of SiC Schottky Barrier Diodes against ultra fast Si diodes. The main finding of this study is that the SiC Schottky Barrier Diodes are preferred for switching frequencies exceeding $200kHz$. The ultra fast diode optimized for soft-switching was failed during the test due to this diode type is not applicable in the APFC with CCM.

The experiment simultaneously shows that the SiC diode application in the APFCs with frequencies up to $100kHz$ is unfounded. All results are summarized in the figures (7.18, 7.19, 7.20, and 7.21).

From the outcome of this investigation it is possible to conclude that the SiC Schottky Barrier Diodes can improve the efficiency of the APFC working with the switching frequencies above $100kHz$. Although these diodes improve a performance at lower frequencies their use due to higher costs are not profitable. The obtained data shows that the diodes optimized for soft-switching are not appropriate for the hard-switching application.

7.11 Sweeping of Switching Frequency - Frequency Dithering

The CCM current mode with average current control provides a power factor correction function at the constant switching frequency. Generally, the constant switching is popular due to an easy feedback compensation and design of the EMI filters. In the some special cases is preferable a variable switching frequency. The main reason, why the variable frequency is applied, is an inadequate performance of the input EMI filtering or in most cases it can save costs for a serial production due to using cheaper EMI filters [38]. The process begins with final APFC. The EMI input filter is inadequate if the constant switching

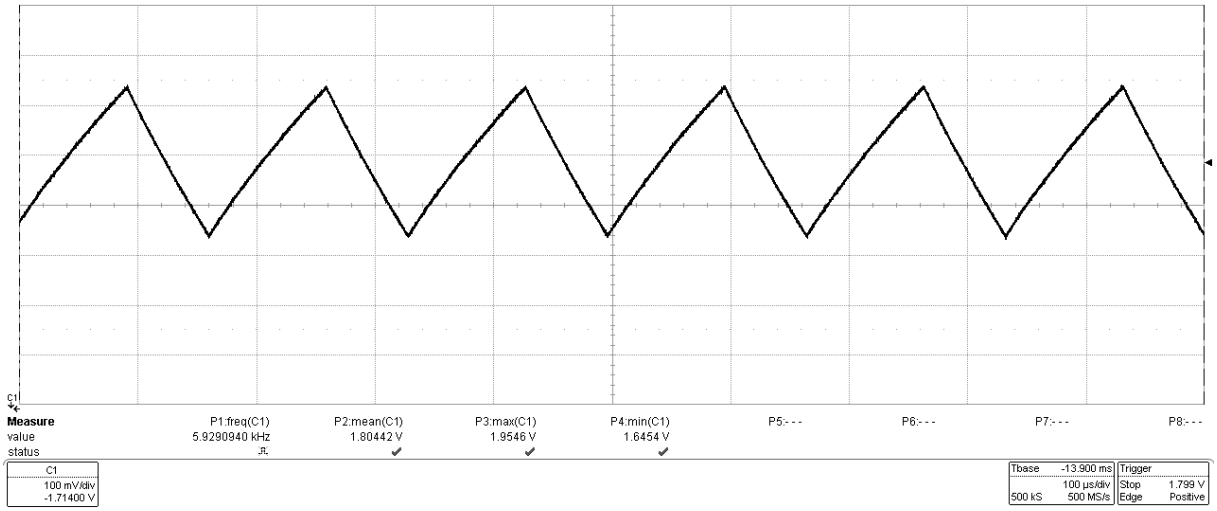


Fig. 7.23 Measured waveform of the frequency dithering output.

frequency is used. A selection of the filter is focused on the lower quality filters with a wider suppressing bandwidth. This type of filters can significantly reduced the costs. An inconvenience of this solution is that the SMPS will not be in compliance with regulation. When the variable switching frequency is used, the signal spectrum is spread into the wider bandwidth conversely the amplitudes of the harmonics which are reduced.

Due to the *UCC*28180 controller does not include a dithering circuitry, it is necessary to solve this issue by an external circuit. It was used a relaxation oscillator (in the figure 7.22) for providing of a suitable signal. The signal causes a voltage changes on the R_{FREQ} resistor. In other words, the relaxation oscillator provide a current sink or source for an internal current source. As a result, the switching frequency of the corrector is variable in the determined range.

The frequency dithering is characterized by a dither magnitude and rate. The dither magnitude determines a range of the switching frequency of the corrector. It is set to $0.31V$. The rate defines a frequency of the variation. In this case it was used $5.93kHz$. It means the change from minimum to maximum frequency takes $84.32\mu s$ [38].

7.12 Bill of Material

This section is devoted to a costs estimation for the prototype of the corrector. Price column includes all components in the row. The estimation is used for a final comparison of the prototypes. The total costs for the prototype with UCC28180 controller reaches 86.73 €.

Table 7.3 Simple bill of the material part 1 (UCC28180).

Designator	Type	Quantity	Price [€]
ARK1, ARK2, ARK3	ARK power connector 2-pin	3	1.4
C1, C2, C4, C5, C9, C10, C11, C15, C16, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30	SMD ceramic chip capacitor $100nF$ 0603	22	0.86
C3	SMD radial electrolytic capacitor $10\mu F/50V$	1	0.23
C6	THT radial electrolytic capacitor $1\mu F/350V$	1	0.24
C7	SMD radial electrolytic capacitor $10\mu F/50V$	1	0.25
C8, C17	SMD tantal capacitor $2.2\mu F/35V$ 1411	2	0.42
C12, C14	THT foil capacitor $470nF/275VAC$	2	1.08
C13	THT radial electrolytic capacitor $470\mu F/450V$	1	4.81
C31, C32, C33	SMD ceramic chip capacitor $100nF/630V$ 2512	3	1.8
D1, D7, D9, D10	Universal diode $BYD37M$ $1000V/1A$	4	0.44
D2	Ultrafast diode $600V/1A$ $MURS160-13-F$	1	0.36
D3	Bridge rectifier $600V/10A$ $KBPC1006$	1	1.32
D4	Universal diode $1000V/3A$ $1N5408$	1	0.29
D5	SiC Schottky diode $C3D10060$	1	4.03
D6	Schottky diode $40V/1A$ $FMKA140$	1	0.02
D8	Transil $550V$ $P4SMA550A$	1	0.48
D11, D12, D13, D14, D15, D16, D17, D18	Universal diode $1N4148$	8	0.64
F1	Fuse $10A/250V$ + fuse holder	1	0.5
FN1	EMI filter Schaffner $FN402-6.5-02$ $250V/6.5A$	1	10.48
K1	Electromechanical relay $RM50-3011-85-1012$	1	0.98
L1	Power inductor $1mH/260mA$ DR127-102-R	1	1.06
L2	Power inductor $ETD44$	1	6

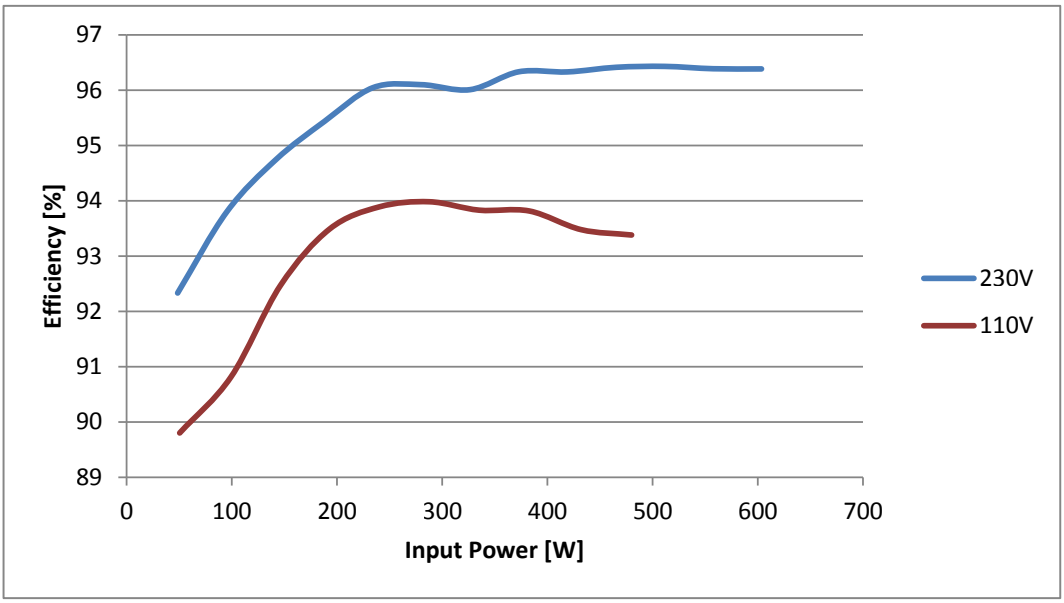
Table 7.4 Simple bill of the material part 2 (UCC28180).

Designator	Type	Quantity	Price [€]
P1	Male header $5x2$	1	0.49
P2	Male header $3x1$	1	0.12
Q1	Power MOSFET $SIHG30N60E$	1	5.93
Q2	Power MOSFET $IRFRC20PBF$	1	0.87
Q3, Q4, Q5	Power MOSFET $SQ2360EES$	3	0.99
R1, R2, R3, R4, R13, R14, R16, R24, R25, R26, R27, R28, R29, R32, R33, R34, R35, R36, R37, R38, R42, R43, R47, R48, R49	SMD chip resistors 0603	25	0.97
R5, R7, R12, R15, R17, R19, R20, R21, R22, R23, R30, R31, R44, R45, R50	SMD chip resistors 1206	15	1.17
R6, R8, R18, R46	SMD power resistor $SMF5W33KJ$	4	3.58
R9, R39, R41	SMD chip resistors 10Ω 2512	3	0.3
R11	SMD chip resistor 0.022Ω 2512	1	0.55
R10	Inrush NTC termistor $250V/5A$	1	0.8
R40	SMD chip resistors 0.01Ω 2512	1	0.45
U1	Analog comparator $TLV3201AIDCKR$	1	1.09
U2	LinkSwitch $LNK304$	1	1.26
U3	Low Drop Voltage Regulator $LE33CD$	1	0.81
U4	Current shunt monitor $INA214$	1	1.28
U5	PFC controller $UCC28180$	1	1.16
U6	Analog comparator $ADCMP608BKSZ-R2$	1	2.44
VAR1	Varistor $S14K275$	1	0.23
ZD1, ZD2, ZD3, ZD4	Zener diode $TZM5248B-GS08$ $18V/0.5W$	4	0.72
Heatsinks	Customized heatsink profiles	2	3
PCB	PCB $114x106mm(1.21dm^2)$	1	20.83
Total			86.73

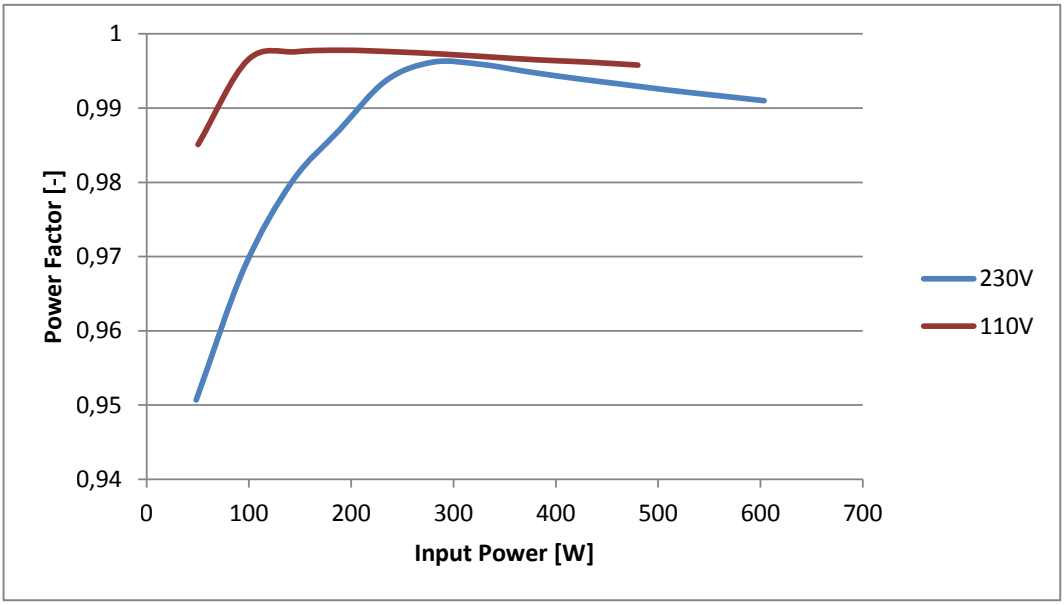
7.13 Experimental Results

7.13.1 Performance Measurement

The measurement was performed by the block diagram described in the section 6.5. The figure 7.24 a) describes an efficiency of the corrector and correction performance. The efficiency reaches 96.5% at 230V input voltage and 93.5% at 110V. Both values are investigated at 500W input power. The second figure 7.24 b) shows a correction performance in a full operation range. The power factor at 50W input power reaches 0.95 in case of 230V line voltage and 0.985 in case of 110V line voltage. The PF curve for 110V reaches its peak at 200W. Whereas the PF peak at 230V line voltage is shifted to the 300W input power and reaches the 0.996 value.



(a)



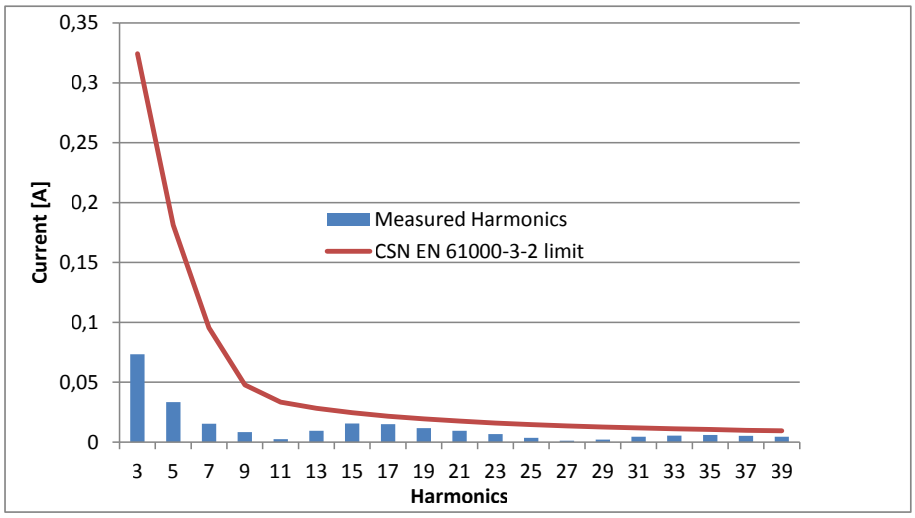
(b)

Fig. 7.24 Performance measurement of the corrector based on the UCC28180 controller a) efficiency, b) Power Factor.

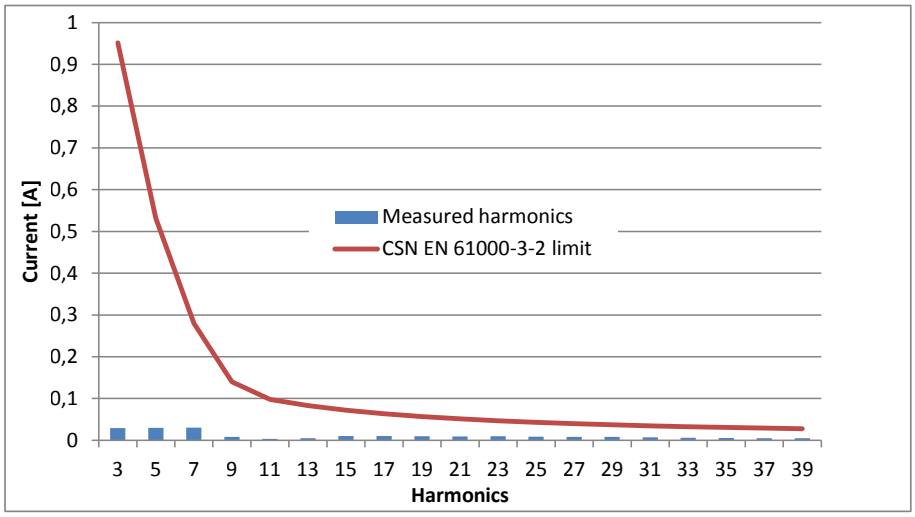
7.13.2 Harmonic Content According to ČSN EN 61000-3-2 Standard

The corrector has to comply harmonic order limits for the line current. The measuring setup uses a same equipment and connection as the performance measurement (the figure 7.24). Experimental results investigate a harmonic content at three input power values. The measurement was performed at $100W$, $300W$, and $500W$. The results are displayed in the figure 7.25. All figures include a harmonic order current limit which is calculated according to the ČSN EN 61000-3-2 standard [42] which defines two limits for *D* class.

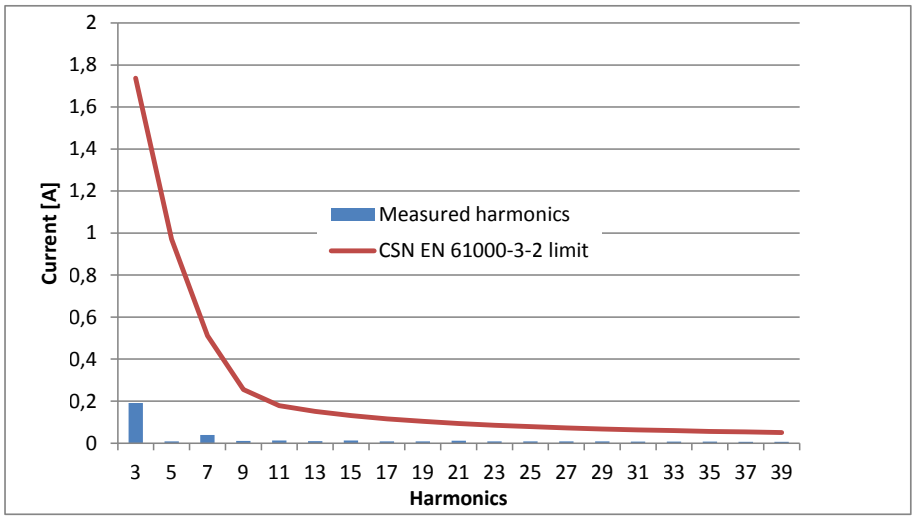
The first limit is related to current over the power (mA per W). Therefore the curve have to respect the power which is used during the measurement. The second limit defines absolute limit for the standard. In this case it was used only first rule for comparison the measured data and limits. The comparison shows that the experimental results fulfilled the limits which are set by the standard. If the figures are compared each other, the figure a) represents the worse correction due to the low input current. The last figure shows a typical behaviour of the correctors at high line and high load which is increment of the 3^{nd} harmonic current [42].



(a)



(b)



(c)

Fig. 7.25 Harmonics content of the corrector at different loads, a) 100W, b) 300W, c) 500W.

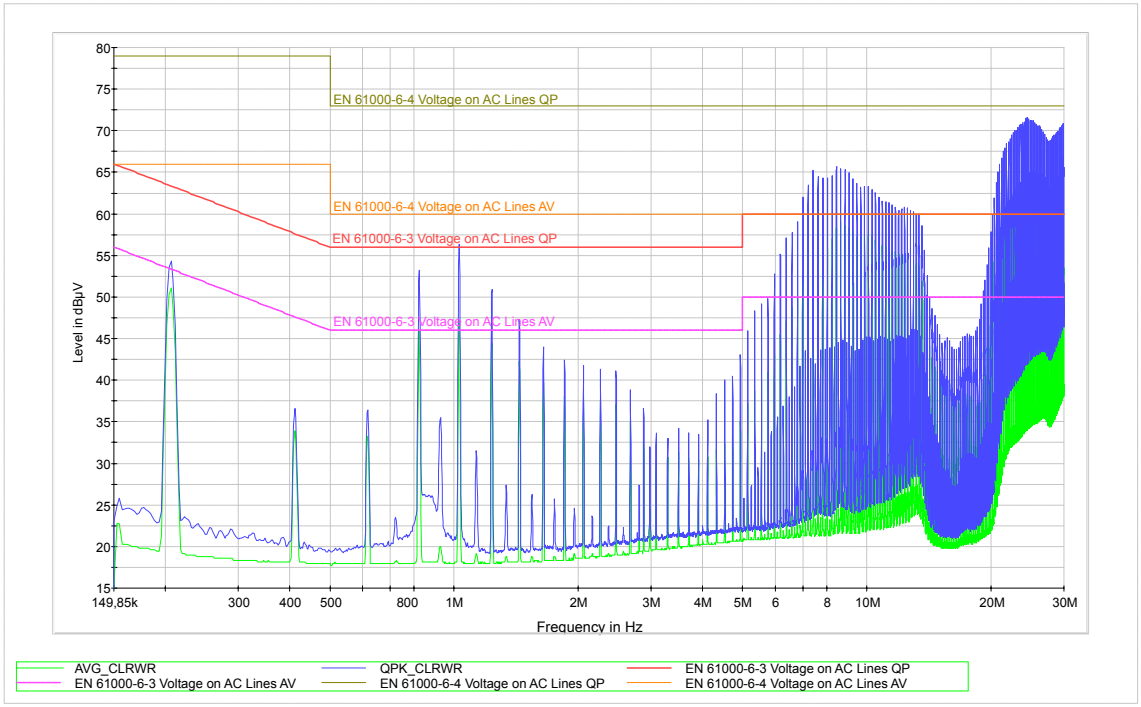
7.13.3 Conductive EMI Test

The conductive EMI tests were carried out regarding to the section 6.7. The measurement was performed into two hardware configuration of the correctors. The first option is the corrector which is optimized for highest efficiency. The corrector operates with $200kHz$ switching frequency, 4.7Ω gate resistor, high-speed MOSFET transistors without snubber and frequency dithering. The efficiency reaches $96,5\%$ at $230V$ and 94% at $110V$ line voltage.

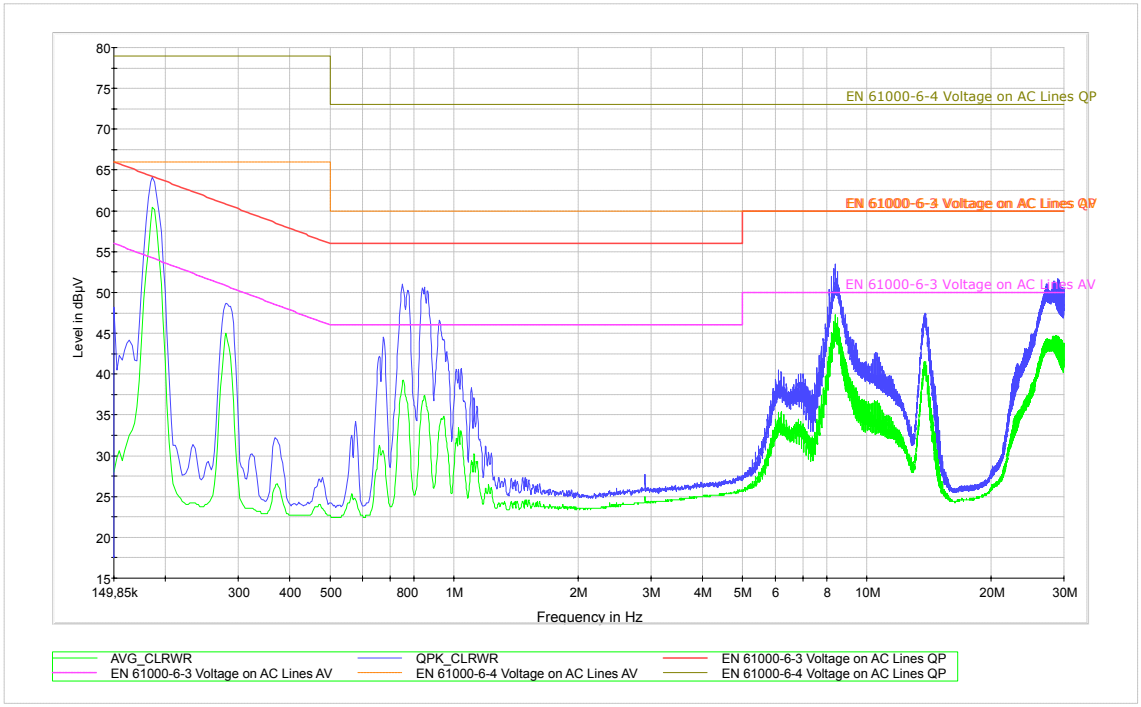
The using MOSFET transistors with 4.7Ω gate resistor causes a short edges of the switching waveforms and low switching losses. This setup has a direct impact on the EMI performance. The figure 7.26 a) includes narrow peaks at multiples of the fundamental frequency. Due to the short rise and fall times the high frequency content is rose. Several peaks overcome the limit line for EMI standard EN 61000-6-3.

Second option of the corrector is characterized by a reduced switching frequency to $100kHz$. The gate resistor was replaced by 10Ω gate resistors. The transistor is equipped by a snubber circuit. MOSFET transistor was replaced by IGBT transistor. The amplitudes of the harmonic content is reduced by a frequency dithering in the range 90 to $110kHz$. Both cases use same EMI filter Schaffner FN2090-10-06 [40].

Second figure shows the experimental results at the second hardware setup. The graph includes flat and smaller peaks of the harmonics 7.26 b). The spectrum is continuous in the full scale. The limit for standard ČSN EN 61000-6-4 [44] is fulfilled. The more strict standard ČSN EN 61000-6-3 [43] is not fulfilled due to the overcomes of measured data. The better results can be reached by following complete revision of the layout.

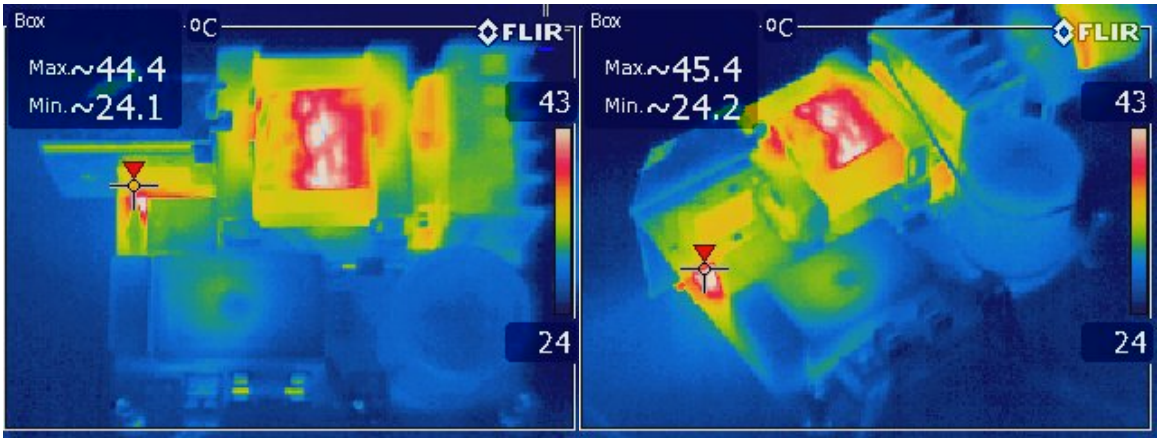


(a)

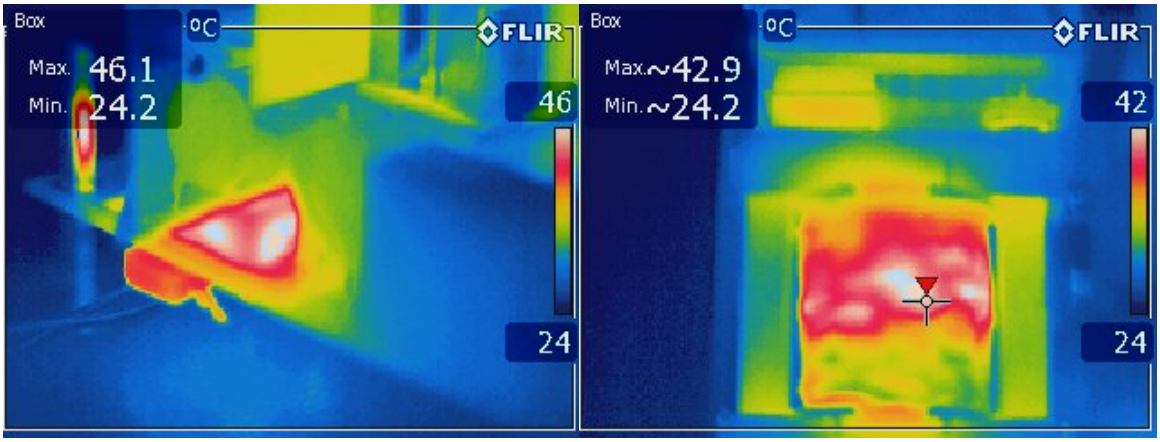


(b)

Fig. 7.26 Conductive EMI test results, a) graph of the emissions without the optimization for EMI, b) graph of the emissions with the optimization for EMI.



(a) (b)

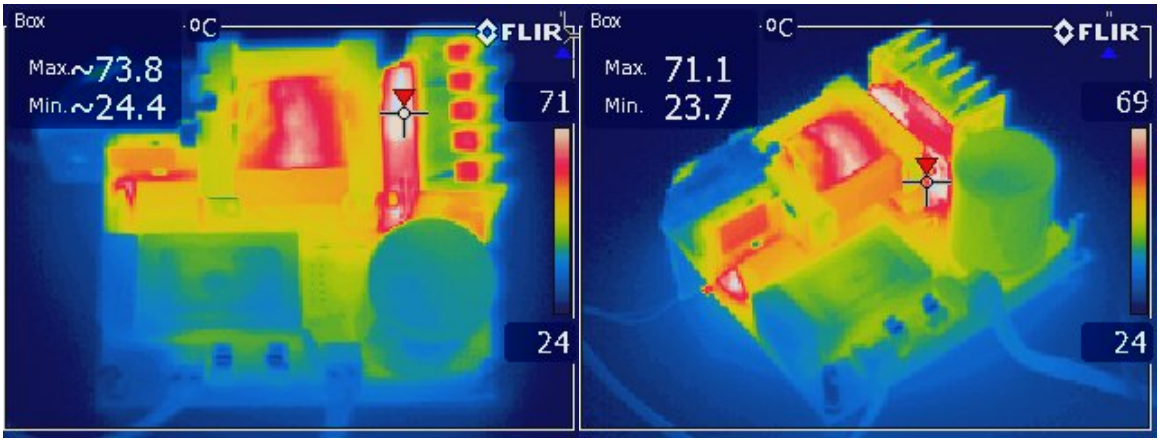


(c) (d)

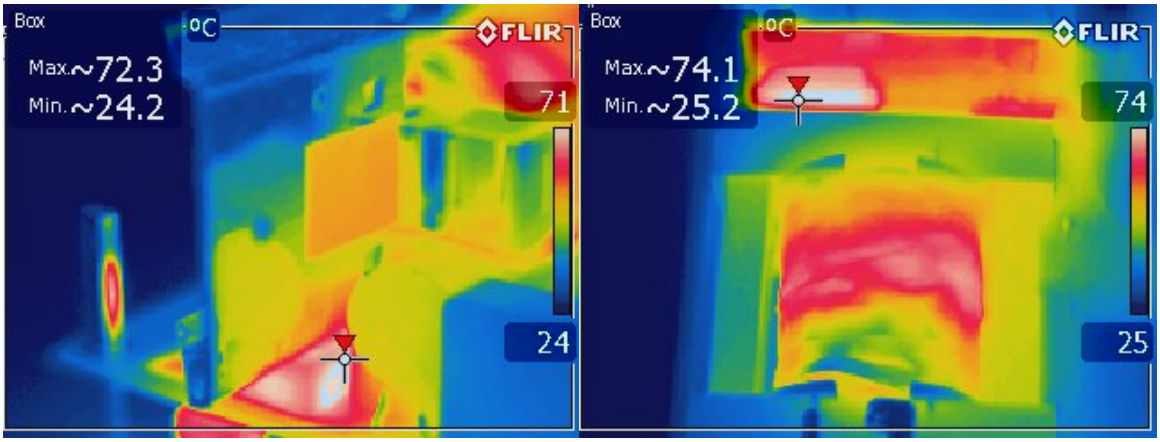
Fig. 7.27 Thermal image of the APFC based on UCC28180 which operates at 500 W output power with active cooling, a) top view, b) isometric view, c) thermal image of the rectifier bridge, d) thermal image of the MOSFET transistor and power inductor.

7.13.4 Thermal Measurement

A thermal measurement was performed according to the 6.8 section. The first group of the figures shows thermal images of APFC based on the $UCC28180$ controller which operates at the $500W$ output voltage. The prototype is actively cooled by a fan. The fan air flow is $240m^3/h$. The second group of pictures shows the thermal images in case of a natural passive cooling. The first figure is focused on the top view of the corrector. The bridge rectifier is a component with the highest temperature on the board. The figure b) shows an isometric view on the corrector. A detail of the bridge rectifier and power inductor is presented by the c) and d) segments.



(a) (b)



(c) (d)

Fig. 7.28 Thermal image of the APFC based on UCC28180 which operates at 500 W output power without active cooling, a) top view, b) isometric view, c) thermal image of rectifier bridge, d) thermal image of the MOSFET transistor and power inductor.

The measurement shows that the bridge rectifier reaches the maximal temperature 46.1 when APFC is actively cooled by a fan. In case of natural cooling the MOSFET transistors are heated to 75.

Chapter 8

Ultra Flat Profile Interleaved APFC

The *UCC*28060 controller allows to construct a two phase interleaved corrector. The controller uses FCCrM which reduces production costs and improves switching losses thanks to the soft switching. The controller uses two identical control loops which can be deactivated in case of the light load.

The technique uses a constant on-time of the transistor within the one cycle period. The on-time parameter is variable with line voltage changes. The current sensing is provided by current sense transformers. The *ZCDx* inputs monitor output voltages from current sense transformers. If the voltages drop to zero, the inductor current decreases also to zero. At this time the new cycle is established and the power transistor is switched on again. As a result, a triangular wave of the input current is produced by these on/off cycles [51].

$$I_{PEAK}(t) = \frac{V_{INAC}(t) \cdot T_{ON}}{L} \tag{8.1}$$

The average input current equals to a half of the I_{PEAK}. The expression is based on the geometrical relation of this signals, which was explained in the section 3.3.

$$I_{AVG}(t) = \frac{V_{INAC}(t) \cdot T_{ON}}{2 \cdot L} \tag{8.2}$$

An interleaving allows to cancel the input current ripple due to the 180° out of phase operation of their branches. As a consequence, input and output filters are significantly reduced in sizes as well as the final costs due to an using of the inexpensive components [51].

8.1 Power Stage Design

A selection of the power stage components is determined by design requirements which are summarized in the table 8.1.

Table 8.1 Requirements for a prototype based on the UCC28060 controller.

Design Parameter	Min	Typ	Max	Unit
Line Voltage $[V_{line}]$	85	-	265	V
Output Voltage $[V_{OUT}]$	-	390	-	V
Line Frequency $[f_{line}]$	47	-	63	Hz
Switching Frequency $[f_{sw}]$	40	-	500	kHz
Output Power $[P_{OUT}]$	-	600	-	W
Efficiency at nominal power $[\eta]$	92	-	-	%

First of all the maximal duty cycle must be defined based on a ratio between the output voltage of the corrector and the minimal value of the line voltage. The output voltage of the corrector is determined to 390 volts. The minimal operational input voltage is limited to 85 volts. Than, the duty cycle is computed by following equation 8.3 [51].

$$D_{peak} = \frac{V_{OUT} - V_{IN(min)} \cdot \sqrt{2}}{V_{OUT}} = \frac{390 - 85\sqrt{2}}{390} = 0.69 \tag{8.3}$$

Based on the duty cycle value, maximal output power and minimal frequency requirement it can be calculated suitable inductance of power inductors, which is defined in the equation 8.4 [51]. The efficiency is estimated to 92%. The minimal switching frequency was determined to $45kHz$ which is certainly out of the audible frequency range of the human hearing [51].

$$L1 = L2 = \frac{\eta \cdot V_{IN(min)}^2 \cdot D_{peak}}{P_{OUT} \cdot f_{min}} = \frac{0.92 \cdot 85^2 \cdot 0.69}{600 \cdot 45000} = 169.868\mu H \tag{8.4}$$

The power inductor shall be capable of handling the peak current at low line [51].

$$I_{Lpeak} = \frac{P_{OUT} \cdot \sqrt{2}}{\eta \cdot V_{IN(min)}} = \frac{600 \cdot \sqrt{2}}{85 \cdot 0.92} = 10.851A \tag{8.5}$$

The equation 8.6 [51] represents a RMS value of the inductor current.

$$I_{LRMS} = \frac{I_{Lpeak}}{\sqrt{6}} = \frac{10.851}{\sqrt{6}} = 4.42A \tag{8.6}$$

If the peak current is defined, the power components ratings can be computed by following equations. The equation 8.7 [51] derives the maximal power transistor current. The next equation 8.8 [51] expresses current through boost diode.

The power transistor is stressed by the voltage which equals to the output voltage. Therefore the minimal recommended voltage margin of the power transistor should be at least one half of the output voltage, the $SPB20N60C3$ [14] transistor was selected due to the $600V$ breakdown voltage and suitable features.

$$I_{DS} = \frac{I_{PEAK}}{2} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot V_{INmin}}{9\pi \cdot V_{OUT}}} = \frac{26.042}{2} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \cdot 85}{9\pi \cdot 390}} = 4.568A \tag{8.7}$$

Similarly, the voltage margin is also valid for the boost diode. The current rating of the diode is obtained as follows (the equation 8.8 [51]).

$$I_D = \frac{I_{PEAK}}{2} \cdot \sqrt{\frac{4\sqrt{2} \cdot V_{INmin}}{9\pi \cdot V_{OUT}}} = \frac{26.042}{2} \cdot \sqrt{\frac{4\sqrt{2} \cdot 85}{9\pi \cdot 390}} = 2.719A \tag{8.8}$$

As a last part of the section it is the output capacitor selection. The capacitor should be determined based on the output voltage ripple and the currents which it has to be capable of filtering them. The equation 8.9 [51] estimates a sufficient value of the output capacitance.

$$C_{OUT} \geq \frac{2 \cdot \frac{P_{OUT}}{\eta \cdot f_{line}}}{{V_{OUT}}^2 - {V_{OUT_{min}}}^2} = \frac{2 \cdot \frac{600}{0.92 \cdot 47}}{390^2 - 229.773^2} = 279.465\mu F \tag{8.9}$$

It was selected $4x82\mu F$ capacitors with the $450V$ voltage rating. The total capacitance is $328\mu F$. The next equation 8.10 [51] gives information about the output voltage ripple if the calculated capacitance is applied[51].

$$V_{RIPPLE} = \frac{2 \cdot P_{OUT}}{\eta} \cdot \frac{1}{V_{OUT} \cdot 4\pi \cdot f_{line} \cdot C_{OUT}} = \frac{2 \cdot 600}{0.92} \cdot \frac{1}{390 \cdot 4\pi \cdot 47 \cdot 3.28e^{-6}} = 17.696V \tag{8.10}$$

The filtering performance of the capacitor is defined by the following equations 8.11 [51] and 8.12 [51]. The first equation 8.11 expresses a required low frequency filtering performance of the output capacitor which defines a filtering of the double line frequency [51].

$$I_{C_{OUT100Hz}} = \frac{P_{OUT}}{\eta \cdot \sqrt{2} \cdot V_{OUT}} = \frac{600}{0.92 \cdot \sqrt{2} \cdot 390} = 1.182A \tag{8.11}$$

Second one (the equation 8.12 [51]) determines the high frequency filtering performance.

$$I_{C_{OUTHF}} = \sqrt{\frac{P_{OUT} \cdot 2 \cdot \sqrt{2}}{2\eta \cdot f_{line} \cdot V_{INmin}}} = \sqrt{\frac{600 \cdot 2 \cdot \sqrt{2}}{2 \cdot 0.92 \cdot 50 \cdot 85}} = 0.466A \tag{8.12}$$

8.2 Timing and Frequency Clamping

The section explains a definition of the timing. The on-time is parametrized by the error voltage and factor K_T (8.13 [51]).

$$T_{ON}(t) = K_T \cdot (V_{COMP} - 125mV) \tag{8.13}$$

Where V_{COMP} is the error voltage and the constant equals to $125mV$ is an offset of the PWM modulator. Due to the correctors are usually designed with the variable input voltage, the correctors have to compensate the voltage variation. For this reason there is in the equation 8.13 [51] a factor K_T which adjusts the on-time setting. The factor at low line is approximately three times larger than the factor at high line condition. The error voltage clamp is set to $4.95V$ therefore the maximal on-time can be calculated by the next equation 8.14 [51].

$$T_{ON(max)} = K_T \cdot (4.95 - 0.125) = K_T \cdot 4.825 \tag{8.14}$$

The on-time limits determine a maximal output power at the specific input voltage level. The timing factors are set by timing resistor R_{TSET}. The factor K_{TH} is related to high line conditions of the corrector (the equation 8.15 [51]).

$$K_{TH} = \frac{R_{TSET}}{1.33e^5} \cdot 1.35\mu s/V \tag{8.15}$$

The factor K_{TL} is related to low line conditions of the corrector. It expresses the equation 8.16 [51].

$$K_{TL} = \frac{R_{TSET}}{1.33e^5} \cdot 4\mu s/V \tag{8.16}$$

The factor K_T varies also when the corrector works under the single phase operation. When the single phase operation is activated the factors K_{TH} and K_{TL} are multiplied by the factor 2 [51].

$$T_{min} = \frac{R_{TSET}}{1.33e^5} \cdot 2.2\mu s \tag{8.17}$$

The parameter minimal switching period, which is defined in the equation 8.17, gives information about setting of the internal timers. When the inductor current drops to zero

before the time elapses, the next switching cycle is postponed until the time elapses. As a result the corrector operates under DCM.

The controller includes also a reset timer which prevents the corrector from operation under CCM. The restart timer is activated if the *ZCD* inputs have no high-to-low transition for $200\mu s$ [51].

$$f_{min} = \frac{\eta \cdot V_{INmin}^2 \cdot \left(1 - \frac{V_{INmin} \cdot \sqrt{2}}{V_{OUT}}\right)}{P_{OUT} \cdot L_{max}} = \frac{0.92 \cdot 85^2 \cdot \left(1 - \frac{85 \cdot \sqrt{2}}{390}\right)}{600 \cdot 2e^{-4}} = 38.319kHz \tag{8.18}$$

The equation 8.18 gives a minimal frequency setting regarding to maximal inductance and other corrector parameters. The frequency should be above the human audible noise which is approximately up to $20kHz$. Based on this result it can be calculated the timing resistor R_{TSET} (the equation 8.19 [51]).

$$R_{TSET} = \frac{1.33e^5 \cdot \left(1 - \frac{V_{in,min} \cdot \sqrt{2}}{V_{out}}\right)}{4.85 \cdot 4e^{-6} \cdot f_{min}} = \frac{1.33e^5 \cdot (1 - \frac{85 \cdot \sqrt{2}}{390})}{4.85 \cdot 4e^{-6} \cdot 38,319e^3} = 123.871k\Omega \approx 120k\Omega \tag{8.19}$$

The equation 8.20 [51] represents a frequency clamp which eliminates inadequate frequencies at low input voltages.

$$f_{max} = \frac{1.33e^5}{R_{TSET} \cdot 2e^{-6}} = \frac{1.33e^5}{1.2e^5 \cdot 2e^{-6}} = 554.167kHz \tag{8.20}$$

8.3 Control Methods

As it was mentioned in the section 5.2 there are several interleaving methods. The controller applies Natural Interleaving which improves the phase matching between branches. As a consequence, the input current ripple is minimized in spite of the inductance differences [51].

The corrector includes a power management feature which helps to improve the efficiency at light load. The feature allows to disable one branch of the corrector so that the efficiency will be improved. Disabling of one branch of the corrector has a direct impact on the losses decomposition. The losses ratio is variable and depends on the duty ratio and required power. As a result, the suitable phase management can improve the efficiency at light load. The controller provides internal and external control of the phase management [51].

The internal phase management corresponds to theoretical and experimental results of the manufacturer. The external phase management allows to customise the thresholds and open a possibility of the phase management tailoring to the specific application. The *PHB*

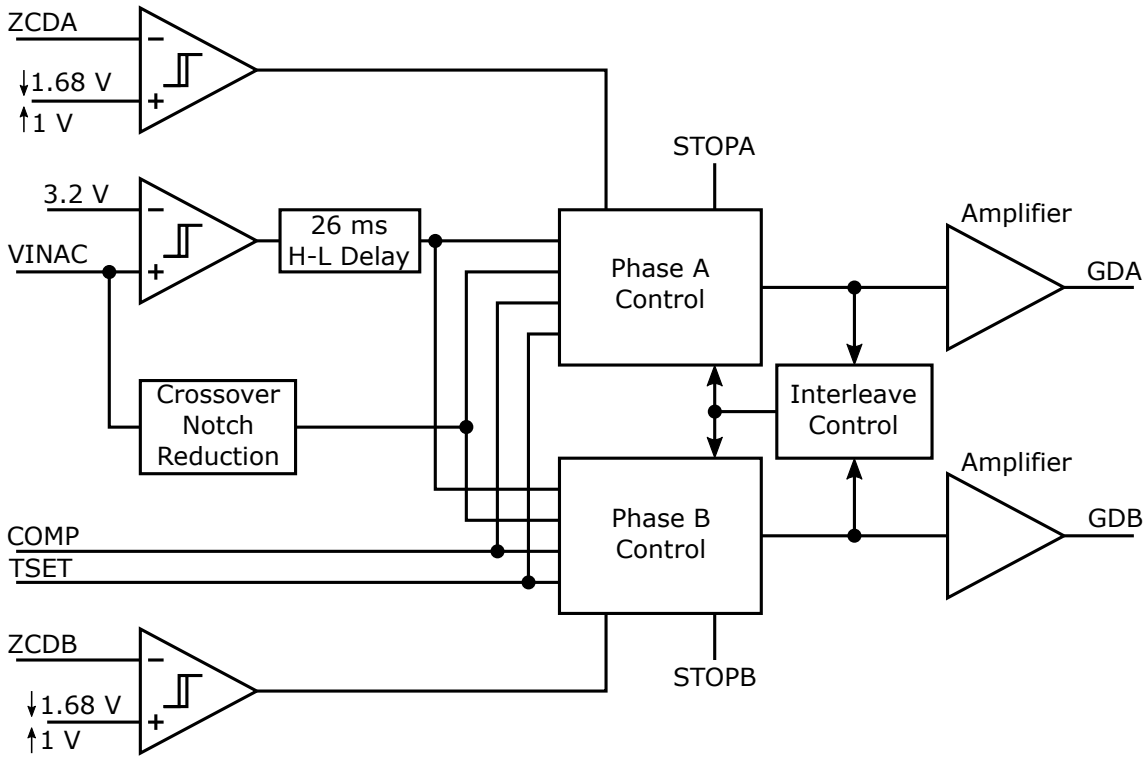


Fig. 8.1 Block diagram of the interleave control.

pin is responsible for the control of the feature. When the pin is connected to the *COMP* pin, the internal phase management is enabled. In the case that the pin is tied to the $VREF$ pin, the feature is disabled. Finally, if the pin is grounded the B branch is shunted down [51].

8.4 Zero Crossing Detection and Valley Switching

The CrM mode is characterized by a fact that the power transistor is switched on when the inductor current drops to zero. The main advantage of the quasi-resonant operation is the efficiency increase at light load. An input voltage range of the *ZCD* inputs is limited to $2V$. A turns ratio of the auxiliary winding can be computed by the following equation 8.21 [51].

$$\frac{N_P}{N_S} = \frac{V_{OUT} - V_{IN(max)} \cdot \sqrt{2}}{2} = \frac{390 - 265 \cdot \sqrt{2}}{2} = 8 \tag{8.21}$$

The controller uses an auxiliary winding for the zero crossing detection. When the auxiliary voltage is zero, the inductor current drops to zero. The input zener clamp of the *ZCD* inputs is limited to $3mA$ therefore the series resistors value is represented by the next

expression 8.22. As a result, the *ZCD* resistors with $18k\Omega$ resistivity were selected [51].

$$R_{ZA} = R_{ZB} = \frac{V_{OUT} \cdot N_S}{N_P \cdot 0.003} = \frac{390}{8 \cdot 0.003} = 16.3k\Omega \approx 18k\Omega \tag{8.22}$$

8.5 Output Voltage Set Point

An output voltage is set to $390V$ due to the value of the peak line voltage and common voltage rating of the output capacitors. Due to the input impedance of the controller the high side resistor is determined to $3M\Omega$. A high voltage condition of the high side resistor requires a splitting of the resistivity into more resistors owing to the maximal acceptable voltage on the SMD resistor type 1206, which is $200V$. Therefore three resistors are used with the $3M\Omega$ overall resistivity. For calculation it is used an internal $6V$ voltage reference due to the low side setting resistor is determined as follows (the equation 8.23 [51]).

$$R_D = \frac{V_{REF} \cdot R_C}{V_{OUT} - V_{REF}} = \frac{6 \cdot 3e^6}{390 - 6} = 47k\Omega \approx 47k\Omega \tag{8.23}$$

It was selected $47k\Omega$ for the low side resistor. The same resistivity is applied also for the voltage divider which is used for sensing AC line voltage.

8.6 Protection Circuits

The controller contains also several additional circuits which are brownout, output over voltage, over current, phase fail, and open loop protection. The block diagram 8.2 describes the basic elements of the protection circuitry [51].

8.6.1 Brownout Protection

The brownout protection helps to avoid an overloading of the power components at low line conditions. The AC line voltage is sensed by the resistor divider. When the line voltage drops below a brownout falling threshold, the gate drivers are immediately pulled low. The *VCOMP* output of the error amplifier is also pulled low [51].

$$R_A = \frac{Hysteresis}{7e^{-6}} = \frac{21}{7e^{-6}} = 3M\Omega \tag{8.24}$$

If the AC line voltage rises over the brownout rising threshold, the corrector soft-starts and after than operates normally. The difference between rising and falling thresholds creates a hysteresis which is set by a resistor divider radio. The ratio determinates the input voltage

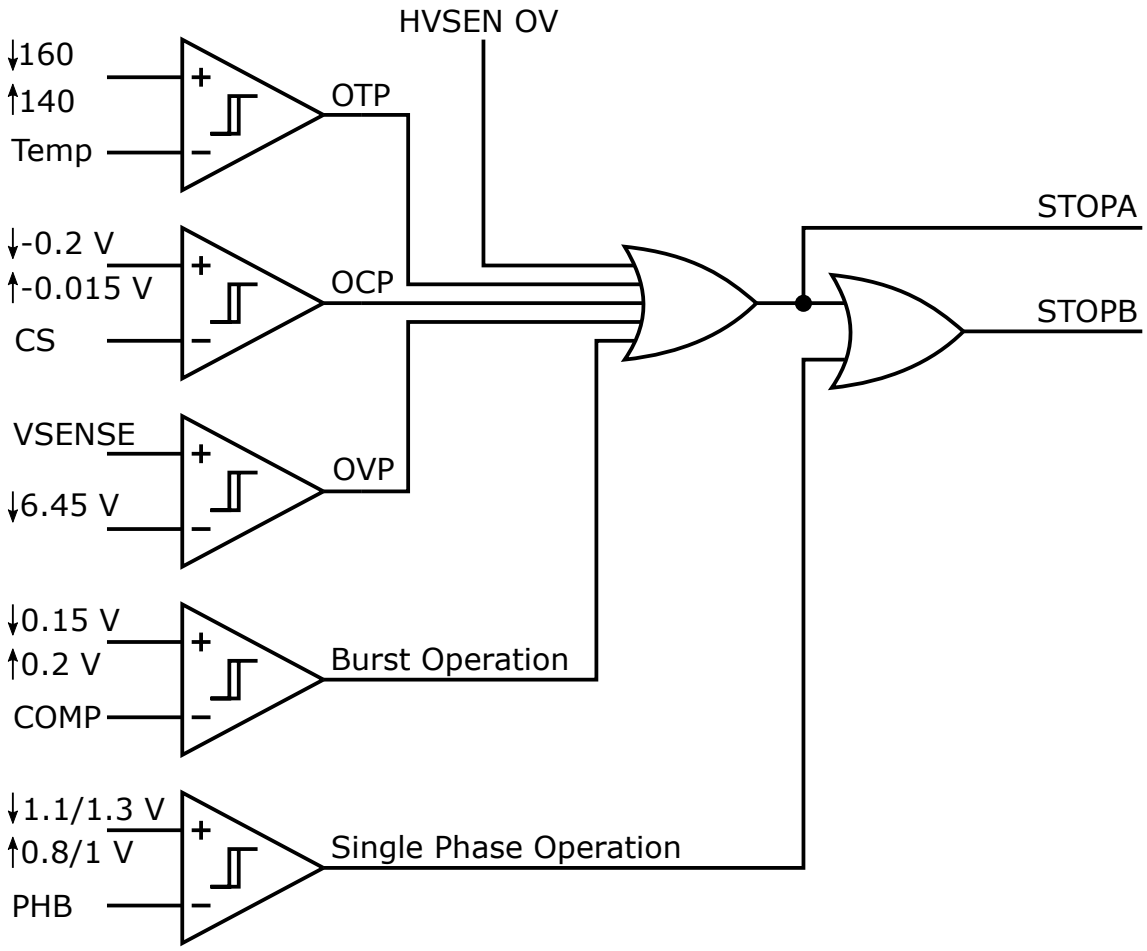


Fig. 8.2 Block diagram of protection circuits.

range for setting corresponding on-times. All parameters are sensed as peak values, the RMS values are derived by the following post processing. In the design, the $3M\Omega$ and $47k\Omega$ resistor are applied. Therefore the falling threshold is set to $65V$ and the rising approximately to $80V$ [51].

$$R_B = \frac{1.4 \cdot R_A}{V_{INmin} \cdot 0.75 \cdot \sqrt{2} - 1.4} = \frac{1.4 \cdot 3e^6}{85 \cdot 0.75\sqrt{2} - 1.4} = 47.32k\Omega \approx 47k\Omega \tag{8.25}$$

8.6.2 Over Voltage Protection

The one of the basic protection is an over voltage protection. For the over voltage protection it is applied two redundant sensing paths which prevent the corrector against the over-voltage conditions at the output. Two protection paths are located on the $VSENSE$ and $HVSEN$ pins. When the over voltage condition is detected on the one path at least, the corrector is shut down. The controller is re-enabled once the voltage decreases into the normal operation range. As a consequence, the PWM signals are generated normally. The $VCOMP$ voltage is not pulled low during the over voltage protection [51].

The resistor choice of the voltage divider 8.23 [51] determines also the primary over-voltage protection represented by the next equation 8.26 [51].

$$V_{OVP} = 6.45 \cdot \frac{R_C + R_D}{R_D} = 6.45 \cdot \frac{3e^6 + 4.7e^4}{4.7e^4} = 418V \tag{8.26}$$

The second sensing path, which is $HVSEN$ pin, is used for redundant over voltage protection and programming of the $PWMCNTL$ output. The output provides information about proper operation of the corrector for a downstream converter. The $PWMCNTL$ pin is pulled low if the output voltage is in the designed range. The pin can be used for enabling of the downstream converter. The following calculation describes the selection process of the voltage divider. First of all, it is necessary to determine the voltage level when the $PWMCNTL$ pin is activated. 90% of the nominal output voltage it seems appropriate 8.27 [51].

$$V_{OUT_{OK}} = V_{OUT} \cdot 0.9 = 390 \cdot 0.9 = 351V \tag{8.27}$$

The threshold and hysteresis are set by high and low side resistors of the voltage divider. If the high side resistor is set to $3M\Omega$ as well as in case of $VSENSE$ and $VINAC$ pins, the controller will provide $108V$ the hysteresis as is clear from the equation 8.28 [51].

$$Hysteresis = R_E \cdot 3.6e^{-5} = 3e^6 \cdot 3.6e^{-5} = 108V \tag{8.28}$$

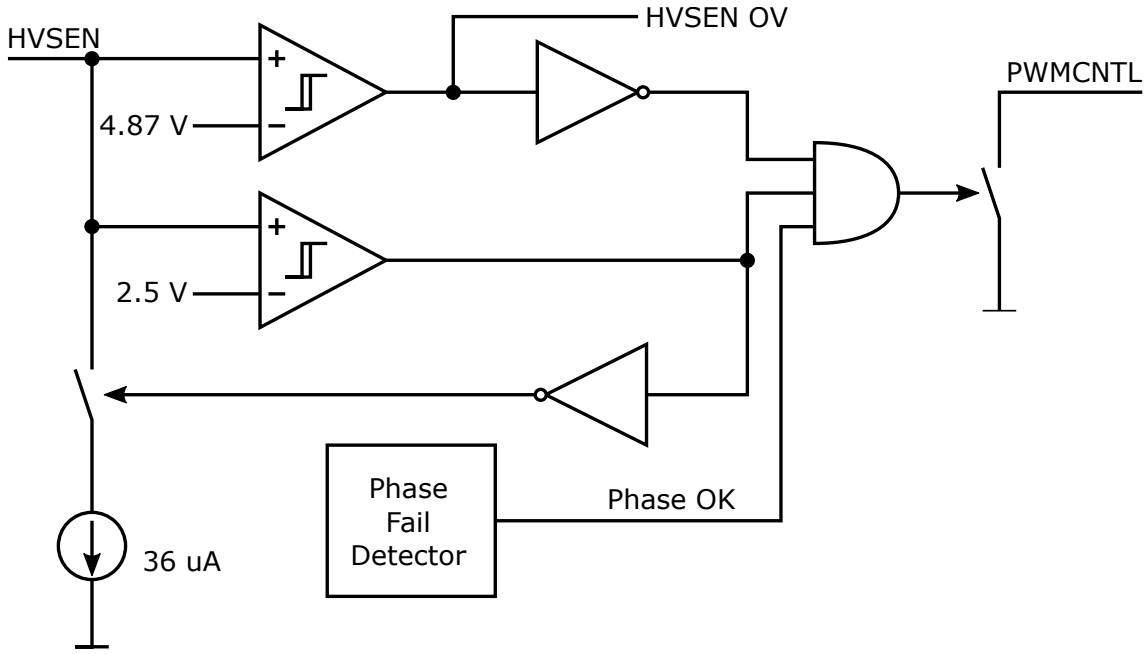


Fig. 8.3 Schematic diagram of the over voltage protection.

The *PWMCNTL* pin is pulled low when the voltage at the *HVSENSE* pin overcomes $2.5V$. The low side resistor provides a setting of the rising threshold. The equation 8.29 [51] represents calculation of the low side resistor.

$$R_F = \frac{2.5}{\frac{V_{OUT_{OK}}-2.5}{R_E} - 3.6e^{-6}} = 31.185k\Omega \approx 33k\Omega \tag{8.29}$$

It was used $33k\Omega$ resistor. Thus, the falling threshold can be computed by the following equation 8.30 [51].

$$V_{OUT_{min}} = \frac{2.5 \cdot (R_F + R_E)}{R_F} = \frac{2.5 \cdot (3.3e^5 + 3e^6)}{3.3e^5} = 229.773V \tag{8.30}$$

The *HVSEN* pin is used also for a fail safe over voltage protection as expresses the equation 8.31 [51]. The setting has to provide the protection level above a voltage level at the normal over voltage protection [51].

$$V_{OUT_{FAILSAFE}} = \frac{4.87 \cdot (R_F + R_E)}{R_F} = \frac{4.87 \cdot (3.3e^5 + 3e^6)}{3.3e^5} = 447.597V \tag{8.31}$$

8.6.3 Peak Current Limiting

The over current protection protects components of the power stage against the current stress during inrush, brownout recovery, and overload. The corrector applies a single shunt resistor which is located between the negative rectifier terminal and the power ground. The shunt resistor senses the total input current. The excessive value of the current causes that the PWM outputs are disabled until the input current decreases to zero. It precludes the corrector against the reverse recovery failures which is caused by a recovering after the brownout. Equation 8.32 [51] defines the inrush current during the starting sequence at low line [51].

$$I_{PEAK} = \frac{2 \cdot P_{OUT} \cdot \sqrt{2} \cdot 1.2}{\eta \cdot V_{INmin}} = \frac{2 \cdot 600 \cdot \sqrt{2} \cdot 1.2}{0.92 \cdot 85} = 26.042A \tag{8.32}$$

The current sense input is clamped to $0.2V$. Now it can be derived a value of the shunt resistor by the next equation 8.33 [51].

$$R_S = \frac{0.2}{I_{PEAK}} = \frac{0.2}{26.042} = 7.68m\Omega \approx 8m\Omega \tag{8.33}$$

A maximal dissipative power of the shunt is given by the expression 8.34 [51].

$$P_{RS} = \frac{P_{OUT}}{\eta \cdot V_{INmin}}^2 \cdot R_S = \frac{600}{0.92 \cdot 85}^2 \cdot 0.01 = 0.588W \tag{8.34}$$

When the over current condition is released, the PWM outputs are enabled. Both control signals operate temporarily in-phase. The in-phase operation causes that the over current threshold is multiplied by factor 2 due to the current ripple cancellation technique does not temporarily work [51].

8.6.4 Phase Fail Protection

The controller monitors a sequence of the pulses on the *ZCD* pins. When one *ZCD* pin remains idle for $14ms$ at least while the second phase switches properly, the $PWMCNTL$ pin is pulled high. This pin gives information about a proper operation of the corrector. If the corrector operates under the single phase operation, the phase failure feature is deactivated.

In the transition, a resonance of the drain-source capacitance and the boost inductor causes a reduction of the energy absorption at the low input voltage around $0V$. As a result, the harmonic distortion grows significantly. Therefore on-times of the transistors are prolonged when the instantaneous input voltage is around zero volts. Thanks to this feature, the power absorption at the low voltage is compensated [51].

8.6.5 Open Loop Protection

The controller consists an open-loop protection circuitry which defines a behaviour of the corrector when the $VSENSE$ voltage is not connected. The protection pulls the $VSENSE$ pin to low in this condition.

If the $VSENSE$ voltage drops below $1.2V$, the controller disables both gate drivers and $VCOMP$ pin is pulled low. The current consumption is significantly reduced. The controller is re-enabled when the $VSENSE$ voltage grows above $1.25V$. The gate drivers start a normal operation. An external grounding of the $VSENSE$ pin has same consequences, the controller is actively forced into a standby mode which consumes an incomparable lower supply current. It can be used in a case of the external shut down. If the condition is not present, the controller soft-starts [51].

8.6.6 Light-Load Operation

The controller is equipped by a light load optimization feature. When the load current is low, the $VCOMP$ voltage decreases as well. If the PHB pin is connected to $VCOMP$ pin and the voltage is $0.8V$ for low line or $1.1V$ at high line respectively, the branch B of the corrector stops a normal operation and an on-time of the branch A will be multiplied by the factor 2 due to the compensation. The burst mode is activated when a voltage on the $VCOMP$ pin drops under $150mV$. The burst mode is characterized by the cycle skipping [51].

8.6.7 Supply Under Voltage Protection

The controller consists also an under voltage protection. The supply voltage has to be within the range 13 to $21V$. If the controller is powered from a poorly regulated voltage supply, it is recommended to use an external clamp diode which protects the circuit against an excessive supply voltage. The under voltage protection disables the gate drives if the supply voltage drops below the threshold [51].

8.7 Loop Compensation

The controller uses an transconductance type of the error amplifier. Thanks to this solution, the impedance of the output network determines a transient response. The controller includes improvements which help to charge the compensation network in a case of the low $VSENSE$ voltage. When the voltage is below $5.815V$, the output of the amplifier is charged by an

additional $160\mu A$ current source. The transconductance of the amplifier equals to $g_m = 96\mu S$. These improvements enhance a charging speed of the compensation network [51].

The transfer function of the output voltage divider is defined as follows (the equation 8.35 [51]).

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6}{390} = 0.015 \tag{8.35}$$

A resistor R_Z regulates an output voltage ripple under 2% of the nominal output voltage [51].

$$R_Z = \frac{0.1}{V_{RIPPLE} \cdot H \cdot g_m} = \frac{0.1}{11 \cdot 0.015 \cdot 96e^{-6}} = 6.313k\Omega \approx 6k\Omega \tag{8.36}$$

A capacitor C_Z enhances a phase margin at $1/5^th$ of the switching frequency of the corrector [51].

$$C_Z = \frac{1}{2\pi \cdot \frac{f_{line}}{5} \cdot R_Z} = \frac{1}{2\pi \cdot \frac{50}{5} \cdot 6e^3} = 2.652\mu F \approx 2.2\mu F \tag{8.37}$$

A capacitor C_P improves a noise immunity of the corrector [51].

$$C_P = \frac{1}{2\pi \cdot \frac{f_{min}}{2} \cdot R_Z} = \frac{1}{2\pi \cdot \frac{3.8319e^4}{2} \cdot 6e^3} = 138.447pF \approx 150pF \tag{8.38}$$

8.8 Philosophy of the Interleaved Corrector

This section concentrates on the performance improvements of the active power factor correctors. The improvements consist of the special flat corrector design and additional control system. In this section, it was explored a possibility of control of the multiphase correctors. Simultaneously, the section is devoted to a developing of the flat corrector. The most of the APFCs are designed as a single boost topology. Disadvantages of this solution are a correction performance at low output power, and worse heat loss dissipation. The multiphase correctors solve both of these problems. The main idea of the multiphase correctors is interleaving of the individual correctors based on the boost topology [24].

Two phase interleaved correctors have a better power dissipation but the improved performance during adverse conditions. It is solved by a advanced power management. The corrector was designed as a flat profile corrector with embedded components and planar inductors. The control system of the power management is based on the STM32F4 discovery kit which measures input and output parameters.

As a consequence, it produces the control signals for an operation change. The experimental results ((8.14) and (8.15)) of the single phase and interleaved operation were used for a setting convenient borders between operations. The results indicate that the advanced

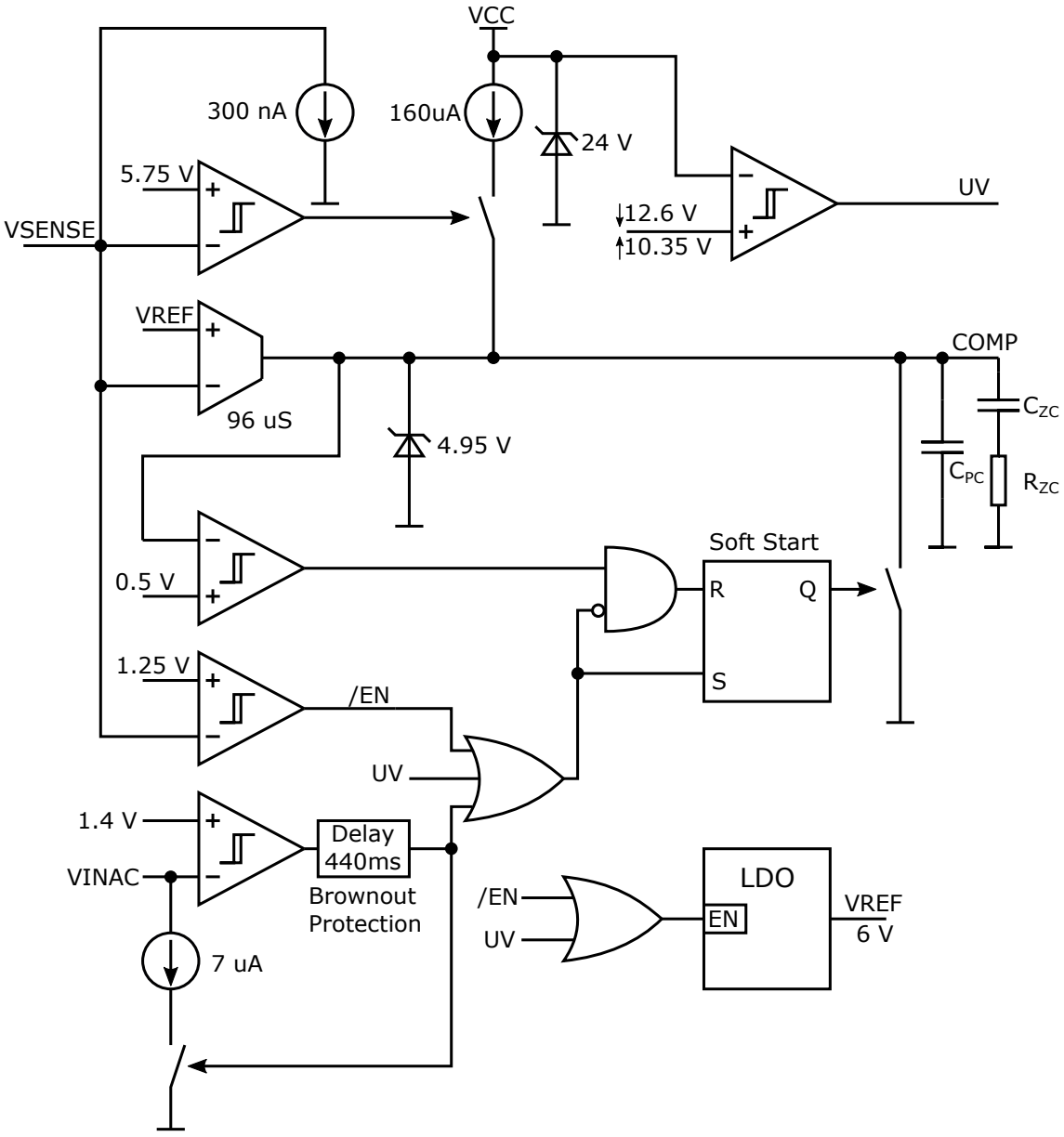


Fig. 8.4 Block diagram of the error amplifier.

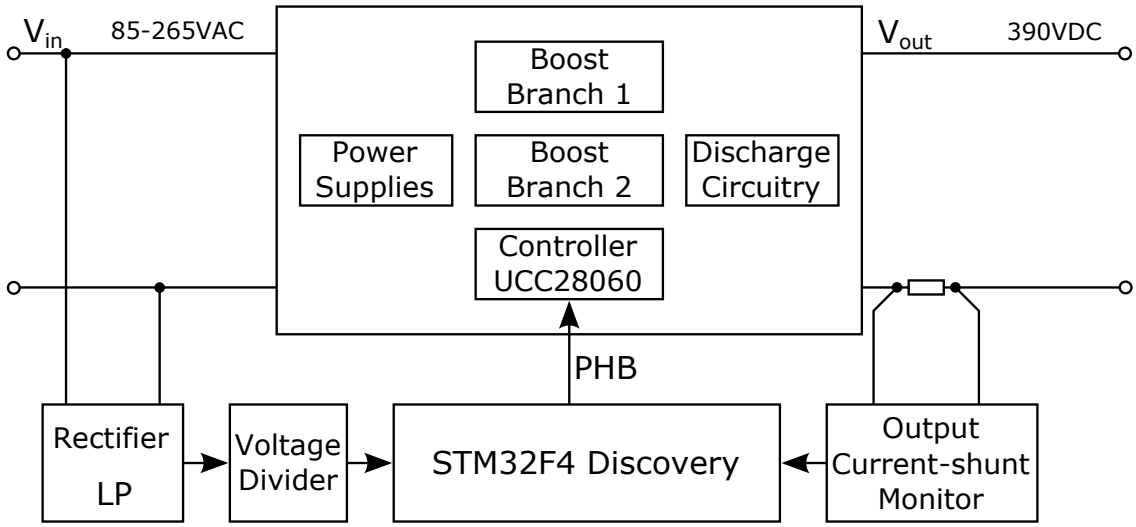


Fig. 8.5 Block diagram of the interleaved corrector.

power management enhances effectively PF correction and improves the overall efficiency at light load [23].

The figure 8.5 outlines the proposed block diagram . The backbone of the corrector makes a pair of the boost converters and analog PFC controller. The corrector is based on the natural interleaving method, which is implemented by the control circuit. The block diagram shows also other subsystems which will be described in the hardware implementation chapter.

8.9 Power Management Implementation

This section is devoted to the implementation of the power management of the corrector. The borders between single phase and interleaved operation should be variable due to a lot available conditions. They are influenced by the variable input voltage and load of the corrector. The figure 9.11 shows a flow chart of the implementation.

The first block of the flow chart provides the acquisition of measured input and output parameters. An averaging function is implemented due to the switching noise of the corrector. The next block is responsible for a calculation of the required parameters.

Then the comparative blocks determine a type of the operation. The borders between single phase and interleaved operations are defined according to the empirical findings. The experimental results are shown in the figures 8.14 and 8.15. According to the measurement it was decided $0.25A$ at low line and $0.5A$ at high line as borders between the single phase and interleaved operation. A hysteresis is determined to $0.1A$. The border between a high line and low line was defined to a $200V$ amplitude of the input voltage. A hysteresis is set to $20V$.

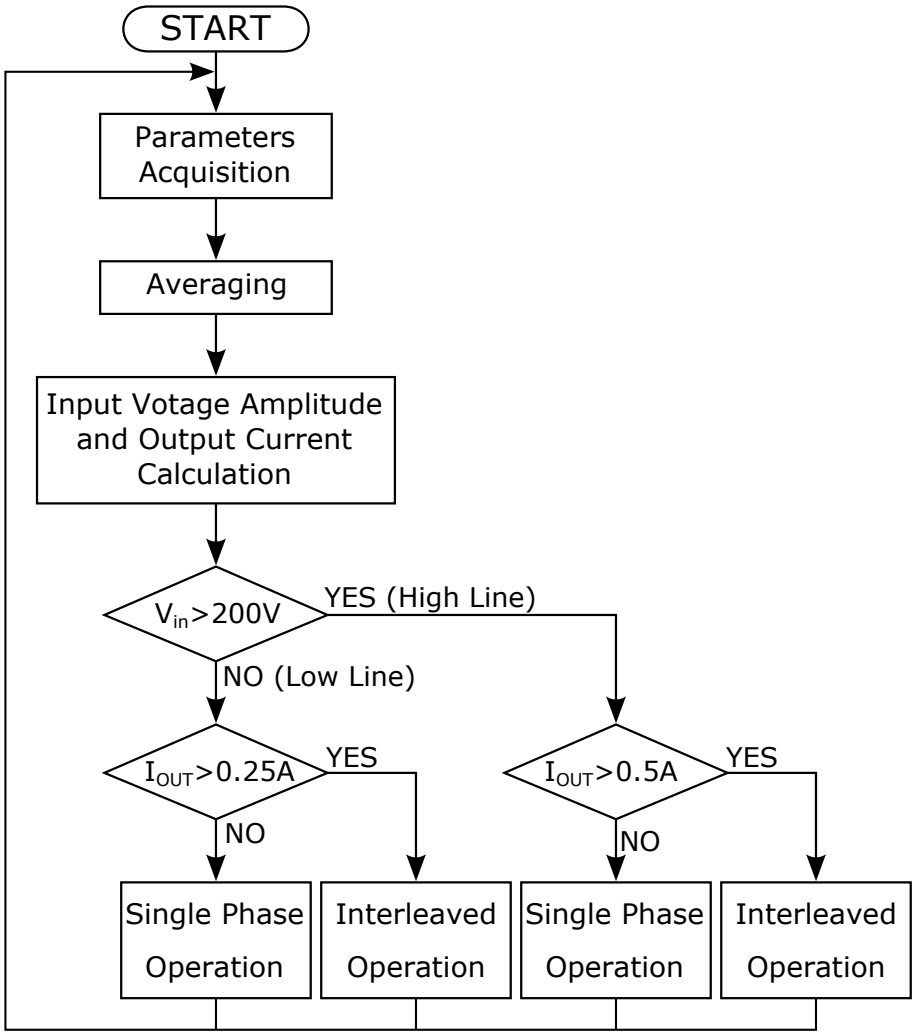


Fig. 8.6 Flow chart of the interleaved corrector.

The main benefit is a distribution of the tasks into two controllers. The analog controller is responsible for low level control. Contrary, the microcontroller serves only high level tasks [23].

8.10 Hardware Implementation

The corrector was built on a two layer printed circuit board (PCB) with dimensions $162x144mm$. The design respects a flat profile of the final device. The height of the corrector does not exceed $22mm$. Due to height of several components, these components were designed as embedded into the PCB. This solution was applied for EMI filter, bulk capacitors, and foil capacitors.

The power inductors were constructed as planar with auxiliary winding on the main board and three power windings pressed on the top layer. This arrangement allows to change position and count of the power layers during a development stage. Surface mounted packages are used also for switching elements (the boost diodes, the MOSFETs) on the board.

Heat sinks, which are copper polygons, have two functions. The first one is the heat transfer from a package to the ambient. The second one is a current conduction. For the power transistor a double sided heat sink layer is used due to an improved heat transfer from the transistor to the ambient.

The controller is powered by the step down converter directly from the line voltage without a galvanic isolation. This solution can also be called as Off-Line Switcher. It was selected owing to an absence a downstream converter. Generally, the power supply of the controller is solved by an auxiliary winding of the downstream converter transformer. An output current-shunt monitor, which is needed for a power management, requests a 3.3 voltage level. The linear power supply, which is connected in cascade with previous buck converter, produces the required voltage.

The output current-shunt monitor produces information about the output current. The current-shunt monitor is composed of the shunt resistor 0.02Ω and the differential amplifier with $40dB$ gain [56]. The shunt voltage can be computed by the equation 8.39 [23].

$$V_{shunt} = R_{shunt} \cdot I_{out} \cdot gain \tag{8.39}$$

If it is used for a calculation the $600W$ maximal output power, the output voltage equals to $390V$ and output current to $1.539A$. Then the maximal shunt voltage is calculated by next equation 8.40.

$$V_{shunt} = 0.02 \cdot 1.539 \cdot 100 = 3.078V \tag{8.40}$$

The shunt signal in range 0 - $3.078V$ is used for a monitoring the output power.

The input voltage sensing is provided by two individual resistor dividers. The first divider provides information about an input voltage for the controller. The values of the individual resistors were discussed in one previous section.

The line voltage for second divider is separately rectified and filtered by capacitor $470nF$. The second divider creates a voltage level suitable for microcontroller. An upper value consists of three resistors and reaches $3M\Omega$. The maximal input RMS voltage is $250V$. The maximum peak input voltage will be derived from the next expression 8.41 [23].

$$V_{in(max),peak} = V_{in(RMS),max} \cdot \sqrt{2} = 250 \cdot \sqrt{2} = 354V \tag{8.41}$$

The voltage divider has to provide an output voltage within the input voltage range of the analog-to-digital (ADC) converter of the microcontroller. The input voltage range of the ADC is from 0 to $3.3V$. The bottom resistor can be calculated as follows [23].

$$R_{in2} = R_{in1} \cdot \frac{V_{ADC(max)}}{V_{in(max),peak} + V_{ADC(max)}} \tag{8.42}$$

$$R_{in2} = 3e^6 \cdot \frac{3}{354+3} = 25.21k\Omega \tag{8.43}$$

Based on this calculation it was chosen a standard $27k\Omega$. The maximal voltage of the divider output can be verified by the following expressions.

$$V_{ADC(max)} = V_{in(max),peak} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}} \tag{8.44}$$

$$V_{ADC(max)} = 354 \cdot \frac{27e^3}{3e^6 + 27e^3} = 3.15V \tag{8.45}$$

For controlling of the analog PFC controller is used a PHB pin which is driven by an external transistor.

Top and bottom layout patterns are shown in the figures 8.7 and 8.8. Next three figures are devoted 3D models of the board. The last figures show a photo of the hardware realization.

8.11 Bill of Material

This section is devoted to a costs estimation for the prototype of the corrector. The price column includes all components in the row. The estimation is used for a final comparison of the prototypes. The total costs for the prototype with $UCC28060$ controller reaches 99.11 €.

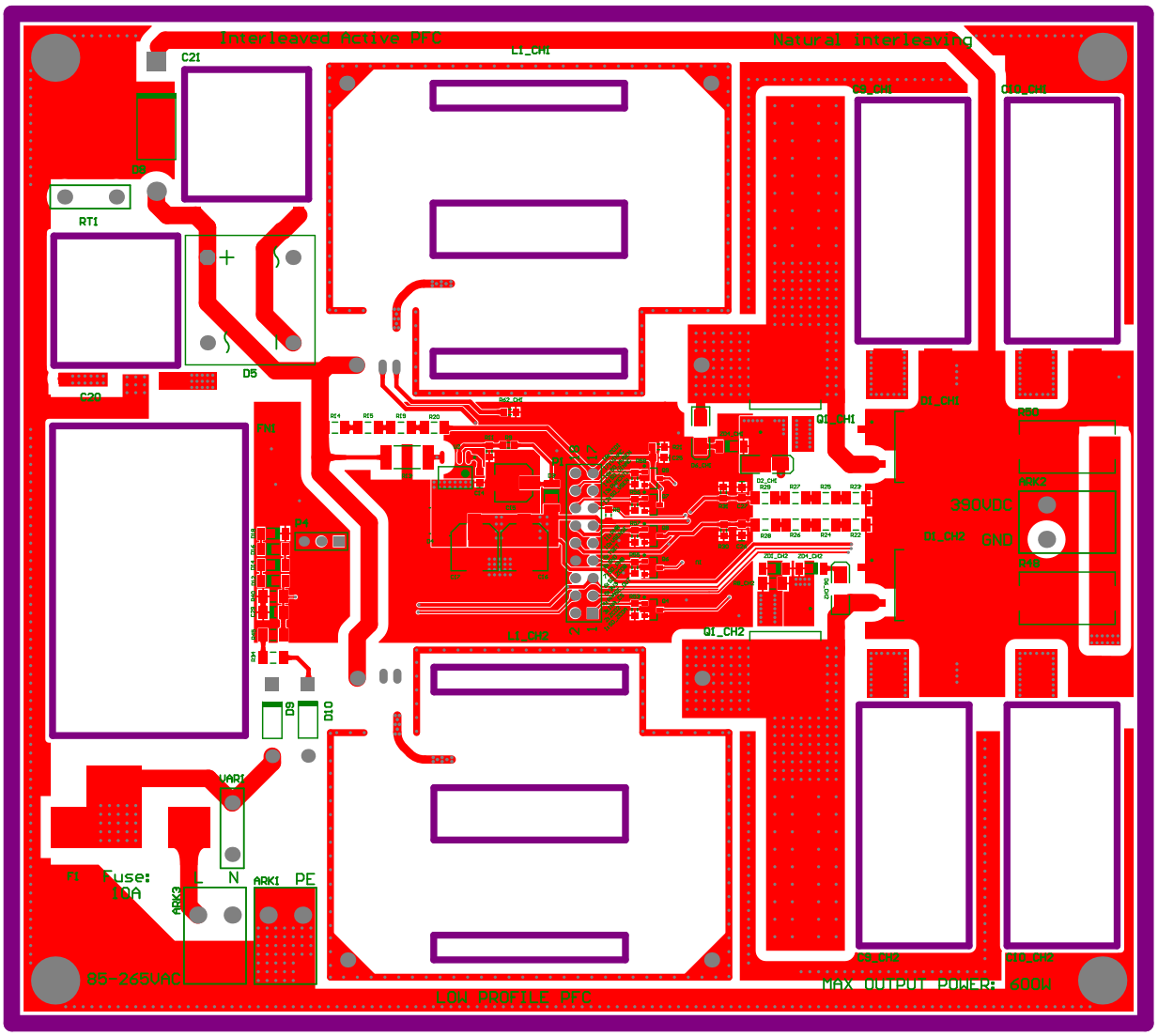


Fig. 8.7 Layout of the corrector - top view (1:1 scale).

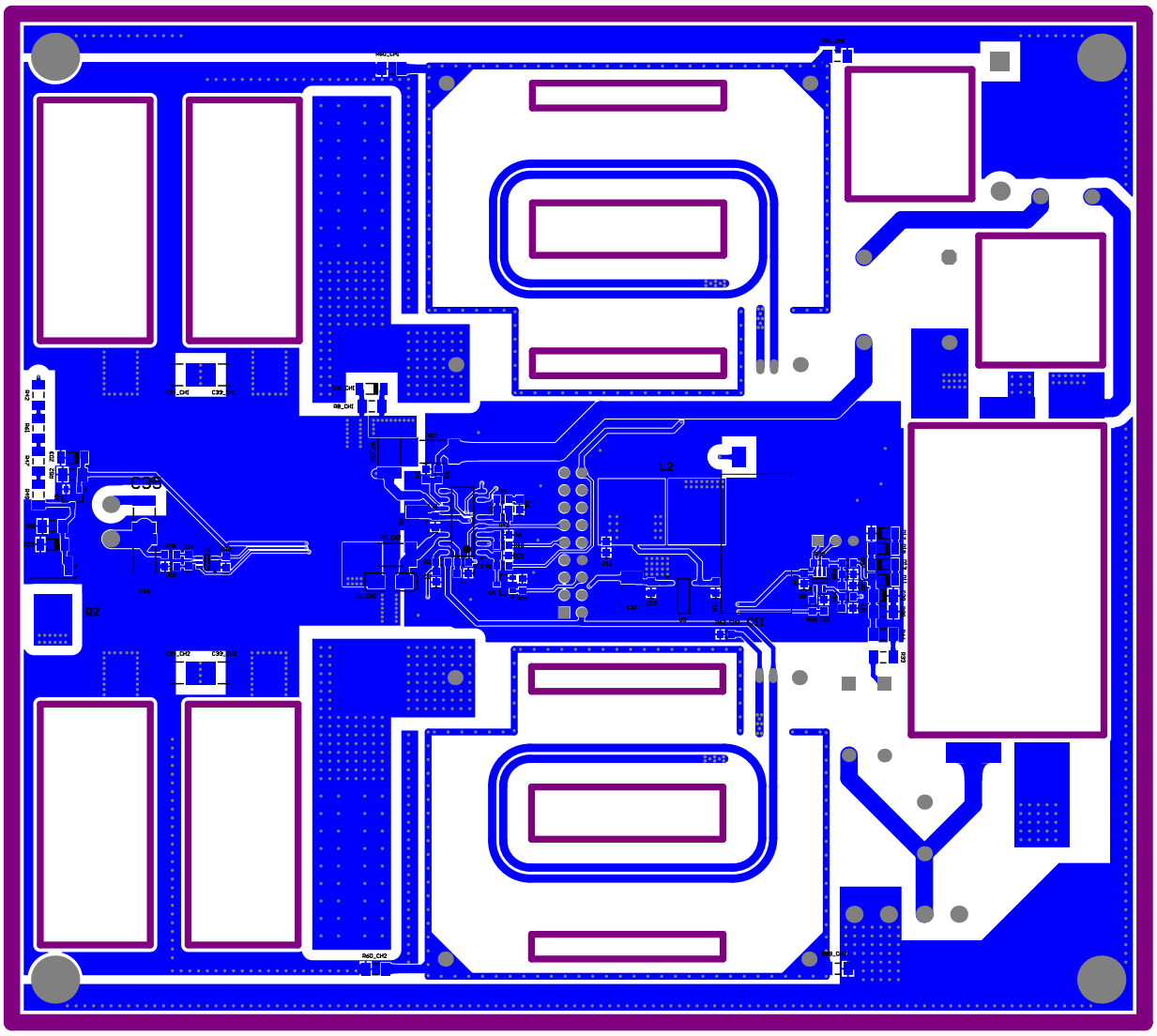


Fig. 8.8 Layout of the corrector - bottom view (1:1 scale).

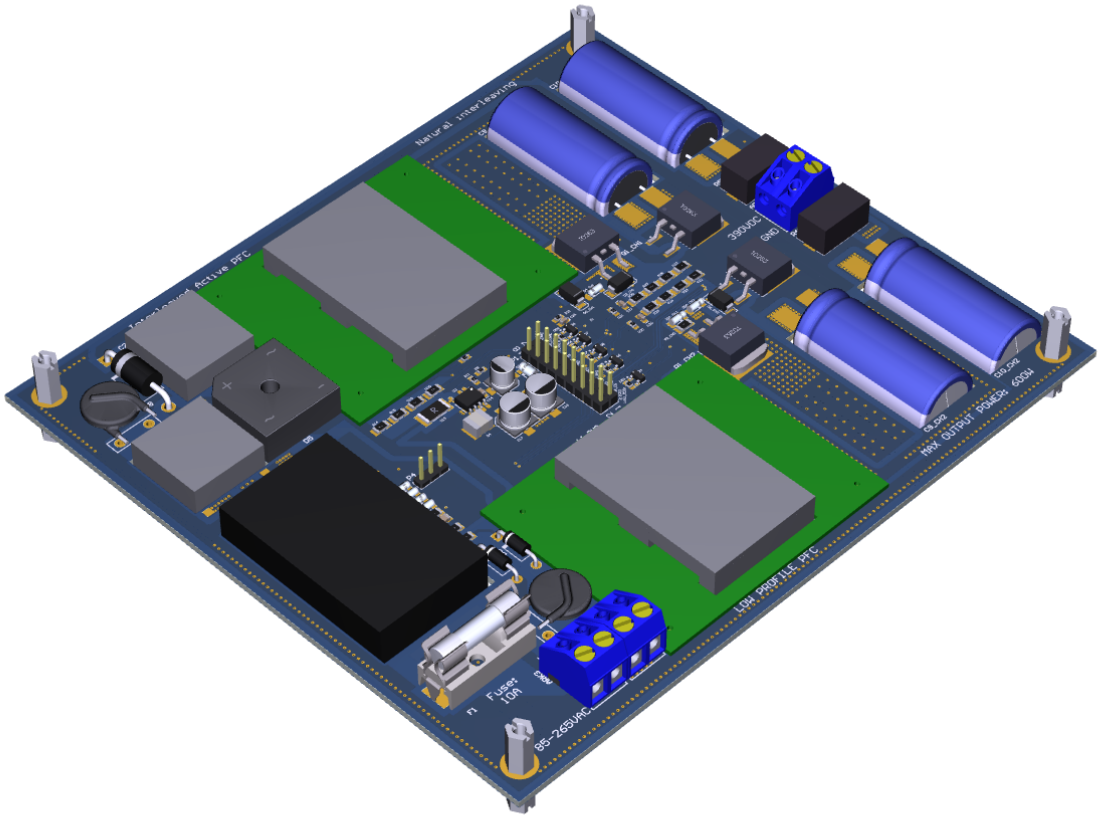


Fig. 8.9 3D model - top view.

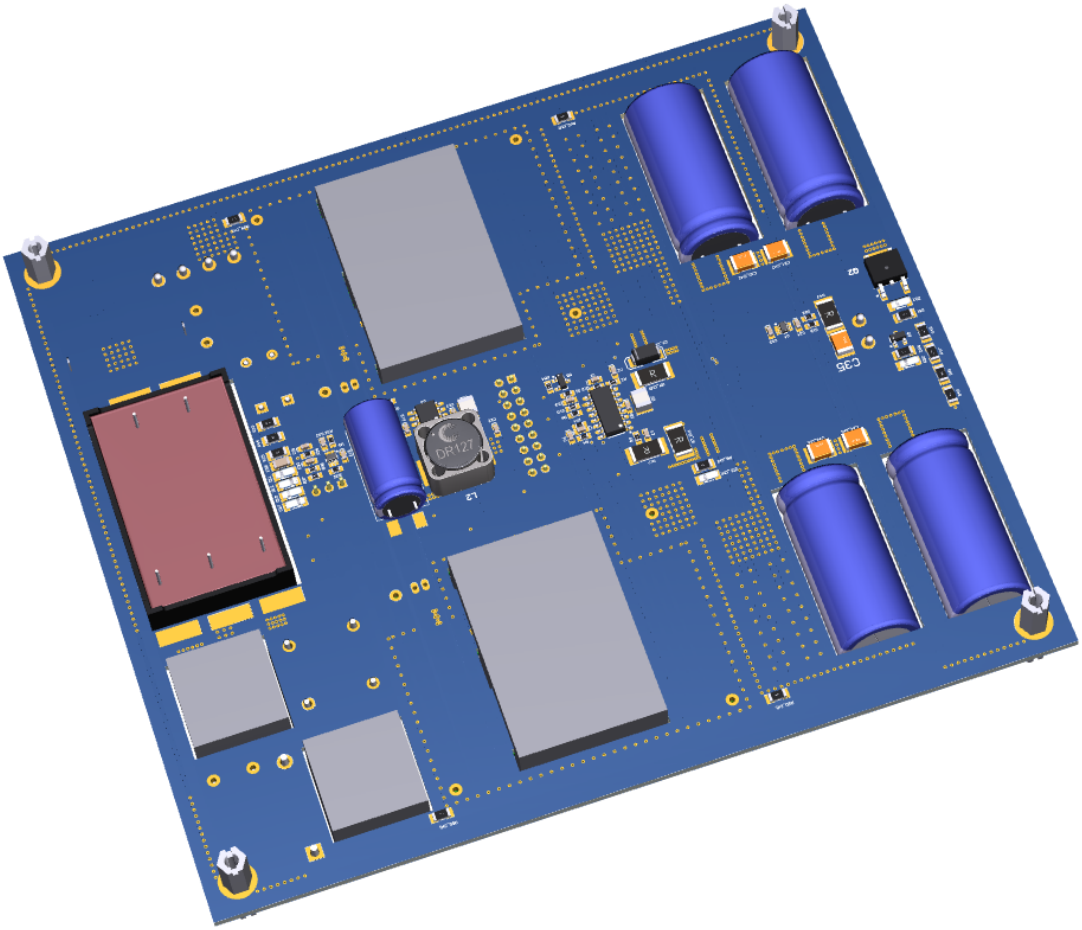


Fig. 8.10 3D model - bottom view.

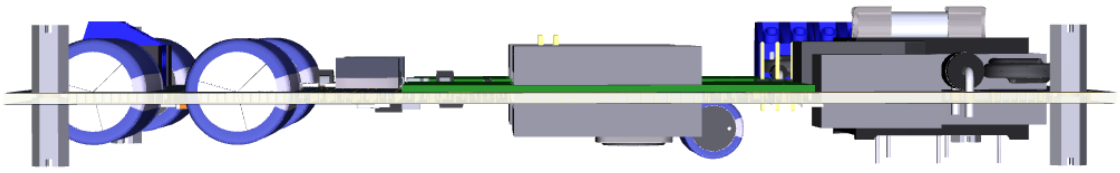


Fig. 8.11 3D model - side view.

Fig. 8.12 Top view of the interleaved corrector.

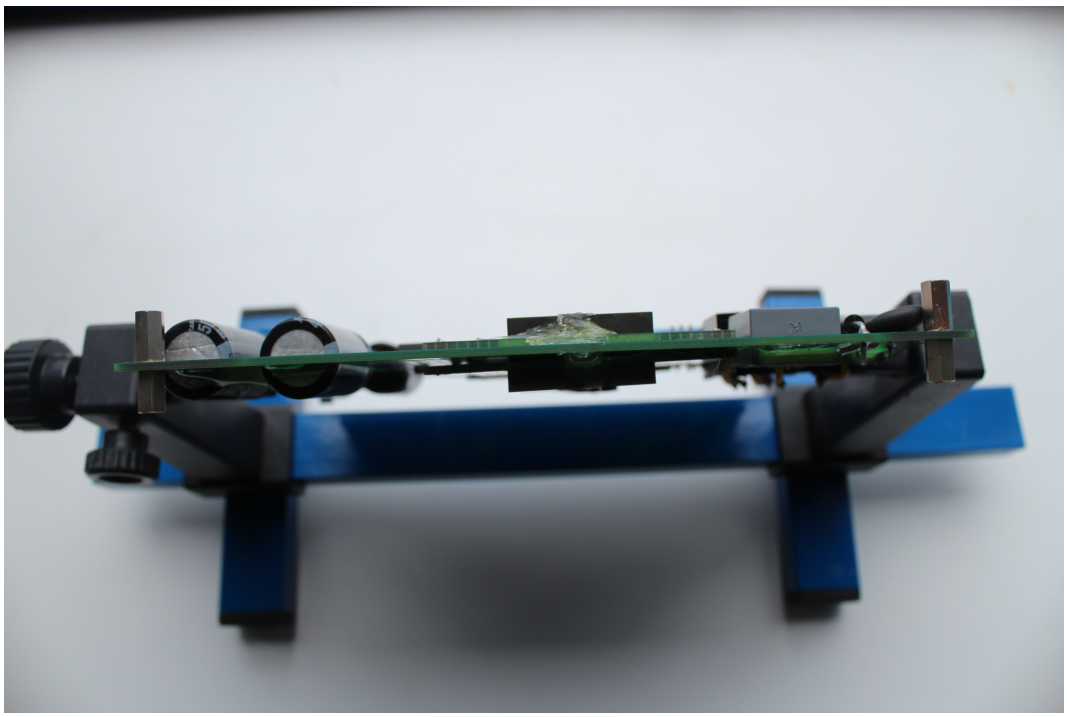


Fig. 8.13 Side view of the interleaved corrector.

Table 8.2 Simple bill of the material part 1 (UCC28060).

Designator	Type	Quantity	Price [€]
ARK1, ARK2, ARK3	ARK power connector 2-pin	3	1.4
C1, C2, C3, C4, C6, C7, C8, C12, C13, C14, C18, C19, C22, C23, C24, C25, C26, C27, C30, C31	SMD ceramic chip capacitor $100nF$ 0603	20	0.78
C5, C32	SMD tantal capacitor $2.2\mu F/35V$ 1411	2	0.42
C9-CH1, C9-CH2, C10-CH1, C10-CH2	THT radial electrolytic capacitor $82\mu F/450V$	4	11.64
C11	THT radial electrolytic capacitor $1\mu F/350V$	1	0.24
C15	SMD radial electrolytic capacitor $10\mu F/50V$	1	0.25
C16, C17	SMD radial electrolytic capacitor $10\mu F/50V$	2	0.5
C20, C21	THT foil capacitor $470nF/275VAC$	2	1.08
C28, C29	SMD ceramic chip capacitor $100nF$ 1206	2	0.31
C33-CH1, C33-CH2, C34-CH1, C34-CH2, C35	SMD ceramic chip capacitor $100nF/630V$ 2512	5	3
D1-CH1, D1-CH2	Ultrafast rectifier $FESB16JT$	2	2.74
D2-CH1, D2-CH2	Schottky diode $40V/1A$ $FMKA140$	2	0.04
D3	Universal diode $BYD37M$ $1000V/1A$	1	0.11
D4	Ultrafast $600V/1A$ $MURS160-13-F$	1	0.36
D5	Bridge rectifier $600V/10A$ $KBPC1006$	1	1.32
D6-CH1, D6-CH2	Transil $550V$ P4SMA550A	2	0.96
D8	Universal diode $1000V/3A$ 1N5408	1	0.29
D9, D10	Diode $1000V/1A$ 1N4007	2	0.18
D11, D12, D13, D14, D15, D16, D17, D18	Diode $100V/150mA$ 1N4148	8	0.64
F1	Fuse $10A/250V$ + fuse holder	1	0.5
FN1	EMI Schaffner $FN402-6.5-02250V/6.5A$	1	10.48
L1-CH1, L1-CH2	Planar Inductor	2	3
L2	Power inductor $1mH/260mA$ DR127-102-R	1	1.06
P1	Header $9x2$	1	0.6
P4	Header $3x1$	1	0.12
Q1-CH1, Q1-CH2	Power MOSFET $SPB20N60C3$	2	8.44

Table 8.3 Simple bill of the material part 2 (UCC28060).

Designator	Type	Quantity	Price [€]
Q2	Power MOSFET $IRFRC20PBF$	1	0.87
Q3, Q4, Q5, Q6, Q7, Q8, Q9	Power MOSFET $SQ2360EES$	7	2.31
R1, R2, R3, R4, R5, R6, R9, R10, R11, R12, R16, R18, R21, R30, R31, R32, R35, R36, R37, R38, R41, R53, R54, R55, R56, R57, R58, R62-CH1, R62-CH2	SMD chip resistors 0603	29	1.13
R7-CH1, R7-CH2, R13	SMD chip resistors 10Ω 2512	3	0.3
R17	SMD chip resistors $8m\Omega$ 2512	1	0.48
R43	SMD chip resistors $20m\Omega$ 2512	1	0.48
R8-CH1, R8-CH2, R14, R15, R19, R20, R22, R23, R24, R25, R26, R27, R28, R29, R33, R34, R39, R40, R42, R44, R45, R47, R49, R51, R52, R59-CH1, R59-CH2, R60-CH1, R60-CH2, R61	SMD chip resistors 1206	30	2.33
R48, R50	SMD power resistor $SMF5W33KJ$	2	1.79
RT1	Inrush NTC termistor $250V/5A$	1	0.8
U1	PFC controller $UCC28060$	1	2.57
U2	LinkSwitch $LNK304$	1	1.26
U3	Low drop voltage regulator $LE33CD$	1	0.81
U4	Current shunt monitor $INA214$	1	1.28
U5	Analog comparator $ADCMP608BKSZ-R2$	1	2.44
VAR1	Varistor $S14K275$	1	0.23
ZD1-CH1, ZD1-CH2, ZD2, ZD3, ZD4-CH1, ZD4-CH2	Zener diode $TZM5248B-GS08$ $18V/0.5W$	5	0.9
PCB	PCB $162x144mm(2.33dm^2)$	1	28.67
Total			99.11

8.12 Experimental Results

8.12.1 Performance Measurements

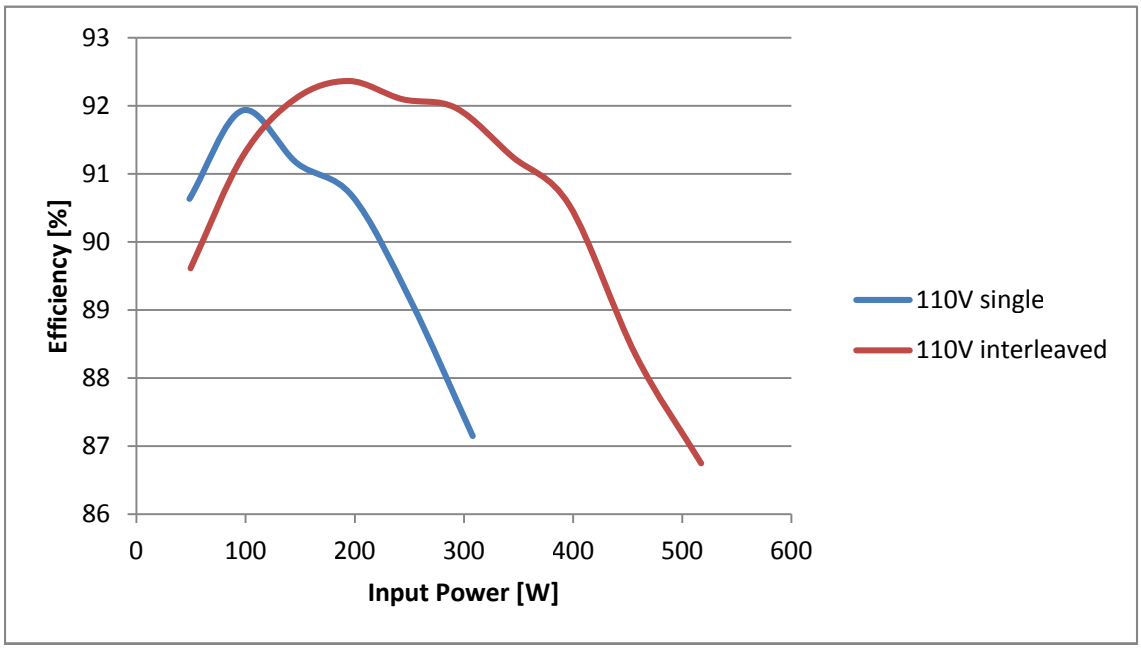
The measurement was carried out by the schematic diagram shown in the section 6.5. The graph 8.14 depicts the efficiency and correction performance at low line ($110V$). The results at high line are presented in the figure 8.15. All graphs consist of two curves for different operational conditions. The red curve represents single operation of the corrector and blue one interleaved operation. The efficiency at low line reaches 92.3%, the corrector operated under interleaving. The graph shows areas where single operation and interleaved operation improves the corrector efficiency. The single phase operation is beneficial up to $100W$ in case of the efficiency and up to $200W$ in case of correction performance.

The similar situation occurs at high line with the different intersection of the curves. The single operation is advantageous up to $200W$. For higher input power it makes sense the interleaved operation.

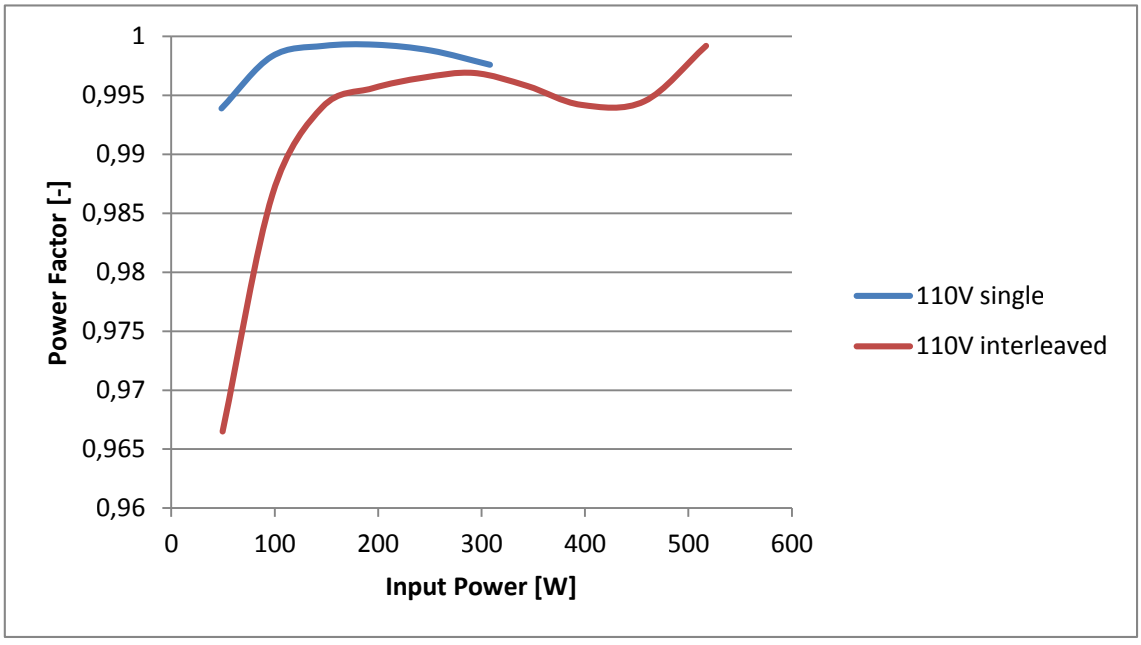
The last two graphs show situation when the power management is enabled 8.16. That means if the single operation is beneficial, the corrector will work with one phase and vice versa. The intersection is variable and is dependent on line voltage. If the line voltage is low, the intersection is shifted to lower power. If the line voltage goes up, the intersection will rise as well. The technique improves performance of the corrector at low power condition and enhances power dissipation at higher powers due to twice number of power components.

8.12.2 Harmonic Content According to ČSN EN 61000-3-2 Standard

The corrector has to fulfill harmonic order limits for the line current according to the ČSN EN 61000-3-2 standard [42]. The measurement of the harmonic content of the input current use same setup as performance measurement. The harmonic content was investigated at three input power values $100W$, $300W$ and $500W$. The investigation was carried out for single 8.17 and interleaved operation 8.18. All figures include a harmonic order current limit which is calculated according to the ČSN EN61000-3-2 standard which defines two limits for D class. First limit is related to current over the power (mA per W). This limit is dependent on the input power of the corrector. The second limit defines absolute limit for the standard. The measurement used only first criterion for comparison the measured data to the limits described in the standard. The comparison shows that the experimental results fulfilled limits set by the standard [42].

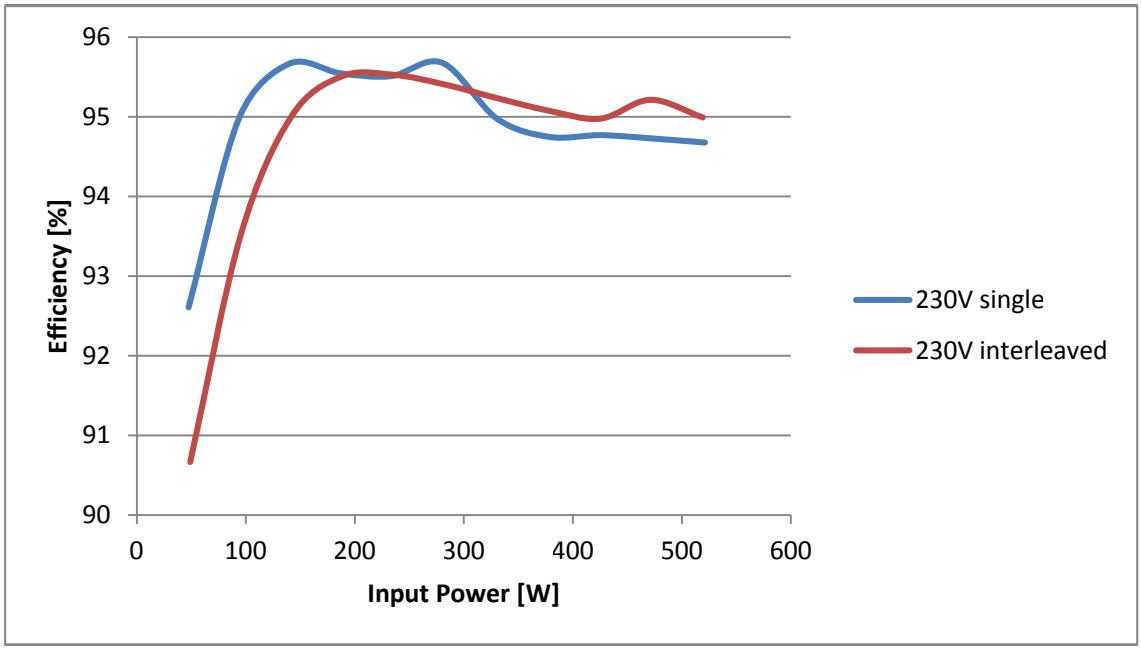


(a)

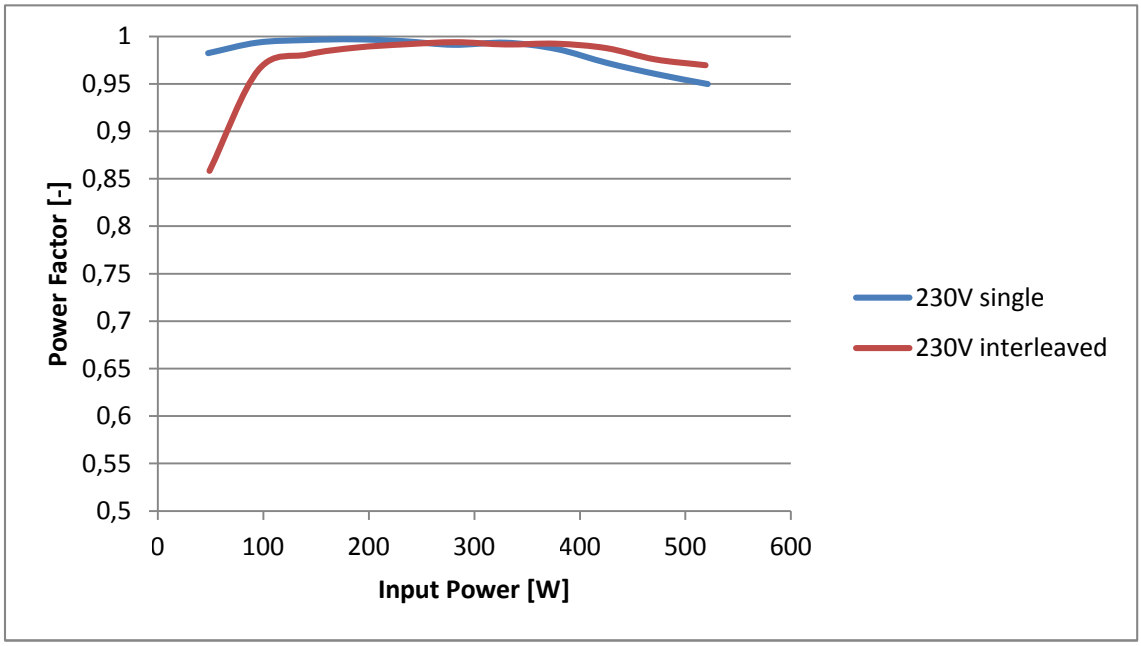


(b)

Fig. 8.14 Performance measurement of the corrector based on the UCC28060 controller a) efficiency at 110V, b) Power Factor at 110V.

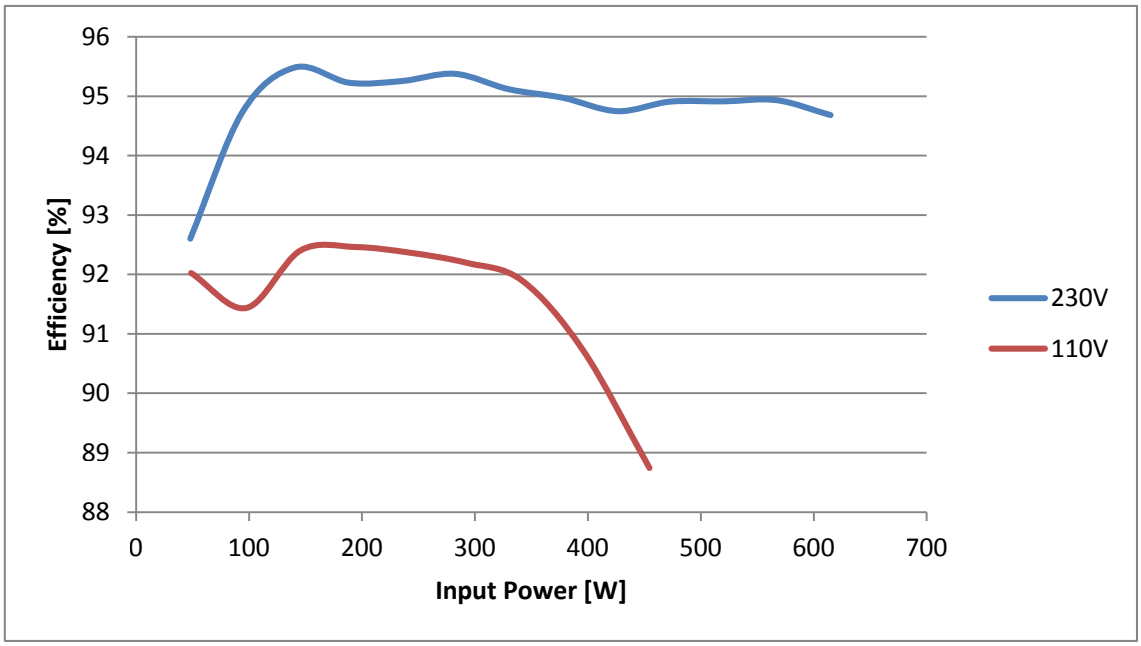


(a)

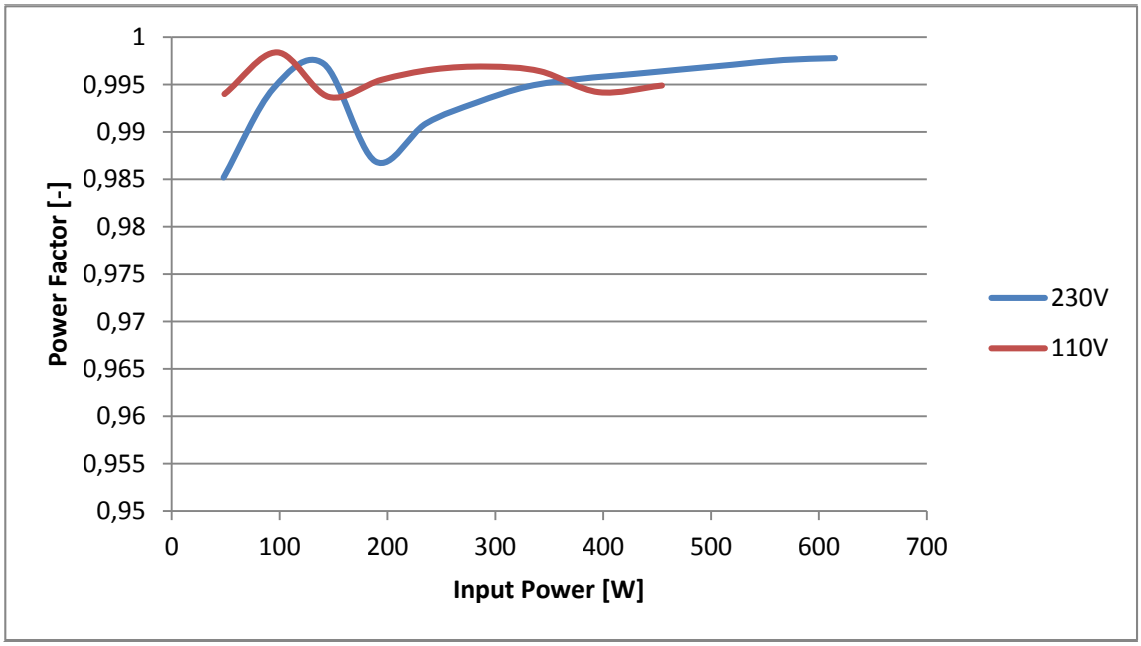


(b)

Fig. 8.15 Performance measurement of the corrector based on the UCC28060 controller a) efficiency at 230V, b) Power Factor at 230V.

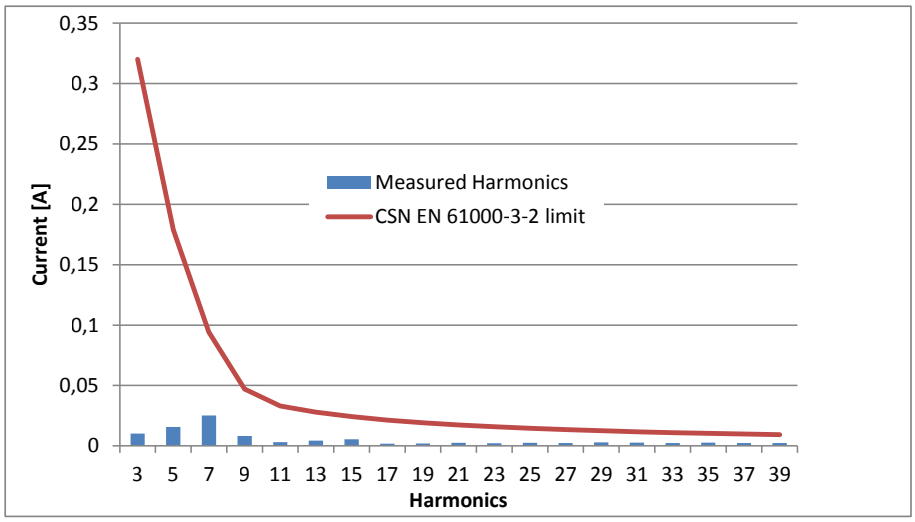


(a)

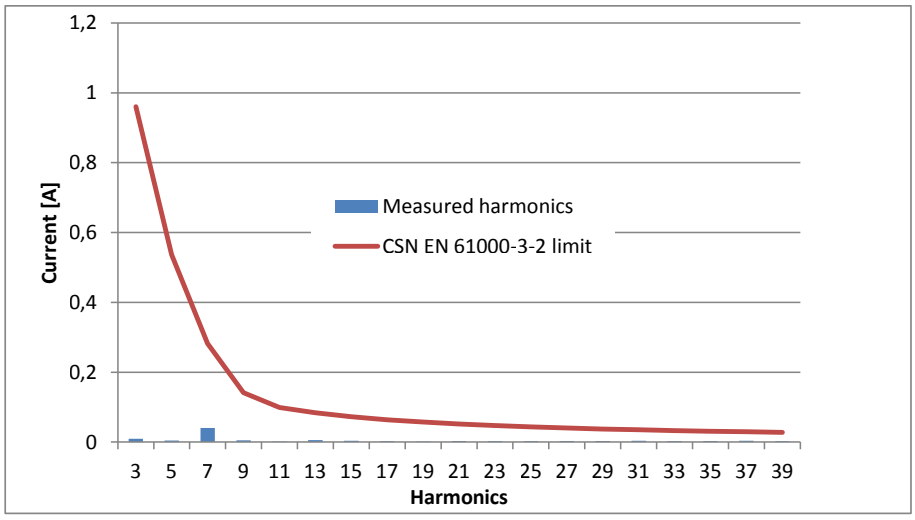


(b)

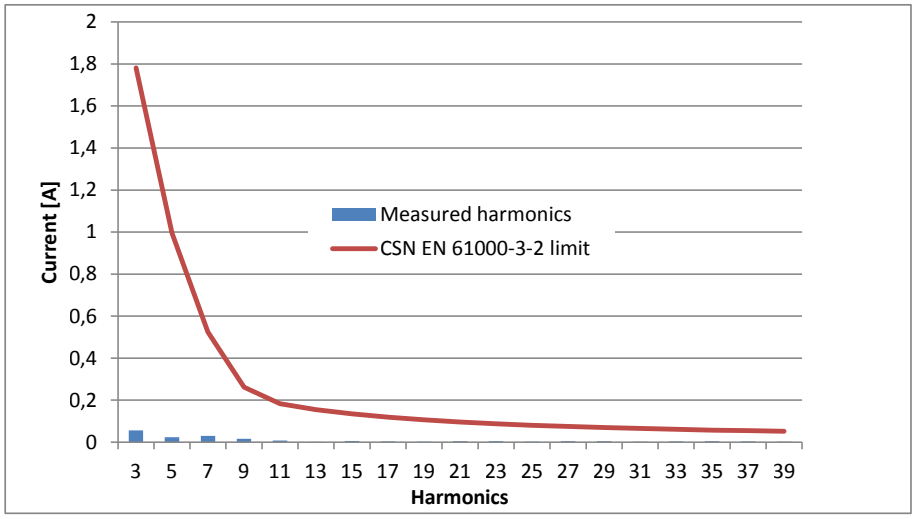
Fig. 8.16 Performance measurement of the corrector based on the UCC28060 controller with power management feature a) efficiency, b) Power Factor.



(a)

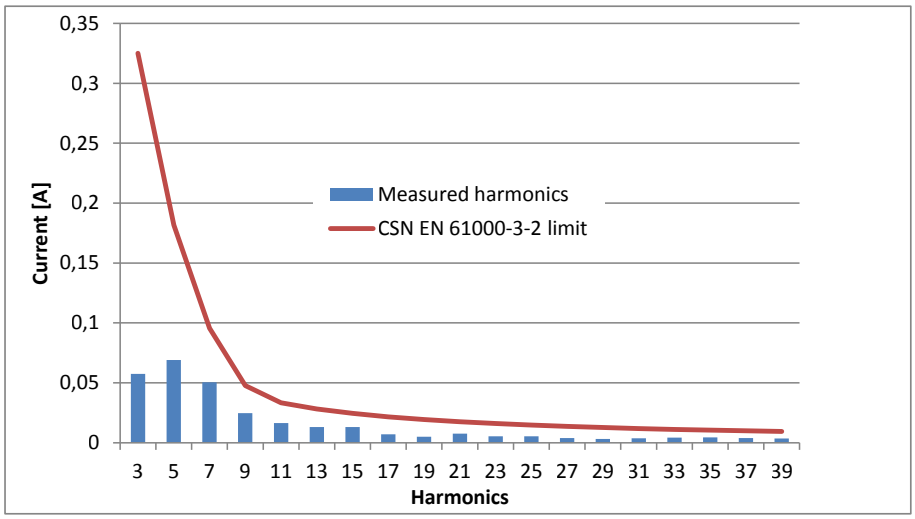


(b)

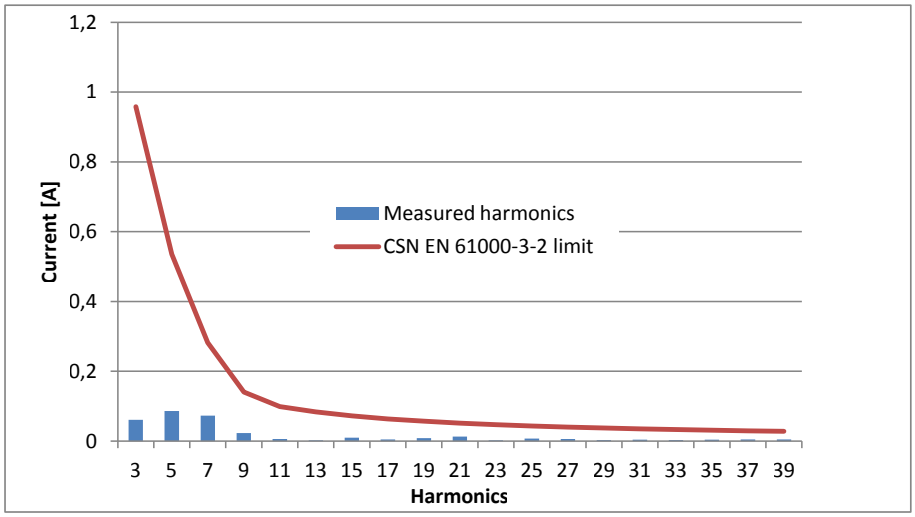


(c)

Fig. 8.17 Harmonics content of the corrector at different loads (interleaving is disabled), a) 100W, b) 300W, c) 500W.



(a)



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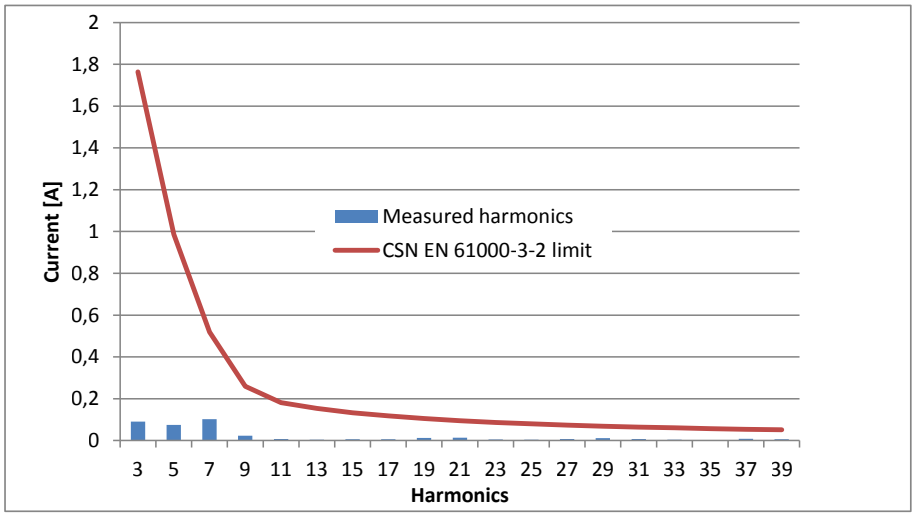


(c)

Fig. 8.18 Harmonics content of the corrector at different loads (interleaving is enabled), a) 100W, b) 300W, c) 500W.

8.12.3 EMC Measurement

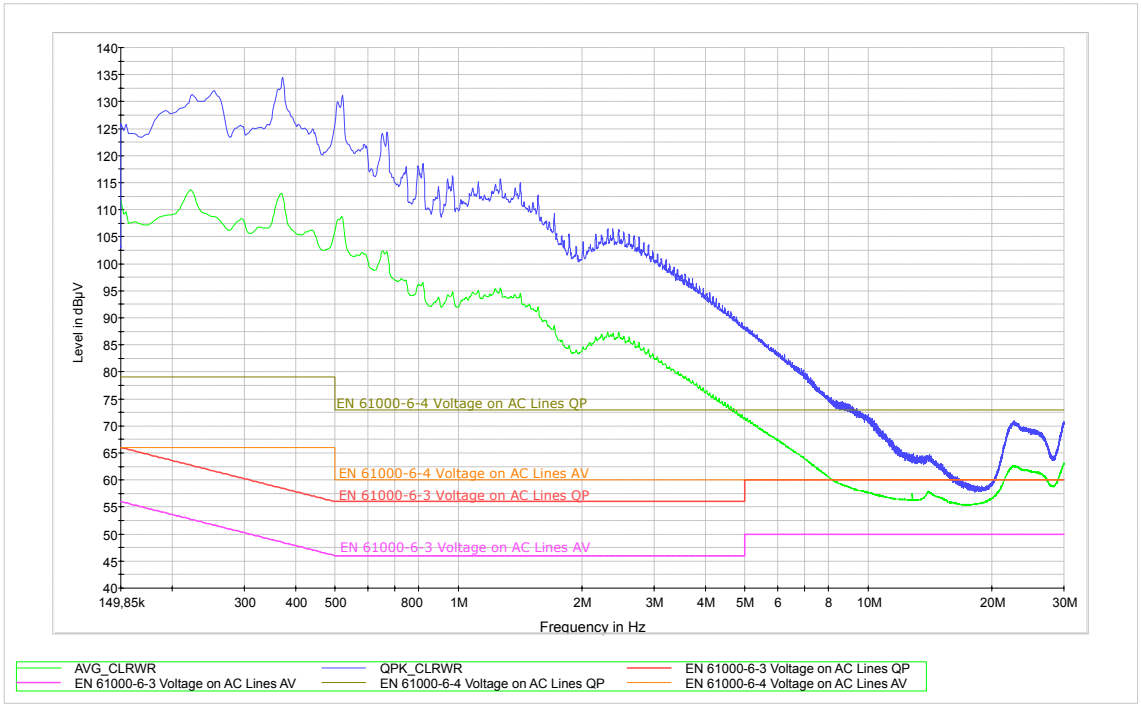
The conductive EMI test was performed according to the section 6.7. The measurement was performed into two stages. First stage was characterized without EMI optimization of the corrector. The corrector operates under CrM therefore the switching frequency is variable in wide range $38kHz$ to $500kHz$. The gate resistors 4.7Ω resistivity gate resistor. The high-speed MOSFET transistors was used as switching elements. The efficiency reaches 96.5% at $230V$ and 94% at $110V$ line voltage. The using MOSFET transistors with 4.7Ω gate resistor causes a short rise and fall times of the switching. The main benefit is low switching losses but high EMI emission at high frequency harmonics.

The design of the board has direct impact on the EMI performance. The figure 8.19 includes continues spectrum of harmonics due to variable switching frequency. Due to the short rise and fall times the high frequency content is rose several peaks overcome the limit line for EMI standard ČSN EN 61000-6-4 [44].

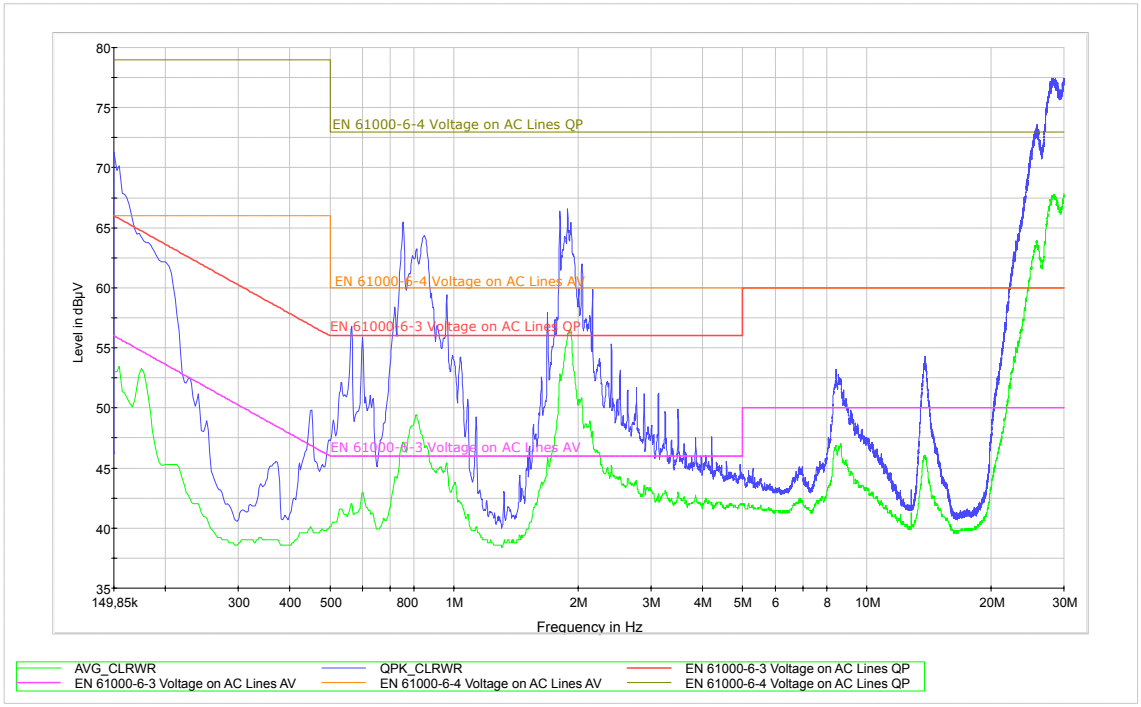
Second measurement was carried out with some optimization. The gate resistors were replaced by 10Ω gate resistors. The transistor is improved by snubber circuits. Both cases use same EMI filter Schaffner FN2090-10-06 [40]. Second figure 8.19 shows the experimental results at the second hardware setup. The graph includes flat and smaller peaks of the harmonics. The spectrum is continuous in the full scale. The ČSN EN 61000-6-4 standard [44] is not fulfilled due to the overcomes of the measured data. The better results can be reached by a following complete revision of the layout.

8.12.4 Thermal Measurement

The first group of the figures show the thermal images of APFC based on the $UCC28060$ controller which operates at $500W$ output voltage. The prototype is actively cooled by a fan which has $240m^3/h$ air flow. Second group of pictures shows the thermal images in case of natural passive cooling. The first figure is focused on the top view of the corrector. The NTC thermistor is the component with the highest temperature on the board. The figure b) shows the isometric view on the corrector. The detail of the bridge rectifier and power inductor is presented by the c) and d) sub figures.

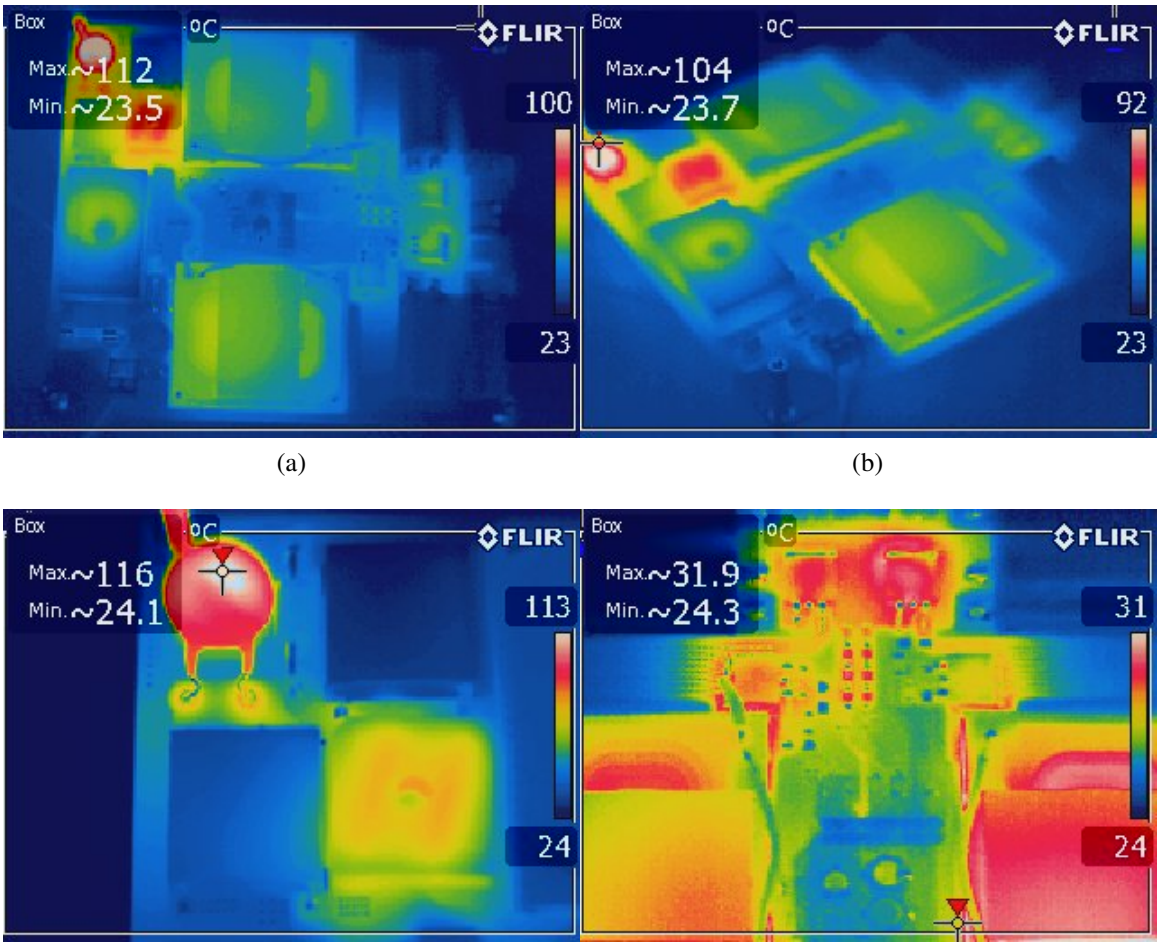


(a)



(b)

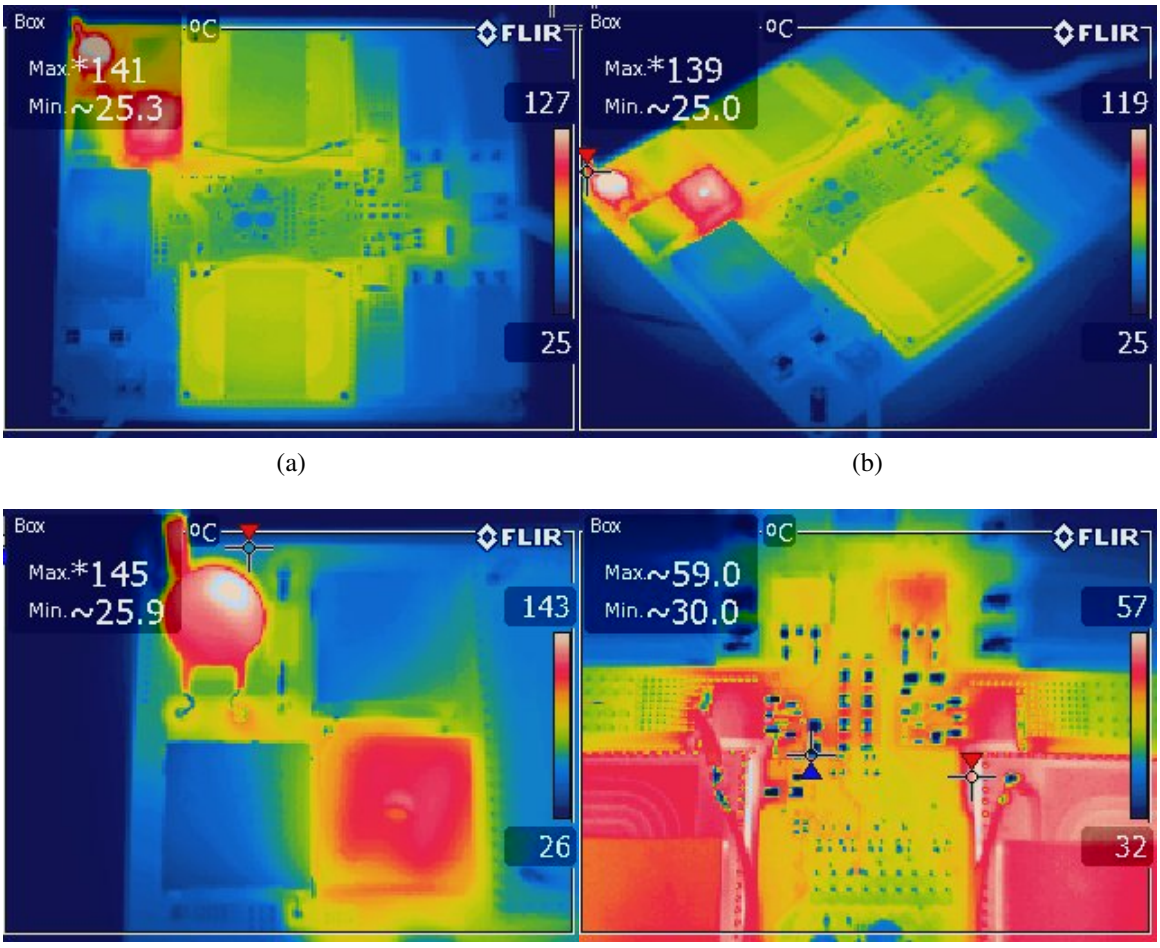
Fig. 8.19 Conductive EMI test results, a) graph of the emissions without the optimization and EMI filter, b) graph of the emissions with the optimization for EMI.



(a) (b)

(c) (d)

Fig. 8.20 Thermal image of the APFC based on UCC28060 which operates at 500 W output power with active cooling, a) top view, b) isometric view, c) thermal image of the rectifier bridge, d) thermal image of the MOSFET transistors and planar inductors.



(a) (b)

(c) (d)

Fig. 8.21 Thermal image of the APFC based on UCC28060 which operates at 500 W output power without active cooling, a) top view, b) isometric view, c) thermal image of the rectifier bridge, d) thermal image of the MOSFET transistors and planar inductors.

Chapter 9

Multi-phase Interleaved APFC

This chapter is devoted to a designing of the multi-phase interleaved corrector. The theoretical background of the interleaved correctors is described in previous chapter 5. The multi-phase converter is based on $UCC28070$ control circuit which is able to handle two-phase correctors. Moreover, the corrector includes a circuitry for synchronisation of the other correctors based on the $UCC28070$ control circuits due to it is possible to build the multi-phase correctors [52], [24].

The chapter consists of two main parts. The first part includes calculation related to the particular design and important features of the control circuit, the second part is engaged in design of the superior digital control system based on the $STM32F4$ discovery kit and hardware implementation.

9.1 Components Selection

First of all, it is necessary to select the main features of the corrector. The basic requirements are defined in the table 9.1.

Table 9.1 Requirements for a prototype based on the UCC28070 controller.

Design Parameter	Min	Typ	Max	Unit
Line Voltage $[V_{line}]$	85	-	265	V
Output Voltage $[V_{OUT}]$	-	390	-	V
Line Frequency $[f_{line}]$	47	-	63	Hz
Switching Frequency $[f_{sw}]$	-	200	-	kHz
Output Power $[P_{OUT}]$	-	1000	-	W
Efficiency at nominal power $[\eta]$	92	-	-	%

The output current is calculated by the following expression 9.1 [54].

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{1000}{390} = 2.564A \tag{9.1}$$

The maximal line current is caused by low line and high load conditions (the equation 9.2 [54])

$$I_{in,max} = \frac{P_{out}}{\eta \cdot V_{in,min}} = \frac{1000}{0.92 \cdot 85} = 12.788A \tag{9.2}$$

The previous calculation is an effective value of the maximal input current, the peak current is represented by the equation 9.3 [54].

$$I_{in,pk} = \sqrt{2} \cdot I_{in,max} = \sqrt{2} \cdot 12.788 = 18.085A \tag{9.3}$$

For estimation of the losses in the rectifier bridge, it is necessary to use average value of the peak input current 9.4 [54].

$$I_{in,max,avg} = \frac{2}{\pi}\sqrt{2} \cdot I_{in,max} = \frac{2}{\pi}\sqrt{2} \cdot 12.788 = 11.513A \tag{9.4}$$

The rectifier losses are computed by the following expression 9.5 [54].

$$P_{BR,max} = 2 \cdot V_F \cdot I_{in,max,avg} = 2 \cdot 0.95 \cdot 11.513 = 21.875W \tag{9.5}$$

The Boost converter maximal duty cycle is determined at the minimum line voltage condition (the equation 9.6 [54]).

$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{85}{390} = 0.782 \tag{9.6}$$

The inductor ripple is estimated by the next equation 9.7 [25]. The constant factor can be selected in range 0.1 to 0.4. It was chosen the 0.2 factor.

$$\Delta I_L = 0.2 \cdot I_{out,max} \cdot \frac{V_{out}}{V_{in}} = 0.2 \cdot 2.564 \cdot \frac{390}{85} = 2.353A \tag{9.7}$$

The inductance of the power inductor is estimated by the equation 9.8 [25]. Based on the calculation it was chosen the power inductor with $350\mu H$ inductance which should improve correction performance and decrease transistor current stress.

$$L \geq \frac{V_{out} \cdot D(1-D)}{f_{SW} \cdot \Delta I_L} = \frac{85 \cdot (390-85)}{2.353 \cdot 2e^5 \cdot 390} = 141.254\mu H \tag{9.8}$$

9.1.1 Output Bulk Capacitor Selection

The output bulk capacitor selection is based on the hold-up requirements which is defined by the following equation 9.9 [25].

$$C_{out} = \frac{\frac{2 \cdot P_{OUT}}{f_{line}}}{V_{OUT}^2 - (V_{OUT} \cdot 0.75)^2} = 639.477\mu F \approx 960\mu F \tag{9.9}$$

The choice of the output capacitor plays crucial role for the final frequency response of the power stage of the converter therefore it was chosen a combination of the $100nF$ ceramic multilayer capacitors with two bulky electrolytic capacitors. As a result, it was selected two $470\mu F$ capacitor and five $100nF$ ceramic capacitors. The final capacity of the output capacitor will be approximately $960\mu F$. In this case the final output voltage ripple is calculated by the equation 9.10 [25].

$$V_{ripple} = \frac{2 \cdot P_{OUT}}{\eta} \cdot \frac{1}{V_{OUT} \cdot 2\pi \cdot 2 \cdot f_{line} \cdot C_{OUT}} \tag{9.10}$$

Inserting the real numbers into the expression 9.10 [25], it will be assumed the final output voltage ripple.

$$V_{RIPPLE} = \frac{2 \cdot 1000}{0.92} \cdot \frac{1}{390 \cdot 2\pi \cdot 2 \cdot 47 \cdot 9.6e^{-4}} = 9.831V \tag{9.11}$$

The output capacitor selection is also based on the low frequency and high frequency currents which must be capable of handling them. The low frequency currents are related to a rectified input voltage and voltage ripple cancellation [25].

$$I_{C_{OUT}LF} = \frac{P_{OUT}}{\eta \cdot V_{OUT} \cdot \sqrt{2}} = \frac{1000}{0.92 \cdot 390 \cdot \sqrt{2}} = 1.971A \tag{9.12}$$

On the other hand, the high frequency currents are important in case of the noise reduction. The high frequency currents requirement is reflected by the following equation 9.13 [25].

$$I_{C_{OUT}HF} = \sqrt{\left(\frac{P_{OUT}}{\eta \cdot V_{OUT}} \cdot \sqrt{\frac{16 \cdot V_{OUT}}{6\pi \cdot V_{in_{min}}\sqrt{2}} - \eta^2}\right)^2 - I_{C_{OUT}LF}^2} \tag{9.13}$$

Inserting the parameters into the previous equation 9.13 [52], it is obtained the high frequency requirement for the output capacitor 9.14 [25].

$$I_{C_{OUT}HF} = \sqrt{\left(\frac{1000}{0.92 \cdot 390} \cdot \sqrt{\frac{16 \cdot 390}{6\pi \cdot 85 \cdot \sqrt{2}} - 0.92^2}\right)^2 - 1.971^2} = 3.306A \tag{9.14}$$

The data sheets of the capacitors usually include low and high frequency current ratings. If both of them are not specified in the data sheets, the currents have to be summed into one value by the squared value of the currents [25].

9.1.2 Power Transistor Selection

The selection of the power transistors has to fulfill the peak current and RMS requirements. The peak current rating of the transistor is defined by the next estimation 9.15 [25].

$$I_{peak} = \left(\frac{P_{OUT} \cdot \sqrt{2}}{2 \cdot V_{in_{min}} \cdot \eta} + \frac{\Delta I_L}{2}\right) \cdot 1.2 = \left(\frac{1000 \cdot \sqrt{2}}{2 \cdot 85 \cdot 0.92} + \frac{2.353}{2}\right) \cdot 1.2 = 12.263A \tag{9.15}$$

The RMS current rating of the power transistor is determined by the next two equation 9.16 and 9.17 [52] numerically respectively. The voltage rating of the power transistor is determined as a summing of the output voltage and voltage margin one half of the maximal acceptable voltage during the normal operation. Therefore, it was chosen the $SPP20N60S5$ [13] transistor with the $600V$ breakdown voltage rating [25].

$$I_{DS} = \frac{\frac{P_{OUT}}{\eta}}{2 \cdot V_{in_{min}} \cdot \sqrt{2}} \cdot \sqrt{2 - \frac{16 \cdot V_{in_{min}} \cdot \sqrt{2}}{3\pi \cdot V_{OUT}}} \tag{9.16}$$

$$I_{DS} = \frac{\frac{1000}{0.92}}{2 \cdot 85 \cdot \sqrt{2}} \cdot \sqrt{2 - \frac{16 \cdot 85 \cdot \sqrt{2}}{3\pi \cdot 390}} = 5.494A \tag{9.17}$$

The next equation 9.18 [52] defines an average current I_D through the boost diode. As well as in case of the transistors, the diodes have to withstand the voltage equals $600V$. The calculation leads to choose the $C3D10065$ [5] SiC boost diodes characterized by the extremely low junction capacity. Owing to this parameter the switching times of the diodes are significantly reduced. Finally, the overall efficiency is improved [25].

$$I_D = \frac{P_{OUT}}{2 \cdot V_{OUT}} = \frac{1000}{2 \cdot 390} = 1.282A \tag{9.18}$$

9.1.3 Current Sense Transformer Setup

The current sense transformer was selected based on the peak current through the power transistor. It was chosen the PULSE transformer $PE68210NL$ [37], which is capable of handling $15A$ current through the primary winding. This current sense transformer has the $1:1:50$ turns ratio therefore the maximal secondary loading current is obtained by the next equation 9.19 [25].

$$I_{SECmax} = \frac{15}{50} = 0.3A \tag{9.19}$$

The turns ratio of the current sense transformer is determined by the equation 9.20.

$$N_{CT} = \frac{N_{SEC}}{N_{PRI}} \geq \frac{I_{peak}}{I_{RS}} = \frac{12.263}{0.3} = 40.877 \tag{9.20}$$

As is clear from the estimation 9.20 [25], the current sense transformer with $1:50$ turns ratio is a suitable choice for the transistor current sensing. The next important parameter of the current sense transformer is a magnetizing inductance L_M which is determined by equation 9.21 [25] as a 2% part of the maximal secondary current of the current sense transformer. The selected current sense transformer reaches the $3.8mH$ magnetizing inductance [25].

$$L_M \geq \frac{V_S}{\frac{I_{peak}}{N_{CT_{real}}} \cdot 0.02 \cdot f_s \cdot V_{out}} \cdot \frac{V_{out} - V_{in_{min}} \cdot \sqrt{2}}{V_{out}} \tag{9.21}$$

Based on the equation 9.22 [25] it was selected the current transformer with $3.8mH$ secondary inductance.

$$L_M \geq \frac{3.7}{\frac{12.263}{50} \cdot 0.02 \cdot 2e^5 \cdot 390} \cdot \frac{390 - 85 \cdot \sqrt{2}}{390} = 2.609mH \tag{9.22}$$

The selection of the load resistor is based on the peak current limit voltage V_S which is $3.7V$ and peak current on the current transformer output (the equation 9.23 [25]). The factor 0.9 is used for the noise immunity improving at light load conditions.

$$R_T = \frac{0.9 \cdot V_S \cdot N_{CT_{real}}}{I_{peak}} = \frac{0.9 \cdot 3.7 \cdot 50}{12.263} = 13.577\Omega \approx 10\Omega \tag{9.23}$$

If it is assumed that the maximal allowable duty cycle is set to 0.97, the reset resistor is determined by the equation 9.24 [25].

$$R_R \geq R_T \cdot \frac{D_{max}}{1 - D_{max}} = 10 \cdot \frac{0.97}{1 - 0.97} = 323.33 \approx 330\Omega \tag{9.24}$$

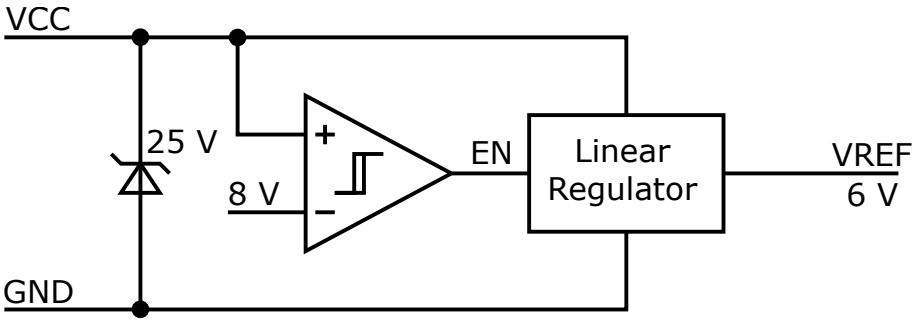


Fig. 9.1 Schematic diagram of the internal voltage reference.

The rectifying diodes have to withstand the current sense transformer reset voltage which is given by the expression 9.25 [25].

$$V_R = \frac{I_{peak} \cdot R_R}{N_{CT}} = \frac{12.263 \cdot 330}{50} = 80.936V \tag{9.25}$$

9.2 Setting Up Peak Current Limiting

The controller is equipped by a programmable cycle-by-cycle current limiting feature. The feature is capable of disabling one or both PWM outputs. When the signal from current sense input overcomes the voltage level which is configured by a resistor divider connected to the *PKLMT* pin, the PWM output of the controller is disabled until the next switching period starts. As a reference voltage it is used the internal source V_{ref} [52]. The reference voltage reaches $6V$. The block diagram of the voltage reference is showed in the figure 9.1. The full range of the *PKLMT* pin is between 0 to 4 V. Unfortunately, the linearity of the amplifiers is disrupted above $3.6V$. The voltage reference allows to provide the current range up to $2mA$. The recommended value of the load current is $0.5mA$. In cases of the high noise interferences, the *PKLMT* voltage can be filtered by a small capacitor. The high-side resistor R_{PK1} is determined to $3.6k\Omega$ [52].

$$R_{PK2} = \frac{V_S \cdot R_{PK1}}{V_{ref} - V_S} = \frac{3.7 \cdot 3.6e^3}{6 - 3.7} = 5.791k\Omega \approx 5.6k\Omega \tag{9.26}$$

The low-side resistor R_{PK2} is assumed by the equation 9.26 [25].

9.3 Converter Timing and Maximum Duty Cycle Clamp

The switching frequency of the corrector is set by the R_{RT} resistor. The frequency is inversely proportional to the R_{RT}. The switching frequency is determined to $200kHz$. The R_{RT} resistor can be computed by the equation 9.27 [25].

$$R_{RT} = \frac{7.5e^9}{f_s} = \frac{7.5e^9}{2e^5} = 37.5k\Omega \tag{9.27}$$

For the R_{RT} resistor it was chosen a standard value $36k\Omega$. The maximal duty cycle D_{MAX} equals to 0.97. The R_{DMX} resistor selection is based on the next equation 9.28 [25].

$$R_{DMX} = R_{RT_{real}} \cdot (2 \cdot D_{MAX} - 1) = 3.6e^4 \cdot (2 \cdot 0.97 - 1) = 33.84k\Omega \approx 33k\Omega \tag{9.28}$$

9.4 Output Voltage Set Point

The divider, which is created by the resistors R_A and R_B, is used for an output voltage programming. The internal reference V_{ref} uses the $6V$ voltage source. This voltage is compared to the output voltage fraction. The divider is set so that the output voltage level is 390 VDC. As a high resistor R_A is used $3M\Omega$ resistor [25].

$$R_B = \frac{\frac{V_{REF}}{2} \cdot R_A}{V_{OUT} - \frac{V_{REF}}{2}} = \frac{\frac{6}{2} \cdot 3e^6}{390 - \frac{6}{2}} = 23.26k\Omega \approx 24k\Omega \tag{9.29}$$

The resistor $24k\Omega$ was chosen based on the equation 9.29 [25]. As a result, the final output voltage is determined in the equation 9.30 [25].

$$V_{OUT} = \frac{V_{REF}}{2} \cdot \frac{R_A \cdot R_B}{R_B} = \frac{6}{2} \cdot \frac{3e^6 \cdot 2.4e^4}{2.4e^4} = 378V \tag{9.30}$$

Concurrently, the over voltage protection limit is set by the equation 9.31 [25].

$$V_{OVP} = 3.18 \cdot \frac{R_A + R_B}{R_B} = 3.18 \cdot \frac{3e^6 + 2.2e^4}{2.2e^4} = 436.816V \tag{9.31}$$

9.5 Current Synthesizer

The controller allows to emulate the down slope signal. Due to this feature it is suitable for the bridgeless topology. Generally, the bridgeless topology requires 3 sensing current transformers. Thanks to the emulation of the down-slope signal it is necessary to use only 2

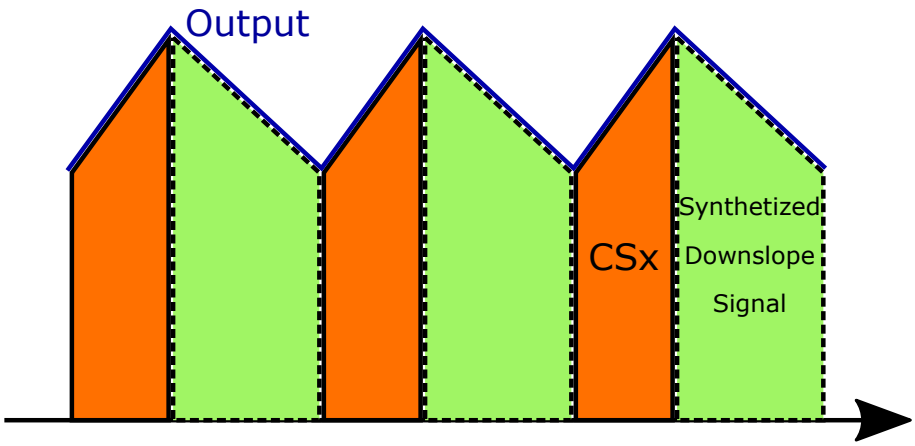


Fig. 9.2 Synthesized waveform.

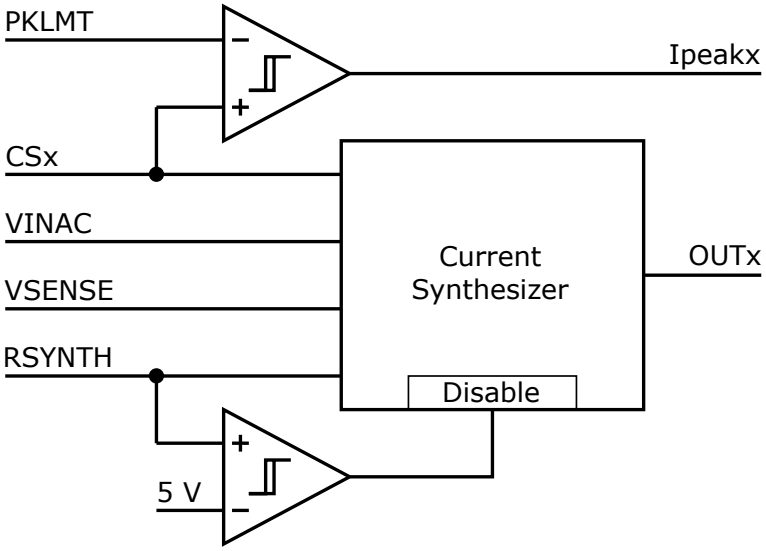


Fig. 9.3 Block diagram of the synthesizer circuit.

current transformers. During the on-times of the transistors the inductor current is sensed by the current transformers. Simultaneously, the input voltage and the output voltage are monitored by the controller. The signals provide complete information for the internal emulation of the inductor down-slope current signal of each output cells [52].

Due to the using slightly different inductors the synthesizer has to adjust the parameters itself. The response characteristics is parametrized by the resistor R_{syn} which can by determined by the equation 9.32 [52]. During the inrush starting sequence at the power up and AC drop-out the synthesizer generates the down-slope equals to zero. As a consequence, the emulated inductor current is kept above the IMO reference. As a result, the duty cycle remains zero. This feature has a positive impact on the stress reduction of the transistor during

the surge condition. The technique monitors input and output voltages. When the input voltage drops below the output voltage, the duty cycle grows until the nominal steady-state condition is reached [52].

$$R_{syn} = \frac{N_{CT_{real}} \cdot L_{max} \cdot \frac{R_B}{R_A+R_B}}{R_S \cdot C_S} \tag{9.32}$$

The synthesizer setting resistor can be calculated by the equation 9.32 [25] where L_B is nominal zero-bias boost inductance, R_T is the resistivity of the current sense resistor, N_{CT} is current sense transformer turns ratio, and $k_R = R_B/R_A + R_B$ is attenuation factor of input and output voltages.

$$R_{syn} = \frac{50 \cdot 5e^{-4} \cdot \frac{2.4e^4}{3e^6+2.4e^4}}{10 \cdot 1e^{-10}} = 198.412k\Omega \approx 200k\Omega \tag{9.33}$$

9.6 Linear Multiplier and Quantized Voltage Feed Forward

The voltage V_{VAO} gives information about the total output power of the APFC. The main advantage of the controller is a internal quantized feed-forward circuitry. There are seven thresholds of the linear multiplier which create eight quantization levels. These eight levels cover the universal line voltage range from 85 to 265 V_{RMS}. The fixed setting of the linear multiplier is described in the table 9.2 [52]. The fixed k_{VFF} factors reduce a distortion of the

Table 9.2 Quantized steps of the feed forward circuitry.

LEVEL	peak voltage	kVFF factor	Vin peak voltage
1	$V_{VINAC(pk)} \leq 1V$	0.398	133 V
2	$1V \leq V_{VINAC(pk)} \leq 1.2V$	0.6	133 - 160 V
3	$1.2V \leq V_{VINAC(pk)} \leq 1.4V$	0.839	160 - 187 V
4	$1.4V \leq V_{VINAC(pk)} \leq 1.65V$	1.156	187 - 220 V
5	$1.65V \leq V_{VINAC(pk)} \leq 1.95V$	1.604	220 - 260 V
6	$1.95V \leq V_{VINAC(pk)} \leq 2.25V$	2.199	260 - 300 V
7	$2.25V \leq V_{VINAC(pk)} \leq 2.6V$	2.922	300 - 345 V
8	$2.6V \leq V_{VINAC(pk)}$	3.857	> 345V

multiplier output which can be produced by the filtered $VINAC$ signal. The filtered signal includes frequently the second harmonics which distort the $VINAC$ signal. The quantization technique enables a fast response on the line voltage changes so that the output voltage disturbances will be eliminated. Due to the chattering problem between quantization levels

the architecture is equipped by the five-percentage hysteresis. The hysteresis allows to avoid ringing and distortion problems [52].

For the appropriate working of the controller the zero crossing detection has to be activated. The zero crossing is defined as the voltage falling of the V_{VINAC} below $0.7V$. The falling takes typically $50\mu s$ at least. The reference current signal I_{IMO} can be calculated by the next equation 9.34 [52].

$$I_{IMO(max)} = 17e^{-6} \cdot V_{VINAC} \cdot \frac{V_{VAOMAX} - 1}{k_{vff}} = 17e^{-6} \cdot 0.76 \cdot \frac{5-1}{0.398} = 130\mu A \tag{9.34}$$

Where V_{vaomax}equals to $5V$, $Vvinac$ is 0.76 and K_{vff} parameter is defined to 0.398. The parameter k_{VFF} corresponds to the RMS value of the line voltage at the center of the quantization level. The voltage signal V_{VAO} provides a compensation of higher or lower values within one quantization step. The compensation is carried out by the voltage feedback loop which is capable of working within the quantization level as well as during the transition between two steps. The hysteresis avoids a chattering problem during the transition [52].

$$R_{IMO} \cdot I_{IMO(max)} = \frac{1}{2} \cdot \frac{I_{IN(pk)} \cdot R_S}{N_{CT}} \tag{9.35}$$

The architecture defines the maximum input power limits within the quantisation steps. The minimal power limit of the first step is defined at the V_{VINAC} voltage equals to $0.76V$. The highest limit within the first step is at the transition between first and second quantization steps. These rules are applied within all steps. If the signal V_{VINAC} is below the $0.76V$ threshold, the input power limits drop linearly to zero with declining line voltage [52].

$$V_1 = 0.76 \cdot \frac{R_A + R_B}{R_B \cdot \sqrt{2}} = 0.76 \cdot \frac{3e^6 + 2.2e^4}{2.2e^4 \cdot \sqrt{2}} = 73.819V \tag{9.36}$$

The design process starts with a selection of the maximum steady state output power. The value is multiplied by the factors 1.1 or 1.2 which represent the recharging of the bulk capacitor at full load conditions. The equation 9.37 [25] defines the output voltage of the current sense transformer at low line and full load [52].

$$V_2 = \frac{1.1 \cdot P_{OUT} \cdot \sqrt{2} \cdot R_S}{2\eta \cdot V_1 \cdot N_{CT}} = \frac{1.1 \cdot 1000\sqrt{2} \cdot 10}{2\eta \cdot 73.819 \cdot 50} = 2.291V \tag{9.37}$$

For the calculation is selected as follows: the V_{VINAC} voltage is $0.76V$, V_{line} equals to $73V$, the k_{VFF} quantization factor is defined to 0.398. $I_{IN(pk)}$ represents the peak input current at low line and maximum determined load. The inductor current is sensed by the current sense

transformer. The output of the current sense transformer is loaded by the R_S resistor. The turns ratio of the current transformer and the resistor value determine an output signal range of the current sense transformer network. The limit voltage of the *CSA* and *CSB* inputs is $3V$ [52].

$$R_{IMO} = \frac{V_2}{I_{IMO}} = \frac{2.291}{130e{-}6} = 17.623k\Omega \approx 18k\Omega \tag{9.38}$$

The current limitation is set by the cycle-by-cycle peak current limiting feature. The same equation can be used for each quantization level. The current limit is set at low line and maximum output power. The current limitation at high line is below the border which is defined at low line. As a consequence, the input current at high line and nominal output power is below the power rating of the components. The multiplier of the controller was considerably improved in comparison to previous generation of the controllers. The accuracy of the controller is affected by V_{VAO} if the voltage is close to 1 due to the expression $(V_{VAO} - 1)$ [52], [25].

9.7 Enhanced Transient Response

The rectification of the line voltage causes fluctuations of the output voltage. The corrector has to be resistant to the slight ripple which has the twice line frequency. Due to this fact the corrector is equipped by a low bandwidth voltage feedback. This feature solves the problem with the ripple. Unfortunately, the input voltage and load transients are not the low frequency phenomena. As a consequence, the voltage feedback is not able to compensate these transients. The linear quantizer is able to handle the issue of the transients. The transient phenomena are regulated by the voltage feedback with the linear quantizer circuitry.

The response of the controller is affected by an auxiliary $100\mu A$ current source which is connected to the voltage amplifier output. The auxiliary current source is activated if the voltage drop on the V_{VSENSE} pin reaches to 93% of the regulation level, which is $2.79V$. During the soft-start sequence the auxiliary current source is disabled. The soft-start circuitry is responsible for the regulation of the output voltage in the cases that the V_{VSENSE} voltage is below the $0.75V$ border [52].

9.8 Current Loop Compensation

The controller includes two identical current feedback transconductance amplifiers. Thanks to these transconductance amplifiers the input line current can be shaped. Each transconductance

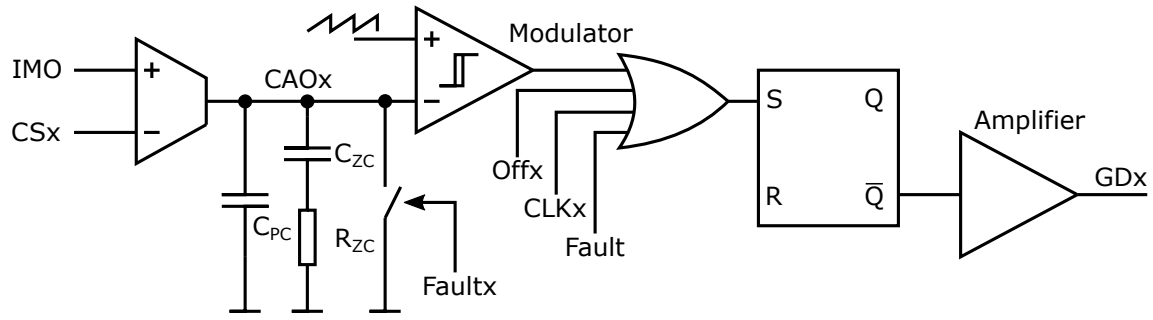


Fig. 9.4 Circuit diagram of the current loop compensation.

amplifier has two input signals. The first one called *IMO* ensures the reference signal which is a product of the multiplier. The signal contains information about average line voltage, instantaneous line voltage and error output voltage signal.

The second signal gives information about an instantaneous transistor current which flows during on state of the transistors. The signal is zero in case of open transistors. Therefore the signal is not sufficient for regulation. The down-slope curve is synthesized and compared to the required current signal from the multiplier stage. The output signal of the transconductance amplifier controls the PWM modulation stage which produces the PWM signals for the power transistors [52], [25].

For a modelling of the boost stage shall be used a small-signal model of the boost stage with current sensing circuitry in case of the frequencies between LC resonance of the power stage and switching frequency. The expression of the model is described in the next equation.

$$\frac{V_{RS}}{V_{CA}} = \frac{V_{OUT} \cdot R_S \frac{1}{N_{CT}}}{\Delta V_{RAMP} \cdot k_{SYNC} \cdot s \cdot L_B} \tag{9.39}$$

Where L_B is an average value of the boost inductance, R_S resistor is a load resistor for the current sense transformer, N_{CT} parameter gives information about the turns ratio of the current sense transformer, V_{OUT} is an output voltage of the corrector,ΔV_{RMP} is the amplitude of the ramp signal, k_{SYNC}, s is Laplace complex variable.

The compensation network of the current error amplifier should provide a high gain at low frequencies of the current ripple and flat gain over the transfer function zero. Due to these features the compensation network offers an attenuation of the switching ripple of the current signal.

The crossover frequency of the current loop is determined to $1/10^{th}$ of the switching frequency.

$$f_{CXO} = \frac{f_{SW}}{10} \tag{9.40}$$

The power stage gain G_{PSC} is calculated at the crossover frequency which is selected as $1/10th$ of the switching frequency.

$$G_{psc} = \frac{V_{OUT} \cdot R_S \frac{1}{N_{CT}}}{2\pi \cdot f_{CXO} \cdot L_{AVG} \cdot V_{RAMP}} = \frac{390 \cdot 10 \cdot 0.02}{2\pi \cdot \frac{2e^5}{10} \cdot 3e^{-4} \cdot 4} = 0.517 \tag{9.41}$$

Let's assume that the open loop gain equals to 1. G_{psc} was calculated at previous equation 9.41. The g_{mc} parameter defines the transconductance of the error amplifier which reaches to $100\mu S$. R_{ZC} is a compensation resistor for the defined crossover frequency.

$$1 = G_{PSC} \cdot g_{mc} \cdot R_{ZC} \tag{9.42}$$

Modification of the equation 9.42 [25] for the open loop gain the R_{ZC} resistor value can be computed.

$$R_{ZC} = \frac{1}{gm_c \cdot G_{PSC}} = \frac{1}{100e^{-6} \cdot 0.517} = 19.342k\Omega \approx 18k\Omega \tag{9.43}$$

Let's assume that f_{CXO} equals to the f_{ZC} frequency. Based on this relation can be found the C_{ZC} capacitance.

$$f_{ZC} = f_{CXO} = \frac{1}{2\pi \cdot C_{ZC} \cdot R_{ZC}} \tag{9.44}$$

C_{ZC} is determined by the previous dependencies.

$$C_{ZC} = \frac{1}{2\pi \cdot \frac{f_{SW}}{10} \cdot R_{ZC}} = \frac{1}{2\pi \cdot \frac{2e^5}{10} \cdot 1.8e^4} = 442.097pF \approx 470pF \tag{9.45}$$

As a result, the phase margin of 45 deg is achieved at the crossover frequency. For the enhanced phase margin is necessary to choose the f_{ZC} frequency below the f_{CXO} crossover frequency.

A small parallel capacitor C_{PC} causes an additional pole at a high frequency. The main reason of this pole is ripple and noise attenuation. The pole is added at the half switching frequency of the corrector 9.46 [25].

$$C_{PC} = \frac{1}{2\pi \cdot \frac{f_{SW}}{2} \cdot R_{ZC}} = \frac{1}{2\pi \cdot \frac{2e^5}{2} \cdot 1.8e^4} = 88.419pF \approx 100pF \tag{9.46}$$

The final verification of the calculation can be provided by the graphical interpretation of the current loop gain $T_{cdB}(dB)$ and loop phase $\phi c(f)$.

$$T_{cdB}(f) = 20log \cdot (|G_{PSC} \cdot gm_c \cdot G_{COMP}|) \tag{9.47}$$

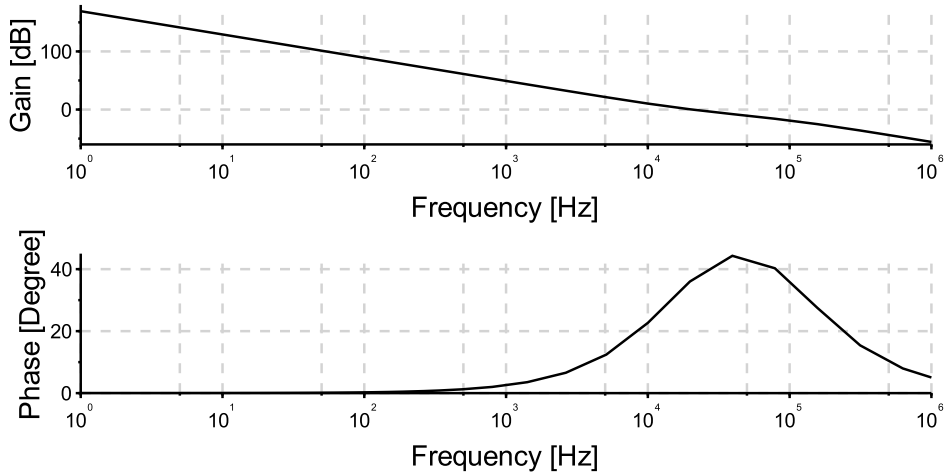


Fig. 9.5 Bode plots of the current loop.

Inserting the transfer functions into the equation 9.47 [25] it can be derived the total closed loop transfer function 9.48.

$$T_{cdB}(f) = 20log\left(\left|\frac{V_{out}\cdot R_S\frac{1}{N_{CTreal}}}{2\pi\cdot f_{CXO}\cdot L_{avg}\cdot V_{ramp}}\cdot\frac{gm_c\cdot(s\cdot R_{ZC}\cdot C_{ZC}+1)}{s^2\cdot(R_{ZC}\cdot C_{ZC}\cdot C_{PC})+s\cdot(C_{ZC}+C_{PC})}\right|\right) \tag{9.48}$$

The graphs 9.5 shows that the crossover frequency of the corrector is placed at approximately $20kHz$ and the phase margin reaches 35 degrees.

9.9 Voltage Loop Configuration

The controller includes one output voltage regulation loop as single phase controllers. The compensation is performed by the traditional compensation techniques. The bandwidth of the voltage feedback has to be below the frequency of the rectified line voltage. In other words it shall be below 100 or $120Hz$ respectively. The setting below this border prevents the output voltage to distortion.

The output of the error voltage amplifier ensures the regulation of the reference signal so that the signal contains information about the load condition. Due to the output voltage ripple is proportional only to the input power, the peak-to-peak ripple is same at different line voltage conditions.

The voltage feedback is based on the transconductance amplifier as well as in case of the current one. An advantage of the transconductance amplifiers are no dependencies the input impedance on the amplifier gain. The gain is affected by the transconductance (g_{mv}) and the

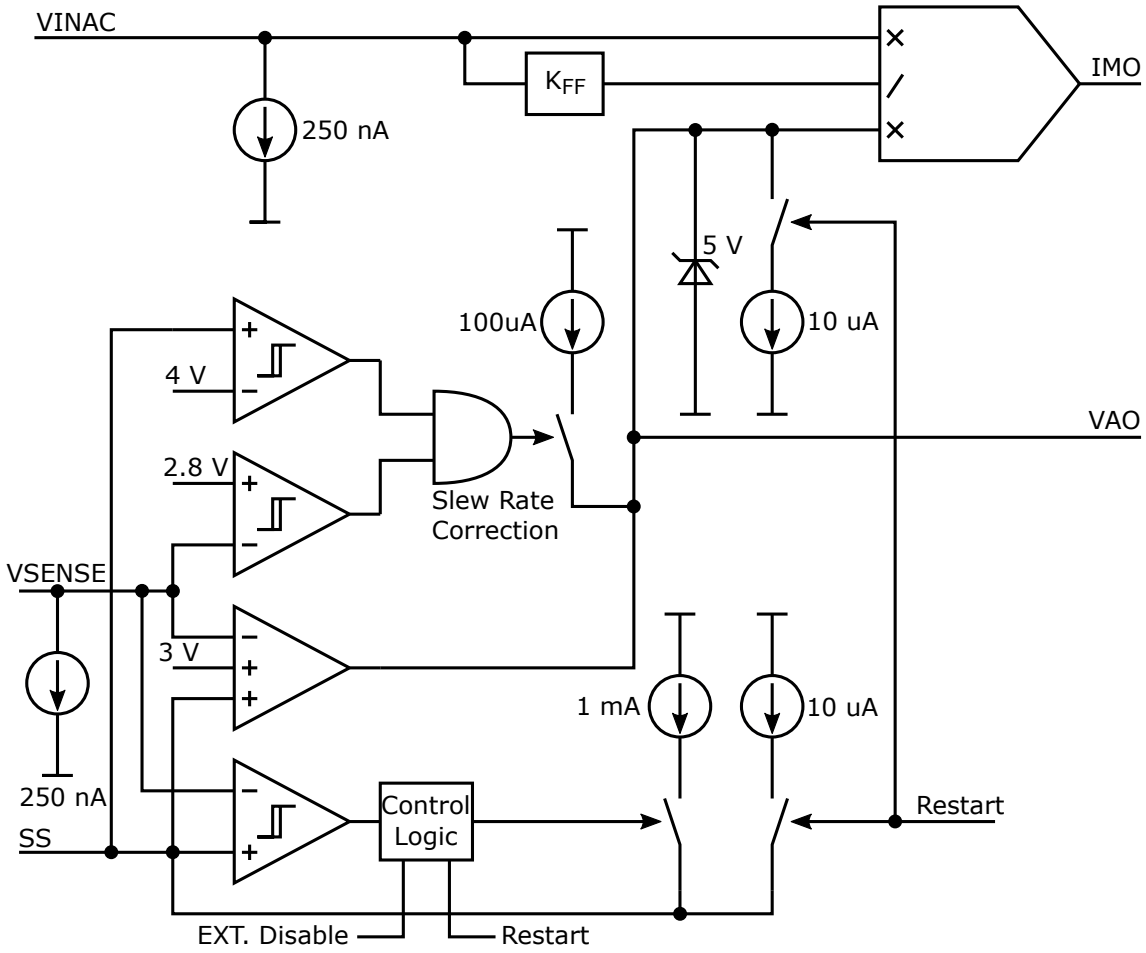


Fig. 9.6 Circuit diagram of the voltage loop.

output impedance (Z_O). As a result, the input setting and compensation can be determined individually.

The twice line voltage ripple of V_{SENSE} voltage should be reduced by an attenuation and a phase shifting of the voltage at the *VAO* pin. It reduces a level of the 3^{rd} distortion. The compensation of the harmonic distortion is performed by an increasing of the gain at twice line frequency [52], [25]. It is valid the next equation 9.49 [25].

$$G_{VEA} = \frac{V_{VAOpk}}{V_{SENSEpk}} = g_{mv} \cdot Z_O \tag{9.49}$$

The 1% of the 3^{rd}-harmonic distortion at the V_SENSE pin is provided by 2% voltage ripple in full range of the *VAO* voltage. The V_{VAO} voltage represents a load power. The range begins at $1V$ in case of zero load power to $4.2V$ at full load conditions. Therefore (ΔVAO) equals to $3.2V$ and 2% of (ΔVAO) is the $64mV$ peak ripple.

The voltage loop uses a transconductance error amplifier which is characterized by the $gm_v = 7e^{-5}\mu S$ transconductance. The voltage divider gain is defined by the equation 9.50 [25].

$$H = \frac{V_{ref}}{V_{out}} = \frac{3}{378} = 7.937e^{-3} \tag{9.50}$$

The output voltage ripple is determined as a 3% of (ΔVAO). The Z_O impedance is defined at twice line frequency (9.51 [25]).

$$Z_{O(f_{2LF})} = \frac{\Delta VAO \cdot 0.03}{V_{RIPPLE} \cdot H \cdot gm_v} = \frac{3.2 \cdot 0.03}{9.831 \cdot 7.937e^{-3} \cdot 7e^{-5}} = 17.575k\Omega \tag{9.51}$$

The C_{PV} capacitor is found according to the equation 9.52 [25], which reflects the output impedance $Z_{O(f_{2LF})}$.

$$C_{PV} = \frac{1}{2\pi \cdot 2 \cdot f_{line} \cdot Z_{O(f_{2LF})}} = \frac{1}{2\pi \cdot 2 \cdot 47 \cdot 1.7575e^4} = 96.338nF \approx 100nF \tag{9.52}$$

The crossover frequency is determined based on the following relation 9.55 [25] so that the power factor correction performance was maximized. The crossover frequency is searched by equation, which defines the open loop gain of the corrector, by assuming that open loop gain equals to 1.

$$Tv(f_{VXO}) = G_{PSV} \cdot G_{CV} \cdot H = 1 \tag{9.53}$$

$$Tv(f_{VXO}) = \left(\frac{\frac{P_{OUT}}{\eta}}{\Delta V_{VAO}} \cdot \frac{\frac{1}{j2\pi \cdot f_{VXO}\, C_{OUT}}}{V_{OUT}} \right) \cdot \frac{g_{mv}}{j \cdot 2\pi \cdot C_{PV}} \cdot H = 1 \tag{9.54}$$

The crossover frequency can derived from the next equation 9.55 [25].

$$f_{CV} = \sqrt{H \cdot gm_v \cdot \frac{\frac{P_{OUT}}{\eta}}{\Delta VAO} \cdot \frac{\frac{1}{2\pi \cdot C_{OUT}}}{V_{OUT}} \cdot \frac{1}{2\pi \cdot C_{PV}}} \tag{9.55}$$

Inserting the numbers into equation 9.55 [25] it can be found out the particular crossover frequency.

$$f_{CV} = \sqrt{7.937e^{-3} \cdot gm_v \cdot \frac{\frac{P_{out}}{\eta}}{\Delta VAO} \cdot \frac{\frac{1}{2\pi \cdot C_{OUT}}}{V_{OUT}} \cdot \frac{1}{2\pi \cdot C_{PV}}} = 11.477Hz \tag{9.56}$$

The R_{ZV} resistor with C_{PV} creates a pole of the loop gain at higher frequency then the crossover. Thereby it provides 45 °phase margin at the crossover frequency. A calculation of the R_{ZV} resistor is based on the equation 9.57 [25].

$$R_{ZV} = \frac{1}{2\pi \cdot f_{CV} \cdot C_{PV}} = \frac{1}{2\pi \cdot 11.477 \cdot 1e^{-7}} = 138.672k\Omega \approx 130k\Omega \tag{9.57}$$

Finally, a voltage compensation capacitor C_{ZV} is determined by the equation 9.58 [25]. The capacitor creates a zero which provides gain increment at the DC gain of the voltage loop. It enhances the phase margin. The additional zero should be selected to $1/10^{th}$ of the crossover frequency. The capacitor value can be also estimated approximately $\approx 10 \cdot C_{PV}$ [25].

$$C_{ZV} = \frac{1}{2\pi \cdot \frac{f_{CV}}{10} \cdot R_{ZV}} = \frac{1}{2\pi \cdot \frac{11.477}{10} \cdot 1.3e^{5}} = 1.067\mu F \approx 1\mu F \tag{9.58}$$

The equation 9.59 [25] consists of voltage divider feedback gain H, transconductance of the error amplifier g_{mv}, and compensation network gain.

$$G_{CV}(f) = \frac{\Delta V_{VAO}}{\delta V_{OUT}} = H \cdot g_{mv} \cdot \frac{s \cdot R_{ZV} \cdot C_{ZV} + 1}{s^2 \cdot (R_{ZV} \cdot C_{ZV} \cdot C_{PV}) + s \cdot (C_{ZV} + C_{PV})} \tag{9.59}$$

The G_{PSV} power stage gain is determined by the following equation 9.60 [25].

$$G_{PSV}(f) = \frac{\Delta V_{OUT}}{\delta V_{VAO}} = \frac{\frac{P_{OUT}}{\eta}}{\Delta VAO} \cdot \frac{\frac{1}{s \cdot C_{OUT}}}{V_{OUT}} \tag{9.60}$$

The verification of the previous calculations can be provided by the plotting of the closed voltage loop gain $T_{vdB}(dB)$ and loop phase $\phi c(f)$.

$$T_{vdB}(f) = 20log(|G_{PSV} \cdot G_{CV}|) \tag{9.61}$$

From Bode plots it can be found that the crossover frequency of the corrector and phase margin. The crossover frequency is placed at approximately $8Hz$ and the phase margin reaches 50 degrees. The final prototype requires as a rule an adjusting the compensation network therefore the selected components in the schematic diagram at appendix may not match the theoretical calculations.

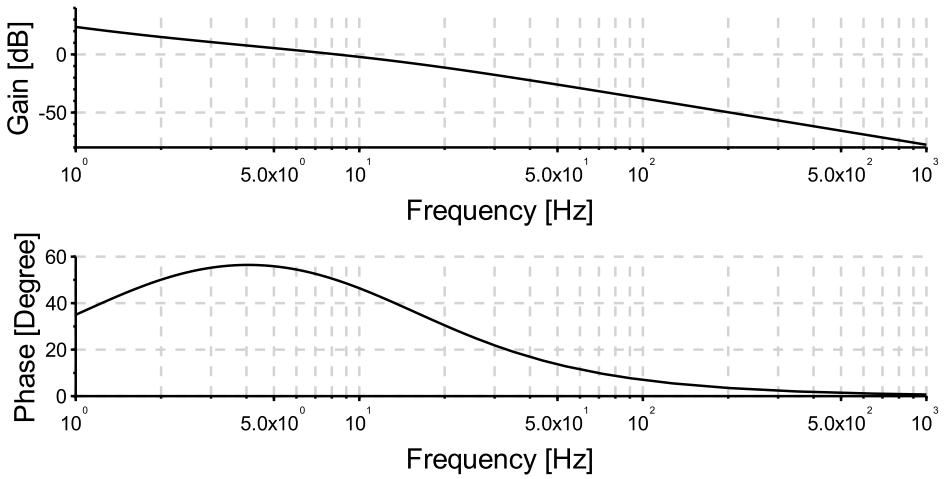


Fig. 9.7 Bode plots of the voltage loop.

9.10 Adaptive Soft Start Circuitry

When the corrector is connected to the line, the bulk capacitor voltage equals to zero level. If the voltage regulation was regulated by the voltage feedback, the inrush current and component stress would be enormous. Therefore the soft start circuit ensures the slight ramp up during the power up. The start sequence begins when the V_{VSENSE} voltage reaches the $0.75V$ border.

The internal pull-down of the *SS* pin immediately disabled. Conversely, the $1.5mA$ pull-up is activated. It ensures the change of the ramping method from the initial one quarter dead time to the traditional zero to V_{REF} regulation of the ramp. In this case the voltage on the *SS* pin reaches to the V_{VSENSE} voltage and the capacitor C_{SS} is charged by the $10\mu A$ current source. As a result, the soft-start duration is found according to the C_{SS} capacitor selection [52].

$$t_{SSmin} = C_{ZV} \cdot \frac{3 - V_{VSENSE}}{10e^{-6}} = 1e^{-6} \cdot \frac{3 - 0.75}{10e^{-6}} = 225ms \tag{9.62}$$

The selection shall respect the rule $C_{SS} \geq C_{ZV}$ so that the soft-start duration is longer than the minimal acceptable value which is defined in equation 9.62 [25]. The initial pre-charging of the C_{SS} capacitor ensures a reduction of the charging delay. The pre-charging uses the $1.5mA$ current source which is able to charge the capacitor in short time to the V_{VSENSE} voltage level.

After pre-charging, the capacitor is charged by the $10\mu A$ current source which controls the voltage increase as it is desired by the capacitor value. The soft-start duration equals

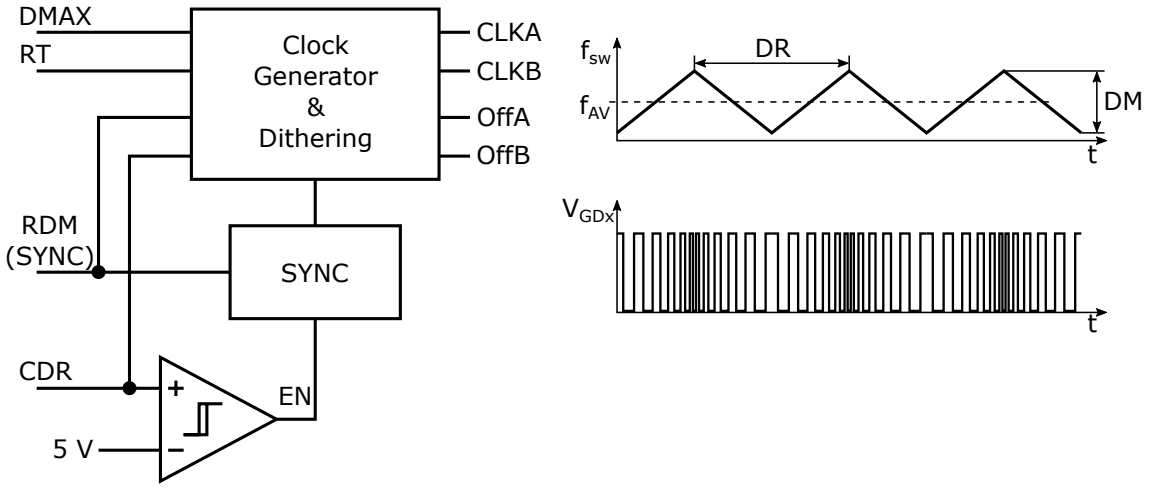


Fig. 9.8 Frequency dithering principle.

approximately to the expression 9.62. The soft-start duration t_{SS} is determined to $500ms$ owing to a reduction of the current stress of the power components. Finally, the soft-start setting capacitor can be derived by the equation 9.63 [25].

$$C_{SS} = \frac{10e^{-6} \cdot t_{SS}}{2.25} = \frac{10e^{-6} \cdot 500e^{-3}}{2.25} = 2.222\mu F \approx 2.2\mu F \tag{9.63}$$

9.11 Frequency Dithering

The accomplishment of the EMI requirement becomes difficult. Sometimes, the EMI filter does not provide a sufficient filtering of EMI. In this case, one possibility is a redesign of PCB. The redesign takes a considerable amount of time and effort. The second option is a reduction of the electromagnetic emissions by a modifying of the switching frequency. The switching frequency of the corrector is modulated by a inner triangular signal.

Thanks to the modulation the conducted EMI noise is significantly reduced. The noise is spread within a wider frequency band. This strategy is used in two cases. When the corrector is developed and the EMI filter is not able to adequately eliminate the conducted noise. The second case is design to cost where EMI filter is designed as cheap as possible [52].

The frequency dithering is defined by two parameters, which are a dither magnitude and a dither rate. The dither magnitude defines a range of the switching frequency changes around a center frequency setting. The center frequency is set by the R_{RT} resistor and it is nominal switching frequency. The typical dither magnitude f_{DM} is determined as one fifth of the nominal frequency.

For example the design uses the $200kHz$ nominal switching therefore the dither magnitude should be $40kHz$. As a result, the switching frequency swings from 180 to $220kHz$. The variable frequency is not a problem for the setting duty cycle clamp by the R_{DMX} resistor. The setting of the clamp remains the same. The dither magnitude is determined by the R_{RDM} resistor. The resistivity is computed by the following expression 9.64 [25].

$$R_{RDM} = \frac{937.5e^6}{f_{DM}} = \frac{937.5e^6}{4e^5} = 23.438k\Omega \approx 27k\Omega \tag{9.64}$$

The second parameter is the dither rate f_{DR} which defines the frequency of the changes from one extreme to other one. In other words the dither rate defines the speed of the frequency variation. For example the dither rate equals to $1kHz$, it means that the switching frequency is modulated between 180 and $220kHz$ once every $1ms$. If the R_{RDM} resistor is defined, the C_{CDR} capacitor connected to *CDR* pin and ground is calculated by the equation 9.65 [25].

$$C_{CDR} = \frac{0.0667e^{-9} \cdot R_{RDM}}{f_{DR}} = \frac{0.0667e^{-9} \cdot 2.7e^4}{1e^3} = 1.8nF \tag{9.65}$$

The setting of the parameters plays a crucial role for EMI reduction and loop stability. The good initial values are 20% of the switching frequency for dither magnitude and $1kHz$ for the dither rate (f_{DR}).

When it is necessary to disable the dithering function, the controller is equipped by the voltage source $VREF$. If the *CDR* pin is connected to the $VREF$ voltage and the *RDM* pin is connected directly to ground, the dithering function is disabled. The typical reason is an external synchronization [52].

9.12 External Synchronization

The external synchronization function provides the multiphase operation of the correctors. If the external synchronization is used, the internal dithering circuitry is disabled due to an unpredictable behaviour during the synchronization.

If the dithering circuitry is disabled, the synchronization circuitry is activated automatically. The internal clock generation is synchronized by the pulses presented on the *RDM* pin. The synchronization pulses have to provide a double switching frequency of the corrector. If the required switching frequency is determined to $200kHz$, the synchronization signal reaches to the $400kHz$ value (the equation 9.66) [52].

$$f_{PWM} = \frac{f_{SYNC}}{2} = \frac{4e^5}{2} = 200kHz \tag{9.66}$$

The generator of the internal pulses shall not interfere with the synchronization signal therefore the internal frequency setting shall be at least 10% below the frequency of the synchronization signal. The R_RT resistor is calculated by the following expression 9.67 [52].

$$R_{RT} = \frac{15000}{f_{SYNC}} \cdot 1.1 = \frac{15000}{4e^5} \cdot 1.1 = 41.25kHz \tag{9.67}$$

Due to the PWM modulator gain is inversely proportional to the R_{RT} timing resistor, the current loop feedback transfer function shall be corrected. The duty cycle clamp is also affected owing to the timing subsystem of the controller which is charged of the right setting of the maximum duty cycle. The process of the maximum duty cycle setting begins at the falling edge of the synchronization pulses. In other words, the R_{DMX} resistor is responsible for the duty cycle clamp which is dependent on the width of the synchronization pulses. The duty cycle of the synchronization signal can be calculated by the following equation 9.68 [52].

$$D_{SYNC} = t_{SYNC} \cdot f_{SYNC} \tag{9.68}$$

As a consequence, the setting resistor value is obtained by the equation 9.69.

$$R_{DMX} = \left(\frac{15000}{f_{SYNC}}\right)(2 \cdot D_{MAX} - 1 - D_{SYNC}) \tag{9.69}$$

As is clear from the equation 9.68, the effect of the pulse width shall be eliminated using by an the pulse as short as possible. The propagation delay between falling edge of the external synchronization signal and internal timing circuitry is from 50 to 100ns. Due to this off-times propagation delay at highest switching frequencies are reduced. At the highest switching frequencies shall be the equation 9.69 modified by the fraction $(t_{SYNC} - 0.1/t_{SYNC})$. The compensation fraction is appropriate to use at the high frequencies. At low frequencies the fraction is insignificant in comparison to PWM period.

The external synchronization shall be used in two cases. The first one, it is synchronization with a downstream converter due to the current interferences. The second one is a synchronization between multi-phase correctors. The controller is able to drive two-phase interleaved correctors. The high-power correctors take advantage of the multiphase operation.

The suitable timing of the synchronization signals optimise the current ripple cancellation. The phase shift between synchronization signals depends on the number of the controllers. For the four-phase interleaved corrector it is necessary to use two controllers. The phase shift

between the signals shall be 180° for the optimal current cancellation. Three synchronization signals with the phase shift 120° to each other should be used for the six-phase interleaved corrector in case of the optimal current cancellation [52].

9.13 Protections of the Corrector

The controller contains several protections which handle inrush condition, over voltage protection, zero power detection feature and thermal shut down. If the *VAO* voltage is below the $0.75V$ level, the soft-start initial period is activated. This circuitry allows to achieve a continuous increase of the duty cycle from zero to the normal value. This feature reduces the inrush current to a minimal value.

The over voltage protection plays a crucial role for the design APFCs with the high output voltage. The $VSENSE$ voltage is used for the output voltage regulation as well as for the over voltage protection. When the voltage exceeds $3.18V$ level, which corresponds to 106% of the nominal value, the *GDA* and *GDB* outputs are disabled. As a result, the output voltage drops down and the current transconductance outputs are pulled low. Thanks to this feature the duty cycle starts with initial value 0% when the over voltage protection condition is not valid. The normal operation is activated if the $VSENSE$ voltage overcomes $3.08V$ [52].

The zero power detection feature protects the corrector to undesired behaviour at non-load or light load conditions. The comparator is able to switch off both *GDA* and *GDB* outputs when the voltage on the *VAO* pin drops below the $0.75V$ border. The *GDx* outputs are enabled when the V_{VAO} voltage overcomes the $0.9V$ level.

The controller shall be supplied by a voltage source in the range from 10 to $21V$. The under voltage lockout feature activates the controller when the supply voltage exceeds the $10.2V$ level. The controller includes also the clamping diode which prevents the circuit to the over voltage conditions at the supply voltage [52].

The controller contains an over temperature comparator which continuously monitors a die temperature. If the die temperature grows above $160°C$, the controller disables almost of the inner circuitry and the *GD* outputs. A hysteresis of the temperature comparator is $20°C$. If the temperature drops below the $140°C$ border, the controller performs a standard soft-start procedure [52].

9.14 Enabling and Disabling

The controller includes two respectively four independent paths for a control of enabling and disabling of the corrector branches. The first two are described in the technical manual. The

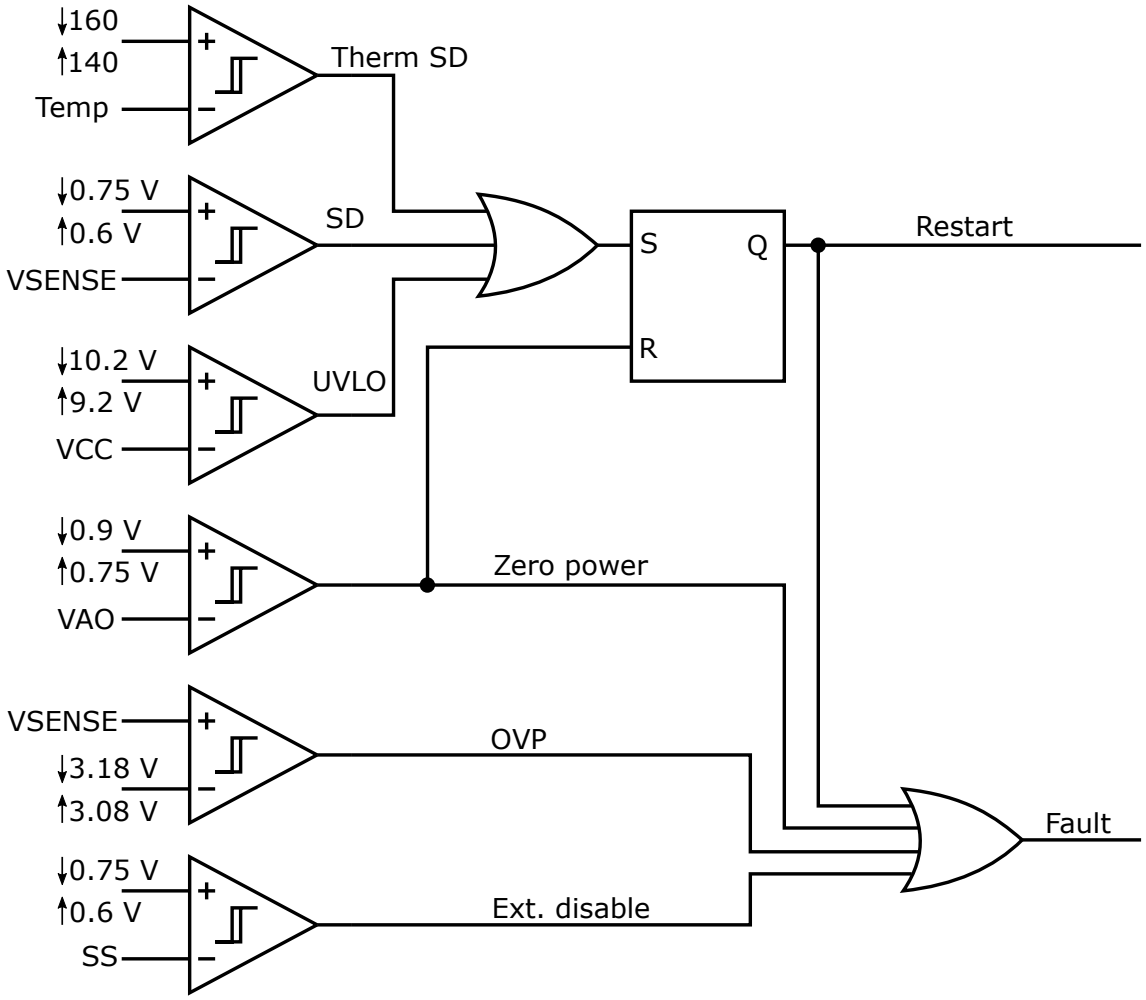


Fig. 9.9 Schematic diagram of protections.

VSENSE and *SS* pins are capable of controlling the corrector branches. When the output voltage is lower than approximately 25% of the nominal value, the corrector is disabled. If the voltage at the *VSENSE* and *VAO* pins exceeds $0.75V$ level, the oscillator, multiplier, and synthesizer are activated. The soft-start circuitry begins with ramping up the voltage on the *SS* pin.

The external driving of the *SS* pin is capable of emulating an internal fault conditions. The *GDA* and *GDB* outputs are instantly disabled and held low when the voltage below $0.6V$ level on the *SS* pin is occurred. If any internal or external fault stimulus are not present, the normal operation of the corrector is resumed. The soft-start circuitry consists an internal adaptive pull-up source which is capable of driving the $1.5mA$ source current. Therefore the external pull-down shall override the pull-up source current and ensure suitable behaviour for an appropriate held below the threshold. The recommendation of the manufacturer is using MOSFET with the 100Ω R_{DSon} resistance or lower [52].

9.15 Design of the Superior Control System

This section is devoted to an implementation of the power management feature into the prototype controlled by *UCC*28070. The controller does not have generally implemented the power management feature. Nevertheless, pins *CAOA* and *CAOB* are capable disabling a A or B channel individually. This feature provides the disabling function in case of a detected error in the particular branch. It suits up for the power management which helps with a performance optimization.

The figure 9.10 shows a block diagram of the solution. The backbone of the corrector is a boost twin which is controlled by the analog control circuit *UCC*28070. Each of them is designed for $500W$ output power. That means an one prototype is able to reach $1kW$ output power at $390V$. An input voltage is sensed by a separate rectifier bridge with a low pass filter and voltage divider. An output current sensing is provided by a shunt monitoring unit based on the *INA*214 differential amplifier with $40dB$ gain. These signals are processed by ADCs.

A superior control system based on the *STM*32*F*4 discovery kit. Output signals from the microcontroller shall be amplified by external transistor drivers. If the transistor is switched on, the *CAOx* is grounded and the controller recognises a fake error. As a consequence, one branch of the corrector is disabled. It operates as a single phase corrector. The performance is optimized in the wide range of the output current.

A flow chart is shown in the figure 9.11. The flow chart begins with an acquisition block which measures input and output parameters of the corrector. Due to the switching noise it is

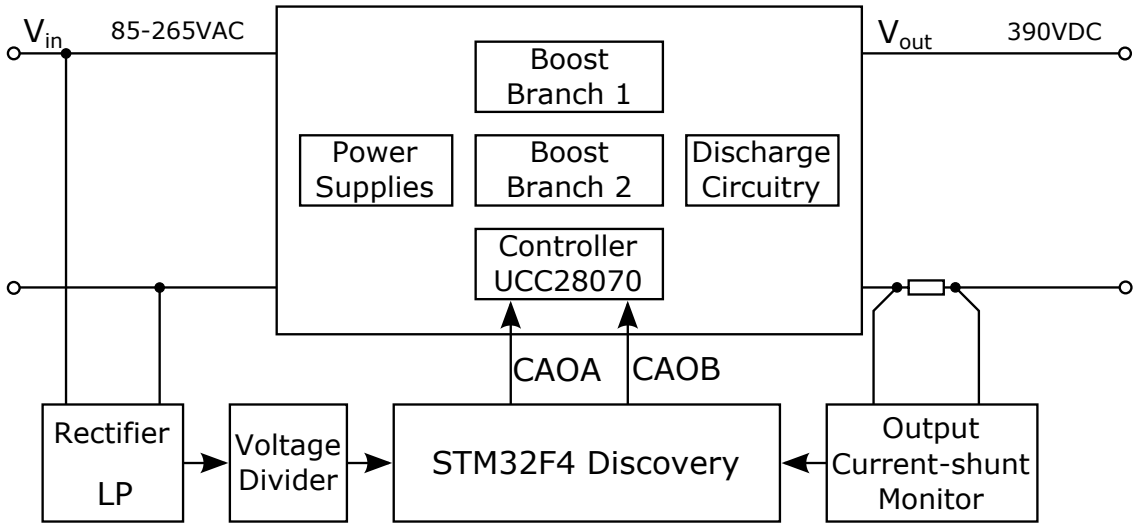


Fig. 9.10 Block diagram of the two phase interleaved corrector.

necessary to provide an averaging function. Then the input voltage amplitude and output current are calculated.

The firmware shall implement appropriate borders between single phase and interleaved operations. The border between a high line and low line was selected a $200V$ amplitude of the input voltage. A hysteresis is set to $20V$. The borders between single phase and interleaved operation were set according to the empirical results of the measurement. The experimental results are represented by the figures 9.18 and 9.19. An appropriate border was set to $300W$ (the $0.75A$ output current) at the $110V$ input voltage. The border was selected due to a downward trend of the curve which represents the single phase operation. Similarly, the experimental data determines the $600W$ border (the $1.5A$ output current) at $230V$ input voltage.

This solution is very profitable due to that the analog controller is responsible for voltage and current regulations. The performance optimization is solved by the superior control system.

In the figure 9.12 is shown a 4-phase interleaved corrector based on the $UCC28070$ analog controller. The $STM32F4$ discovery kit provides the advanced power management and synchronization. This solution was not completely realized. In spite of this fact the solution demonstrates advantages of multi-phase correctors during the development. A conventional design process is slow and uneconomical. In the conventional design, changes of the output power rating lead naturally to a redesigning of all power components and PCB as well.

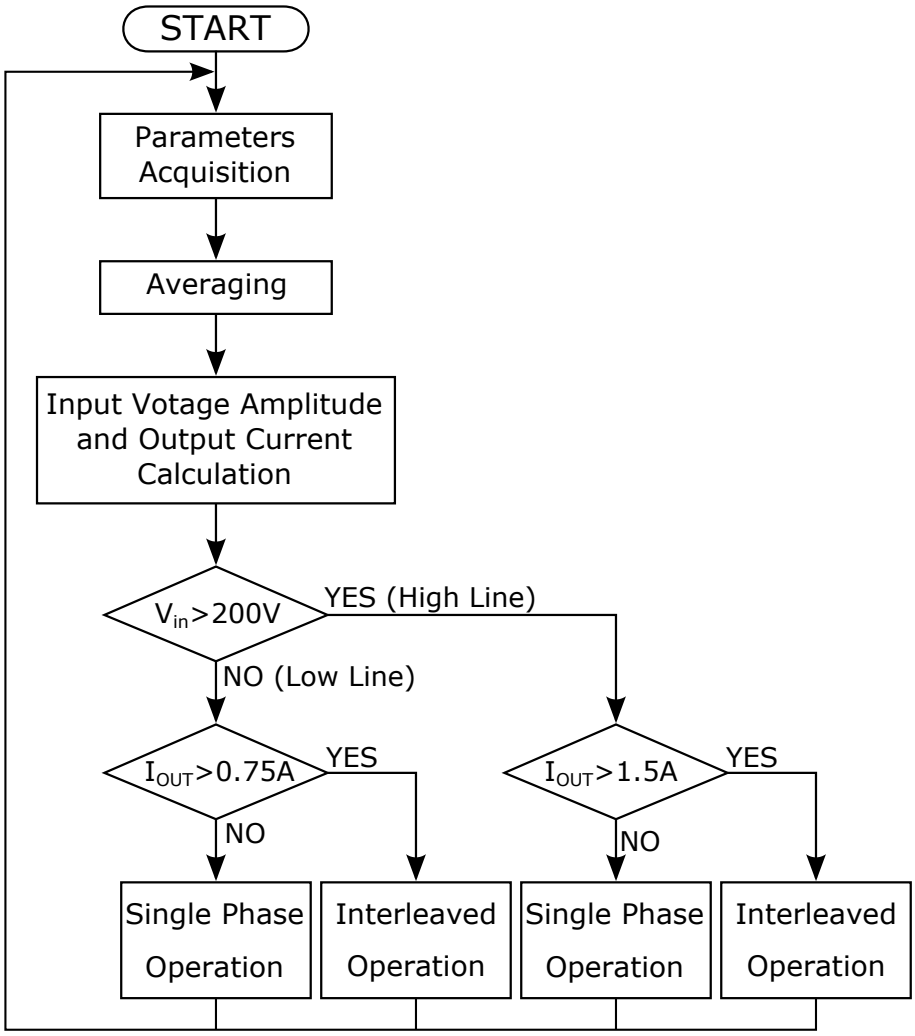


Fig. 9.11 Flow chart of the interleaved corrector.

The main idea of the solution, which is described in the figure, is a modular system of the correctors which is based on the unified corrector. This solution should reduce developing time. Thereby the method save costs for development and mass production. Practically, one prototype with unified power (for example $1kW$) is developed, individual unified branches are merged and operate out of phase to each other.

9.16 Hardware Implementation

The corrector was built on a two layer PCB with dimensions $128x135mm$. The $UCC28070$ controller was chosen due to its flexibility of connection and features. It is characterized as a controller for two phase correctors with the CCM operation. It means that the device is able to drive two boost corrector branches.

Unfortunately, the signals for transistors shall be gained by an external power driver. As the external power driver was used $ADP3634$. The controller includes current sense synthesis, programmable dithering, external synchronisation, quantized feed-forward loop, soft-start, programmable maximum duty-cycle clamp, peak current limitation, and several protection features. All these features fit to multiphase interleaved correctors.

The controller is able to operates under wide range of frequencies from 30 to $300kHz$. The switching frequency plays an important role during the design procedure. Lower switching frequencies lead to bulky power components contrary to higher frequencies which cause higher switching losses. As an appropriate switching frequency it was chosen $200kHz$ which is suitable compromise between dimensions and losses.

The controller is powered by the same buck converter without galvanic isolation which is used in the previous chapter. Auxiliary power source based on the linear regulator supplies an output current-shunt monitor.

The output current-shunt monitor provides a voltage output which represents the output current of the corrector. It includes the shunt resistor 0.01Ω as a sensing element. The voltage drop on the shunt resistor is amplified by the differential amplifier $INA214$ with $40dB$ gain [56]. The output voltage of the current-shunt monitor is determined by the equation 9.70.

$$V_{shunt} = R_{shunt} \cdot I_{out} \cdot gain \tag{9.70}$$

The maximum output power of the whole corrector is $1kW$. The output voltage is set to $390V$. Therefore the output current is in the range from 0 to $2.564A$ which is determined by

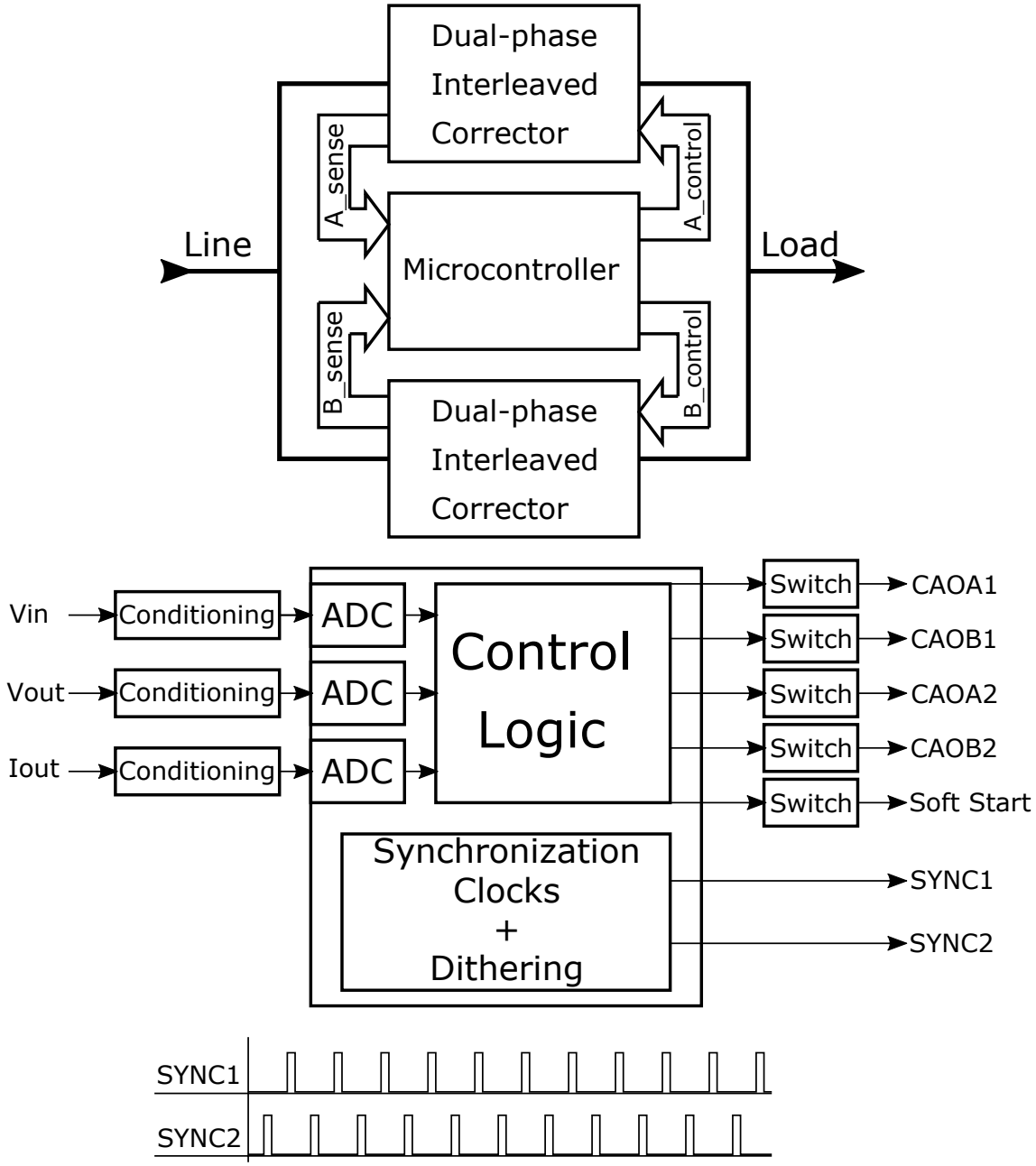


Fig. 9.12 Block diagram of the multiphase interleaved corrector.

the next equation 9.71.

$$I_{out,max} = \frac{P_{out,max}}{V_{out}} = \frac{1000}{390} = 2.564A \tag{9.71}$$

As a consequence, the maximal output voltage of the current-shunt monitor is defined in the equation 9.72. As a result, the output signal is the range from 0 to $2.564V$.

$$V_{shunt} = 0.01 \cdot 2.564 \cdot 100 = 2.564V \tag{9.72}$$

The $UCC28070$ controller needs no sensing resister network. The voltage divider is necessary only for the power management of the corrector.

The line voltage sensing is used same solution as at the previous chapter. It consists of the rectifier, low pass filter, and voltage divider. An upper value includes three resistors with the $3M\Omega$ resistivity. The maximal input RMS voltage is defined to $250V$. Due to the fact an amplitude is calculated by the next expression 9.73.

$$V_{in(max),peak} = V_{in(RMS),max} \cdot \sqrt{2} = 250 \cdot \sqrt{2} = 354V \tag{9.73}$$

The network shall create a voltage within an ADC input range. The range is defined in the interval from 0 to $3.3V$. As a consequence, the bottom resistor is determined in the next equations.

$$R_{in2} = R_{in1} \cdot \frac{V_{ADC(max)}}{V_{in(max),peak} + V_{ADC(max)}} \tag{9.74}$$

$$R_{in2} = 3e^6 \cdot \frac{3}{354+3} = 25.21k\Omega \tag{9.75}$$

According to these calculations a standard $27k\Omega$ resistor was chosen. The verification of the calculation can be provided by the next expressions.

$$V_{ADC(max)} = V_{in(max),peak} \cdot \frac{R_{in2}}{R_{in1} + R_{in2}} \tag{9.76}$$

$$V_{ADC(max)} = 354 \cdot \frac{27e^3}{3e^6 + 27e^3} = 3.15V \tag{9.77}$$

The analog PFC circuit is controlled by *CAOA* and *CAOB* pins. The pins are driven by two external transistors. If the transistor is switched on, the particular branch of the corrector will be disabled. This principle is used for the power management control technique.

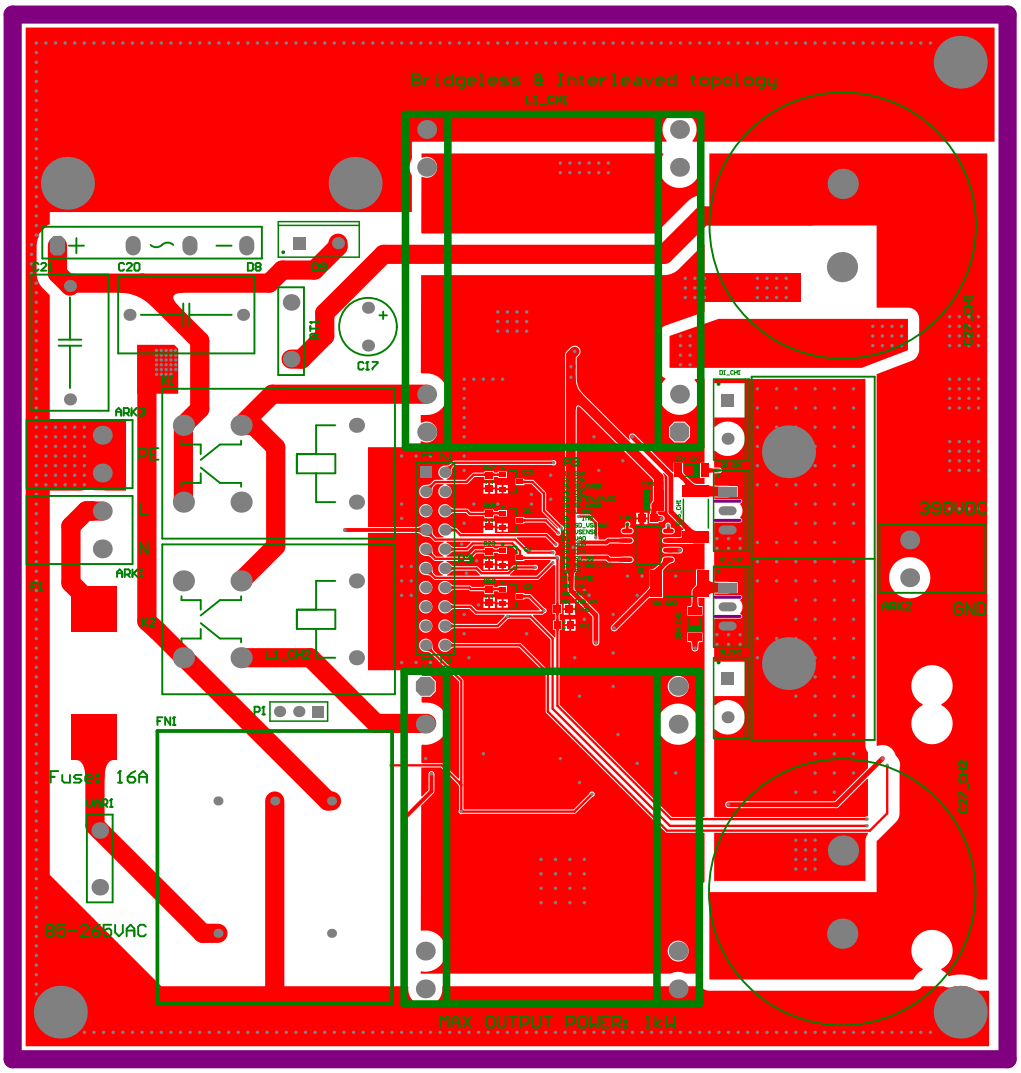


Fig. 9.13 Layout of the corrector - top view (1:1 scale).

The top and bottom layout patterns are shown in the figures 9.13 and 9.14. The next two figures are devoted 3D models of the board. The last figure shows a photo of the hardware realization.

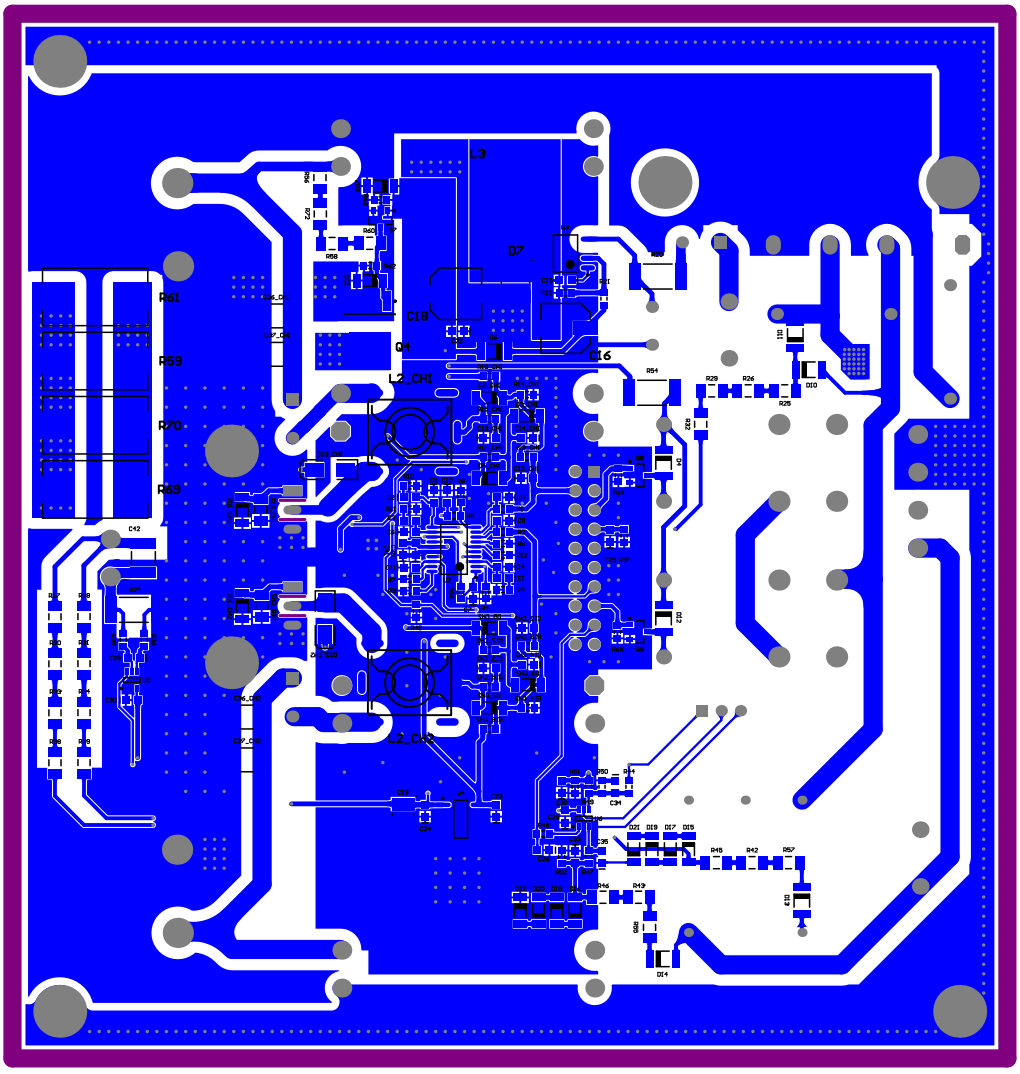


Fig. 9.14 Layout of the corrector - bottom view (1:1 scale).

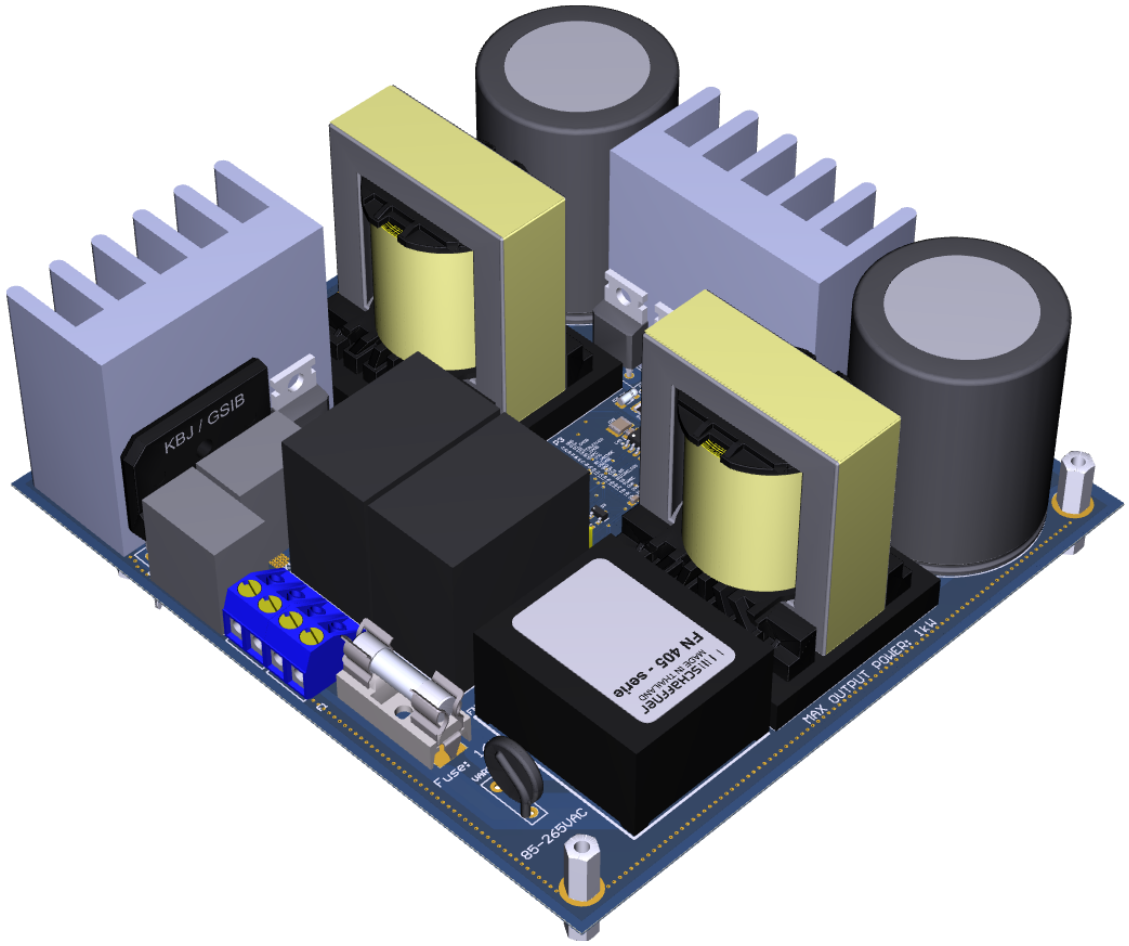


Fig. 9.15 3D model - top view.

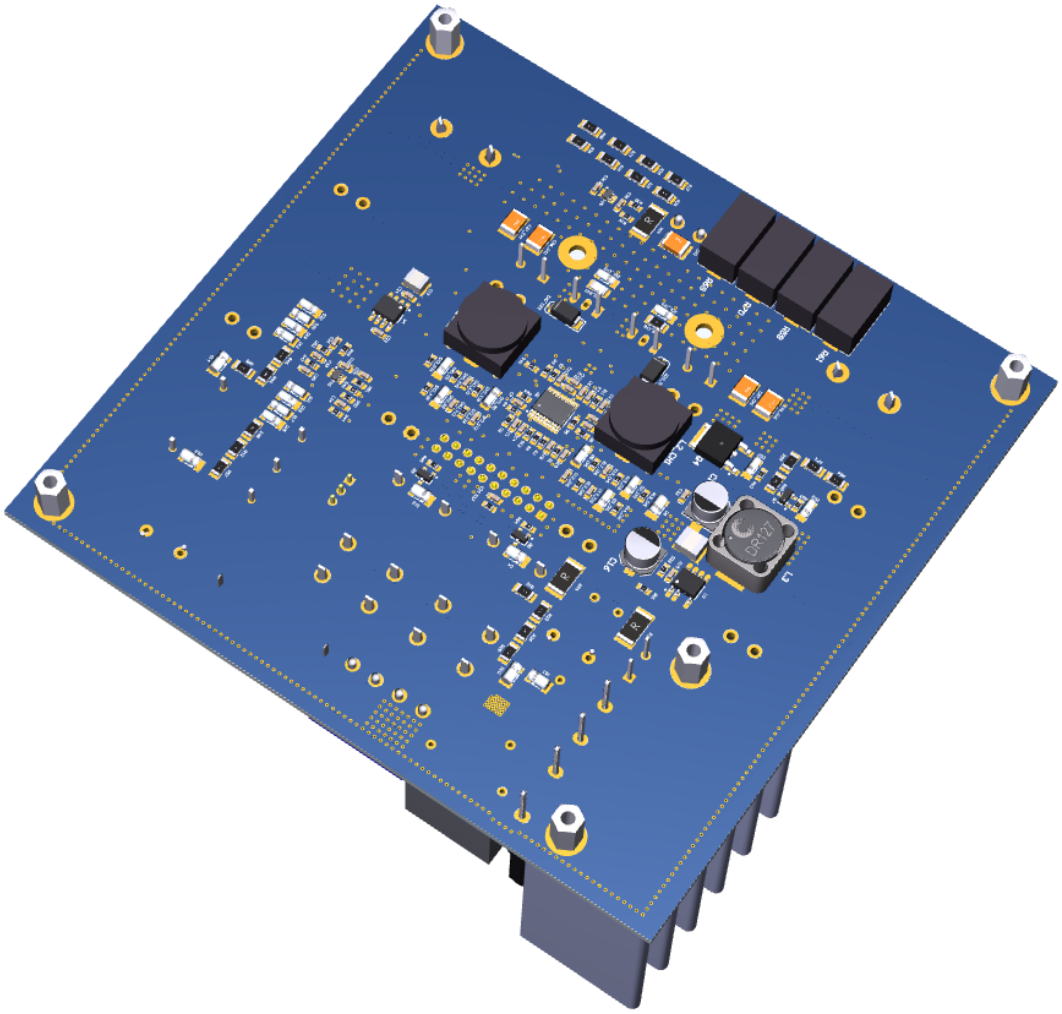


Fig. 9.16 3D model - bottom view.

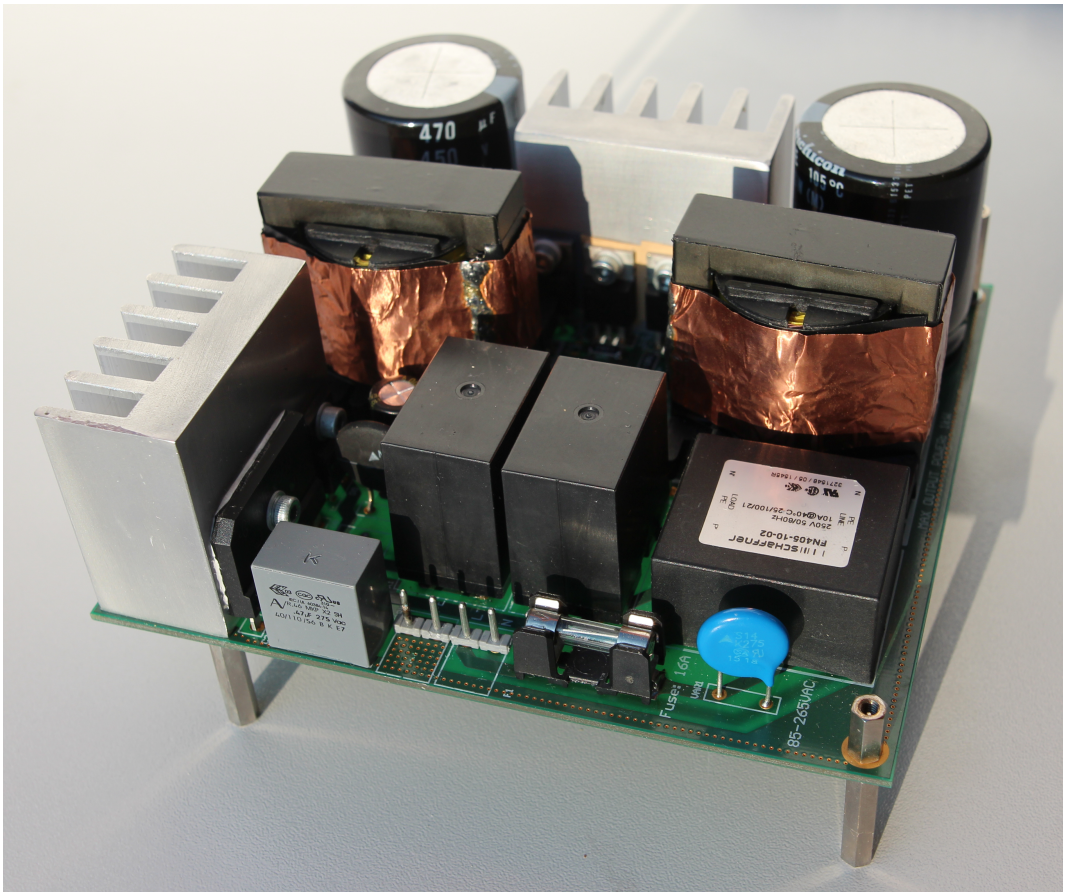


Fig. 9.17 HW realization.

9.17 Bill of Material

This section is devoted to a costs estimation for the prototype of the corrector. The price column includes all components in the row. The estimation is used for a final comparison of the prototypes. The total costs for the prototype with $UCC28070$ controller reaches 140.9 €.

Table 9.3 Simple bill of the material part 1 (UCC28070).

Designator	Type	Quantity	Price [€]
ARK1, ARK2, ARK3	ARK power connector 2-pin	3	1.4
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12_CH1, C12_CH2, C13_CH1, C13_CH2, C14_CH1, C14_CH2, C15, C22, C23, C24, C25, C26, C28, C29, C30, C31, C32, C33, C34, C35, C38, C40, C41	SMD ceramic chip capacitor $100nF$ 0603	34	1.32
C16	SMD radial electrolytic capacitor $10\mu F/50V$	1	0.23
C17	THT radial electrolytic capacitor $1\mu F/350V$	1	0.24
C18	SMD radial electrolytic capacitor $10\mu F/50V$	1	0.25
C19, C39	SMD tantal capacitor $2.2\mu F/35V$ 1411	2	0.42
C20, C21	THT foil capacitor $470nF/275VAC$	2	1.08
C27_CH1, C27_CH2	THT radial electrolytic capacitor $470\mu F/450V$	2	9.62
C36_CH1, C36_CH2, C37_CH1, C37_CH2, C42	SMD ceramic chip capacitor $100nF/630V$ 2512	5	3
D1_CH1, D1_CH2	SiC Schottky diode $C3D10065$	2	8.64
D2_CH1, D2_CH2, D3_CH1, D3_CH2, D5_CH1, D5_CH2, D15, D16, D17, D18, D19, D20, D21, D22	Universal diode $1N4148$	14	1.12
D4, D6, D10, D11, D12, D13, D14	Universal diode BYD37M $1000V/1A$	7	0.77
D7	Ultrafast diode $600V/1AMURS160-13-F$	1	0.36
D8	Bridge $800V/25AGSIB-5SGSIB2580$	1	1.94
D9	Ultrafast diode $600V/30AFFPF30UA60S$	1	0.87
D23-CH1, D23-CH2	Transil $550VP4SMA550A$	2	0.96
F1	Fuse $10A/250V$ + fuse holder	1	0.5

Table 9.4 Simple bill of the material part 2 (UCC28070).

Designator	Type	Quantity	Price [€]
FN1	EMI Schaffner FN402-10-02 $250V/10A$	1	11.88
K1, K2	RELE $12V - 230V/15A$ G4W-2212P-US-TV-5	2	14.48
L1_CH1, L1_CH2	Power inductor $ETD44$	2	12
L2_CH1, L2_CH2	PULSE Current sense transformer 1 : 1 : 50 PE68210NL	2	4.48
L3	Power inductor $1mH/260mA$ DR127-102-R	1	1.06
P1	Header $3x1$	1	0.12
P3	Header $5x2$	1	0.49
Q1_CH1, Q1_CH2	Power MOSFET $SPP20N60S5$	2	5.32
Q2, Q3, Q7, Q8, Q9, Q10, Q11	Power MOSFET $SQ2360EES$	7	2.31
Q4	Power MOSFET $IRFRC20PBF$	1	0.87
R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13_CH1, R13_CH2, R14_CH1, R14_CH2, R15_CH1, R15_CH2, R17_CH1, R17_CH2, R19_CH1, R19_CH2, R21, R22, R23, R35, R36, R37, R40, R41, R44, R47, R48, R49, R50, R51, R52, R53, R62, R63, R64, R65, R66, R67, R68	SMD chip resistors 0603	45	1.75
R16_CH1, R16_CH2, R20, R24, R54	SMD chip resistors 10Ω 2512	3	0.5
R24	SMD chip resistors $10m\Omega$ 2512	1	0.48
R18_CH1, R18_CH2, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R38, R39, R42, R43, R45, R46, R55, R56, R57, R58, R60, R72	SMD chip resistors 1206	24	1.87
R59, R61, R69, R70	SMD power resistor $SMF5W33KJ$	4	3.58

Table 9.5 Simple bill of the material part 3 (UCC28070).

Designator	Type	Quantity	Price [€]
RT1	Inrush NTC termistor $250V/5A$	1	0.8
U1	High speed dual MOSFET Driver $4AADP3634$	1	2.24
U2	PFC controller $UCC28070$	1	4.31
U3	LinkSwitch $LNK304$	1	1.26
U4	Low drop voltage regulator $LE33CD$	1	0.81
U5	Current shunt monitor $INA214$	1	1.28
U6	Analog comparator $ADCMP608BKSZ-R2$	1	2.44
VAR1	Varistor $S14K275$	1	0.23
ZD1_CH1, ZD1_CH2, ZD2, ZD3, ZD4_CH1, ZD4_CH2	Zener diode $TZM5248B-GS08$ $18V/0.5W$	6	1.08
Heatsinks	Customized heatsink profiles	2	5
PCB	PCB $128x135mm$ $(1.73dm^2)$	1	24.45
Total			140.9

9.18 Experimental Results

9.18.1 Performance Measurements

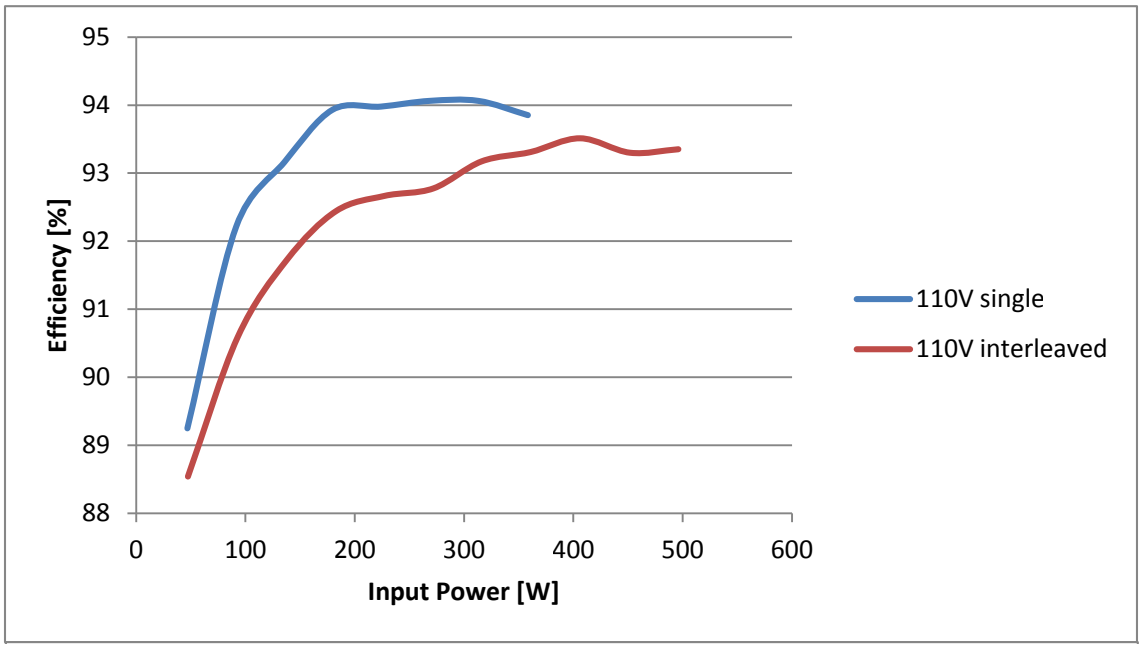
The measurement was carried out according to the schematic diagram shown in the section 6.5. The graph 9.18 demonstrate efficiency and performance of the corrector at low line $(110V)$. The results at high line $(230V)$ are shown in the figure 9.19. All graphs include two curves each for different operating conditions. The red curve represents single operation of the corrector. The blue one corresponds to the interleaved operation.

The efficiency at low line and nominal power is 93.3% with interleaving. The peak efficiency at low line and single phase operation overcomes 94%. The graph shows areas where single operation can improve the corrector efficiency. The single phase operation at low line improves the performance of the corrector up to $300W$. For higher power is suitable an activation of the interleaving.

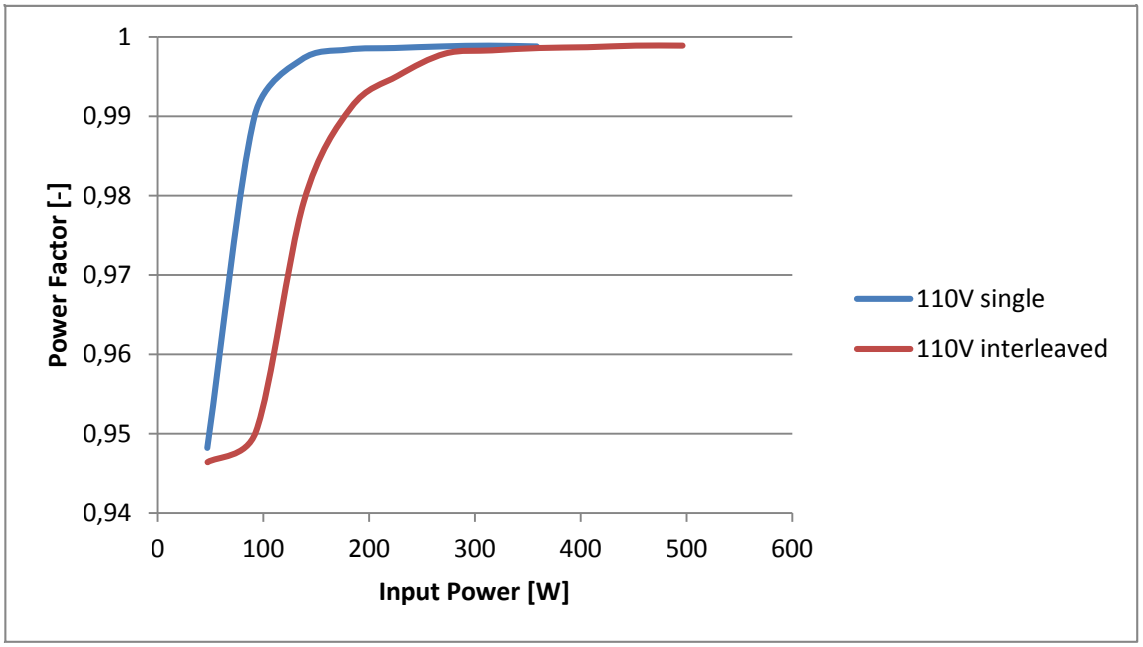
At high line the corrector takes advantage of the single phase operation into the measured range. The differences between curves is negligible, therefore the interleaving is preferable approximately over $600W$ due to better heat dissipation. The intersection of the curves depends on the construction of the corrector, component selection and control method. The benefit of the single phase operation plays crucial role especially at light load. The performance measurement, when the power management is enabled, is depicted in the figure 9.20.

9.18.2 Harmonic Content according to ČSN EN 61000-3-2 Standard

The harmonic content of the input current was investigated by the same setup as in case of the performance measurement. The corrector meets the harmonic order limits for the line current according to the ČSN EN 61000-3-2 standard [42]. The measurement of the harmonic content of the input current was performed at three input power values $100W$, $300W$ and $500W$. The measurement includes experimental data for single and interleaved operation. The measurement results are shown in figure 9.21. All figures include a harmonic order current limit which is calculated according to the ČSN EN 61000-3-2 standard [42] which defines two limits for D class. First limit is related to current over the power (mA per W). This limit is dependent on the input power of the corrector. The second limit defines absolute limit for the standard. The measurement uses only first criterion for comparison the measured data to the limits described in the standard. The comparison shows that the experimental results fulfilled limits set by the standard [42].

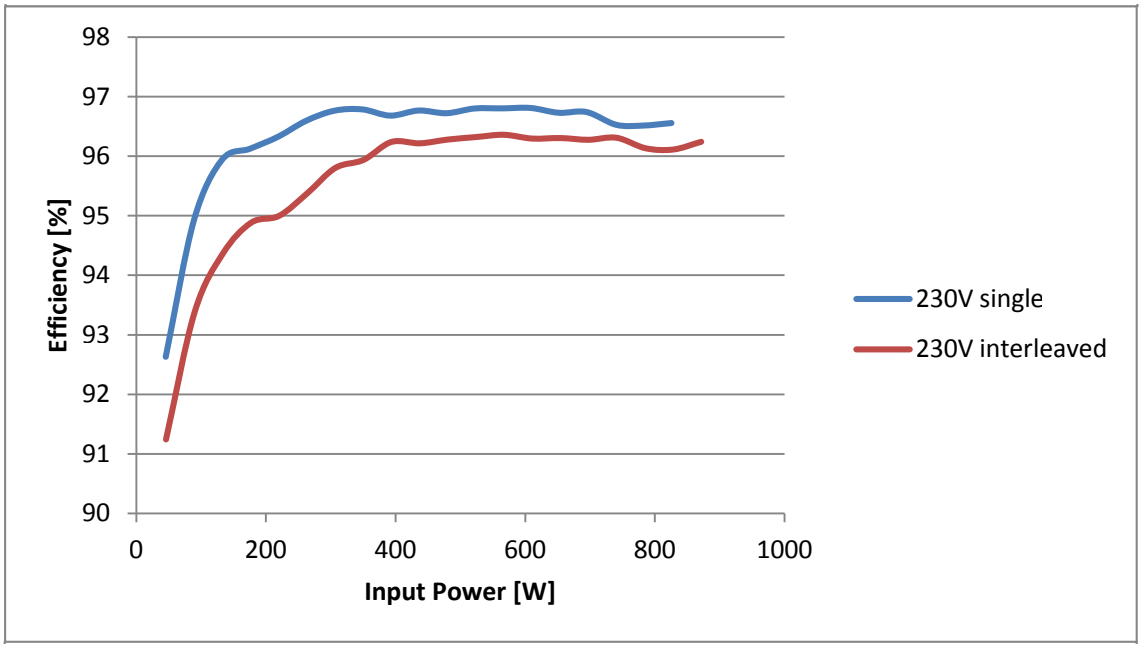


(a)

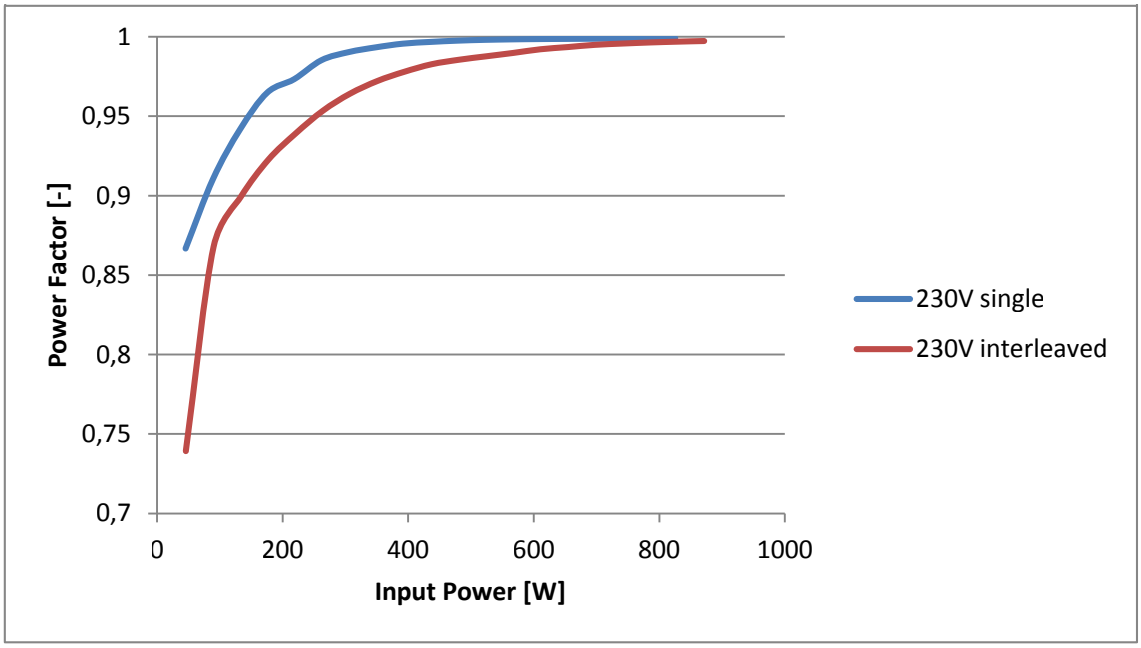


(b)

Fig. 9.18 Performance measurement of the corrector based on the UCC28070 controller a) efficiency at 110V, b) Power Factor at 110V.

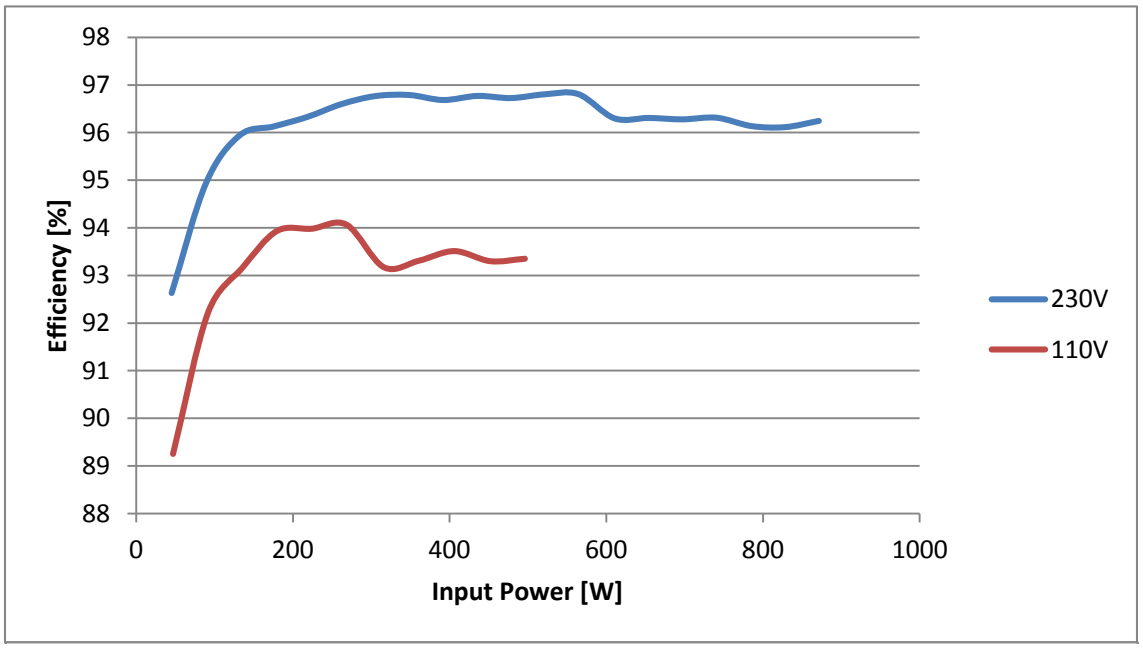


(a)

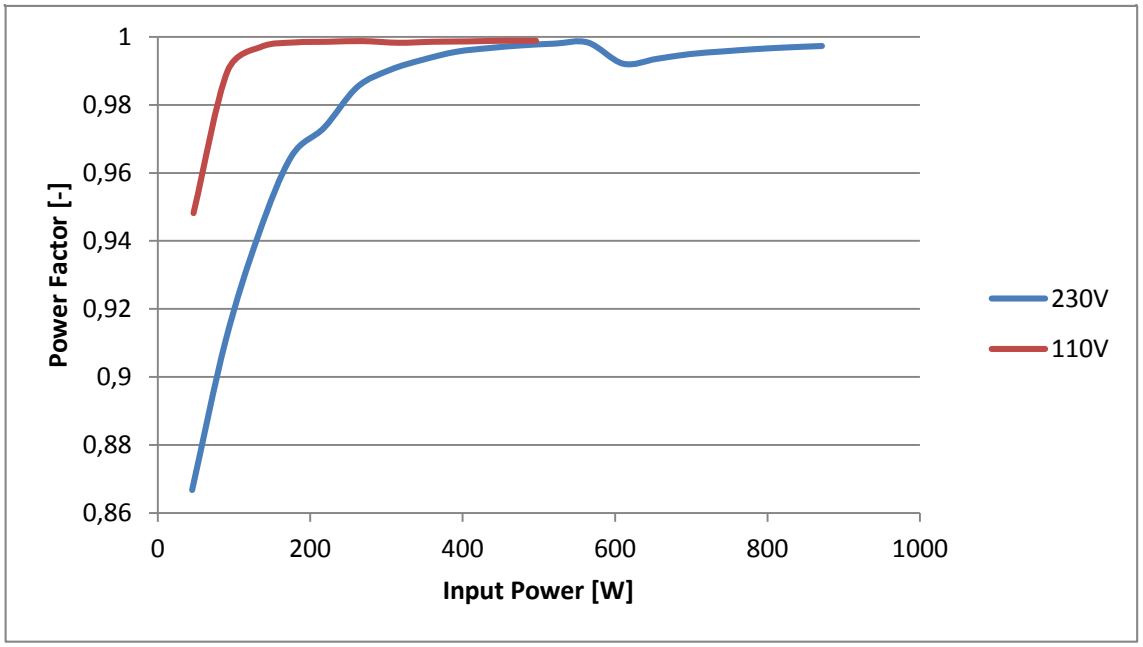


(b)

Fig. 9.19 Performance measurement of the corrector based on the UCC28070 controller a) efficiency at 230V, b) Power Factor at 230V.

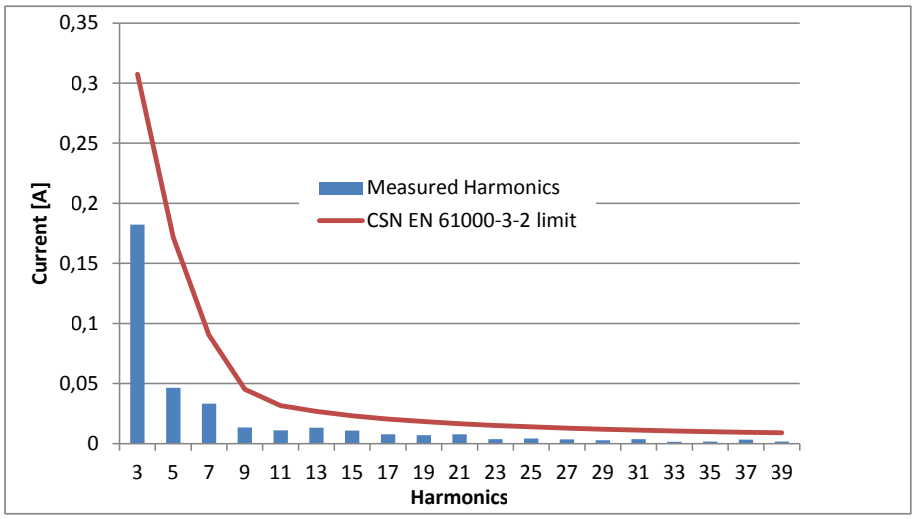


(a)

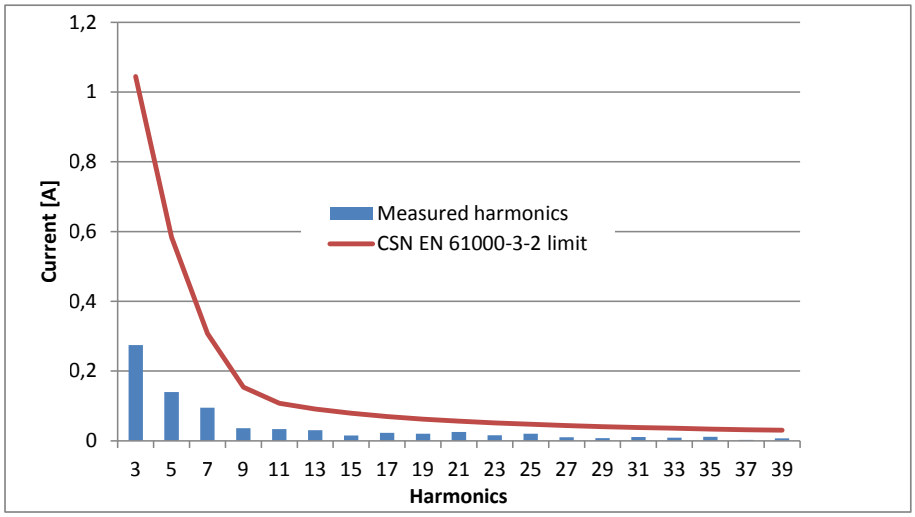


(b)

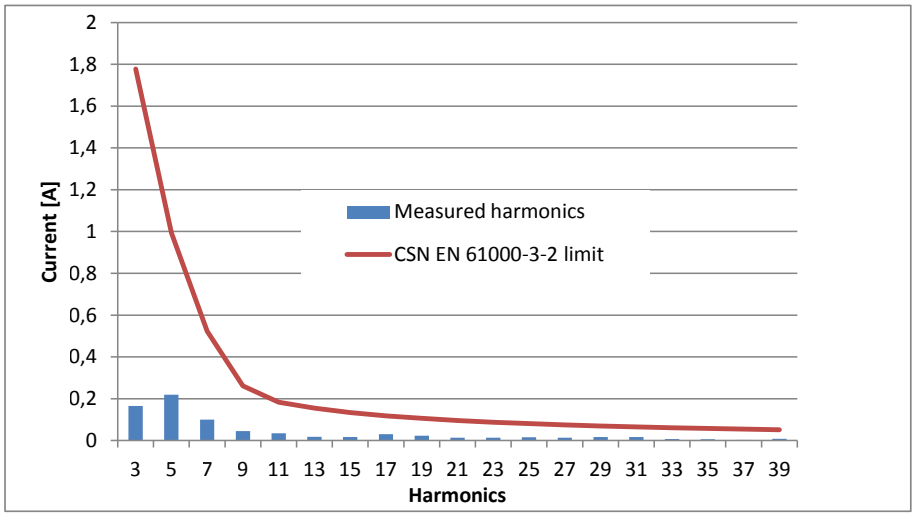
Fig. 9.20 Performance measurement of the corrector based on the UCC28070 controller with power management feature a) efficiency, b) Power Factor.



(a)



(b)



(c)

Fig. 9.21 Harmonics content of the corrector at different loads (interleaving is disabled), a) 100W, b) 300W, c) 500W.

9.18.3 Conductive EMI Test

The conductive EMI test setup was based on the section 6.7. The experimental results were summed up in the figure 9.22. The figure 9.22 a) shows the results for the corrector without EMI optimisation. The corrector uses CCM with fix switching frequency which was set to $200kHz$. The gate resistors have 4.7Ω resistivity. The high-speed MOSFET transistors was used as switching elements and SiC Schottky diodes as a boost rectifier.

The using MOSFET transistors with 4.7Ω gate resistance brings a short transients. As a result the switching losses are minimised but EMI noise is gained at high frequency.

The design of the corrector has direct impact on the EMI performance. The figure 9.22 a) includes narrow peaks at multiples of the fundamental frequency. Due to the short transients the high frequency content is rose. Several peaks exceed the limit for EMI standard ČSN EN 61000-6-4 [44].

The second option of the corrector is characterized by reduced switching frequency to $120kHz$. The gate resistor was replaced by 10Ω gate resistors. The transistor is improved by snubber circuit. The amplitudes of the harmonic content is reduced by frequency dithering in the range from 110 to $130kHz$. Both cases use same EMI filter Schaffner FN2090-10-06 [40].

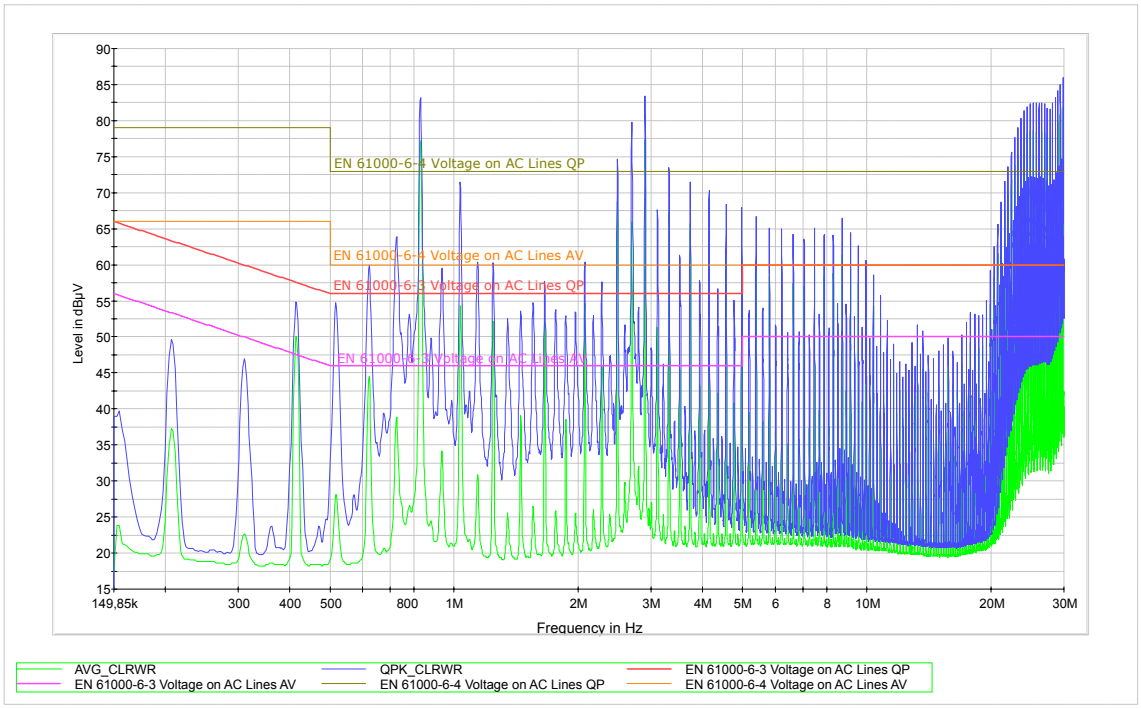
The figure 9.22 b) shows measured data of the optimised corrector. The graph includes flat and smaller peaks of the harmonics. The spectrum is continuous in the full scale. The limit for standard ČSN EN 61000-6-4 [44] is fulfilled. The more strict standard ČSN EN 61000-6-3 [43] is not fulfilled due to the data exceeds the limit. The better results should be reached by following complete revision of the layout. The results are also affected by a grounding. If the corrector uses direct grounding based on the wide copper plate, the high frequency currents flows directly to ground. In case of using flexible cable for connection of the filter and corrector is necessary used the EMI filter with better attenuation at higher frequencies.

9.18.4 Thermal Measurement

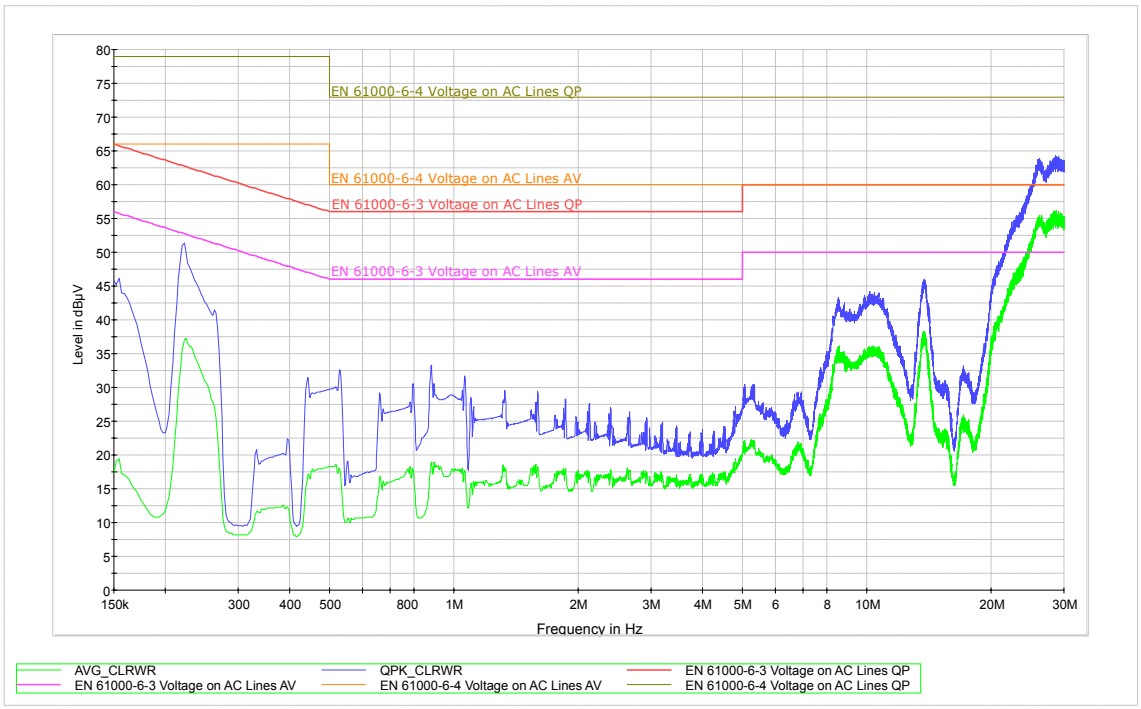
The thermal measurement was performed at $500W$ and $900W$. The first group of the figures 9.23 show the thermal images of the components at $500W$ input voltage with active cooling. The second group of pictures depicts same load conditions without the active cooling. The fan, which was used for active cooling, has $240m^3/h$.

Third group shows the thermal images of the corrector at the nominal power.

The first figure is focused on the top view of the corrector. The bridge rectifier is the component with the highest temperature on the board. The figure b) shows the isometric

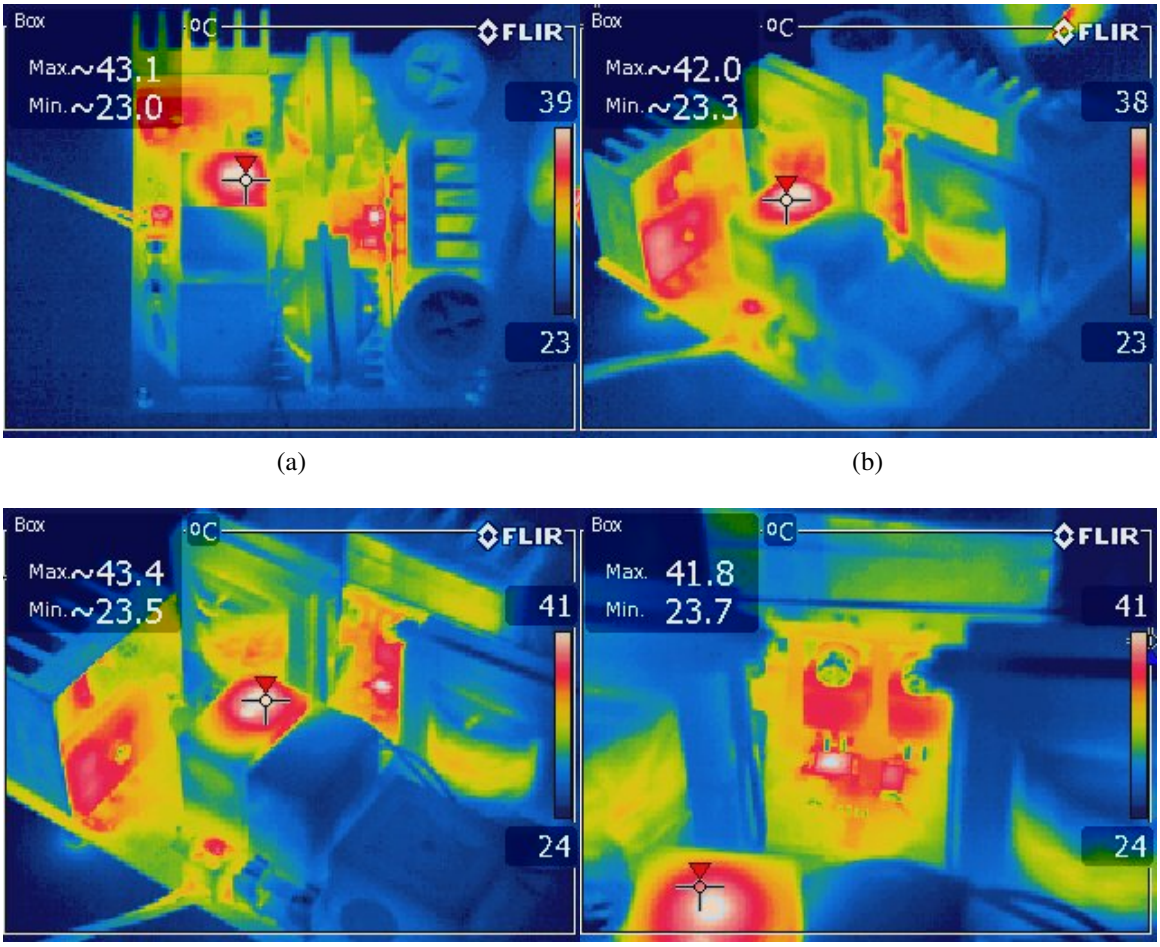


(a)



(b)

Fig. 9.22 Conductive EMI test results, a) graph of the emissions without the optimization for EMI, b) graph of the emissions with the optimization for EMI.

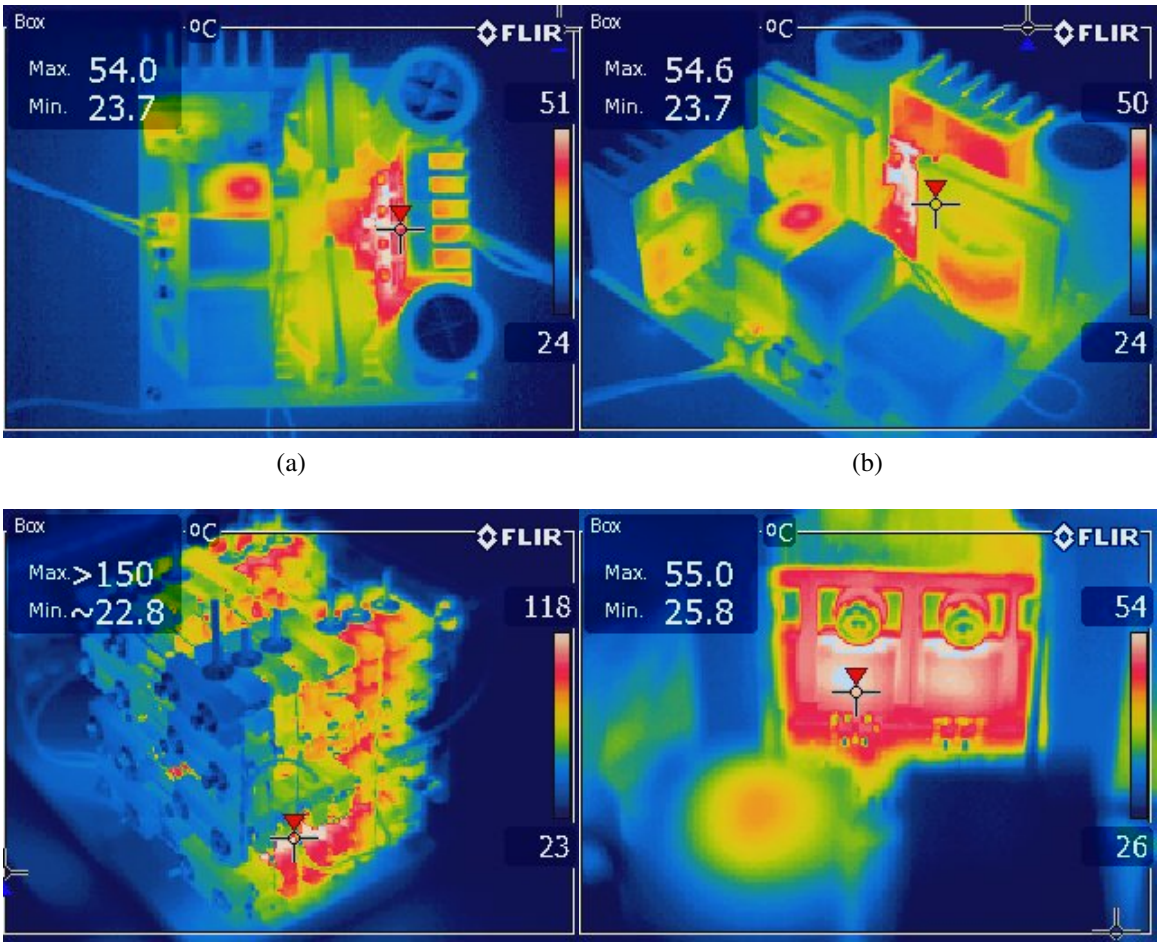


(a) (b)

(c) (d)

Fig. 9.23 Thermal image of the APFC based on UCC28070 which operates at 500 W output power with active cooling, a) top view, b) isometric view, c) thermal image of the rectifier bridge, d) thermal image of the MOSFET transistors.

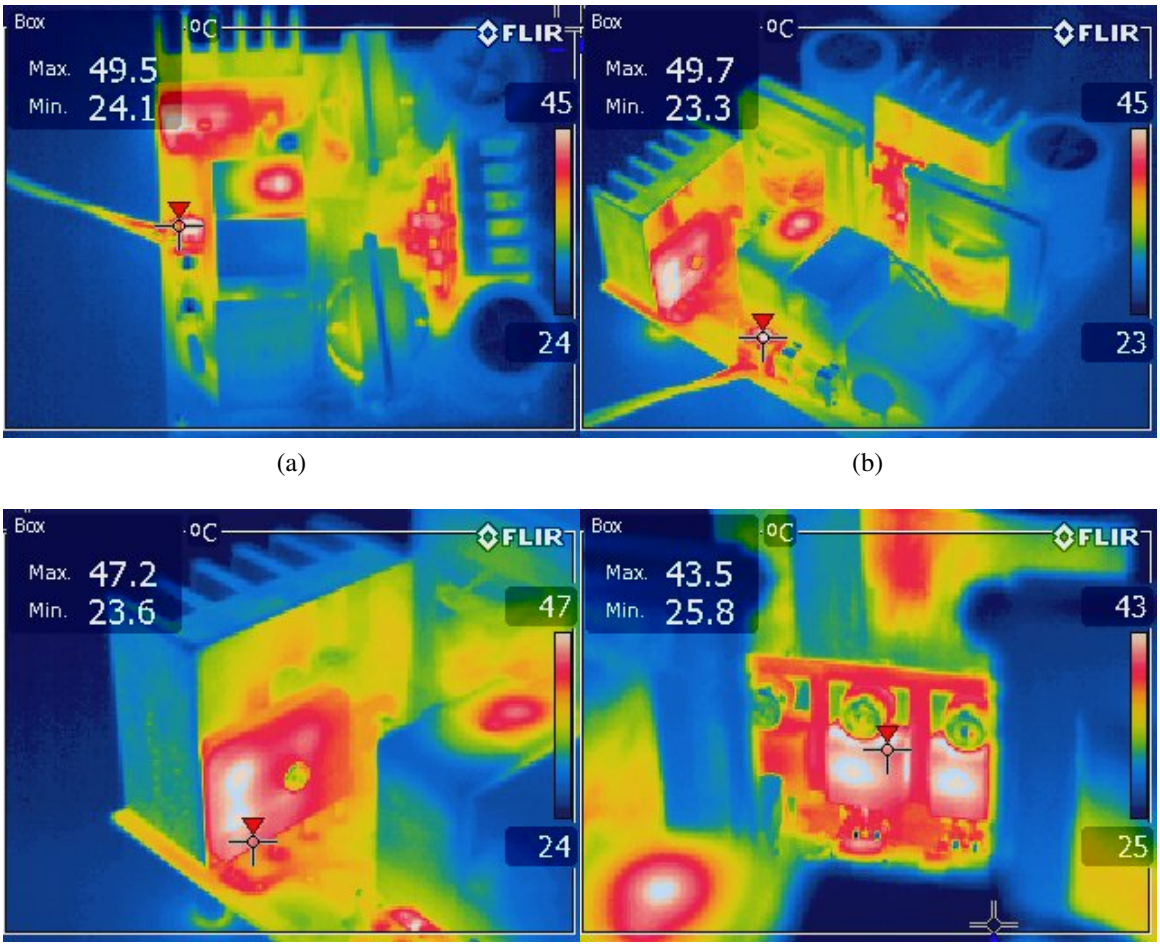
view on the corrector. The detail of the bridge rectifier and power inductor is presented by the c) and d) segments.



(a) (b)

(c) (d)

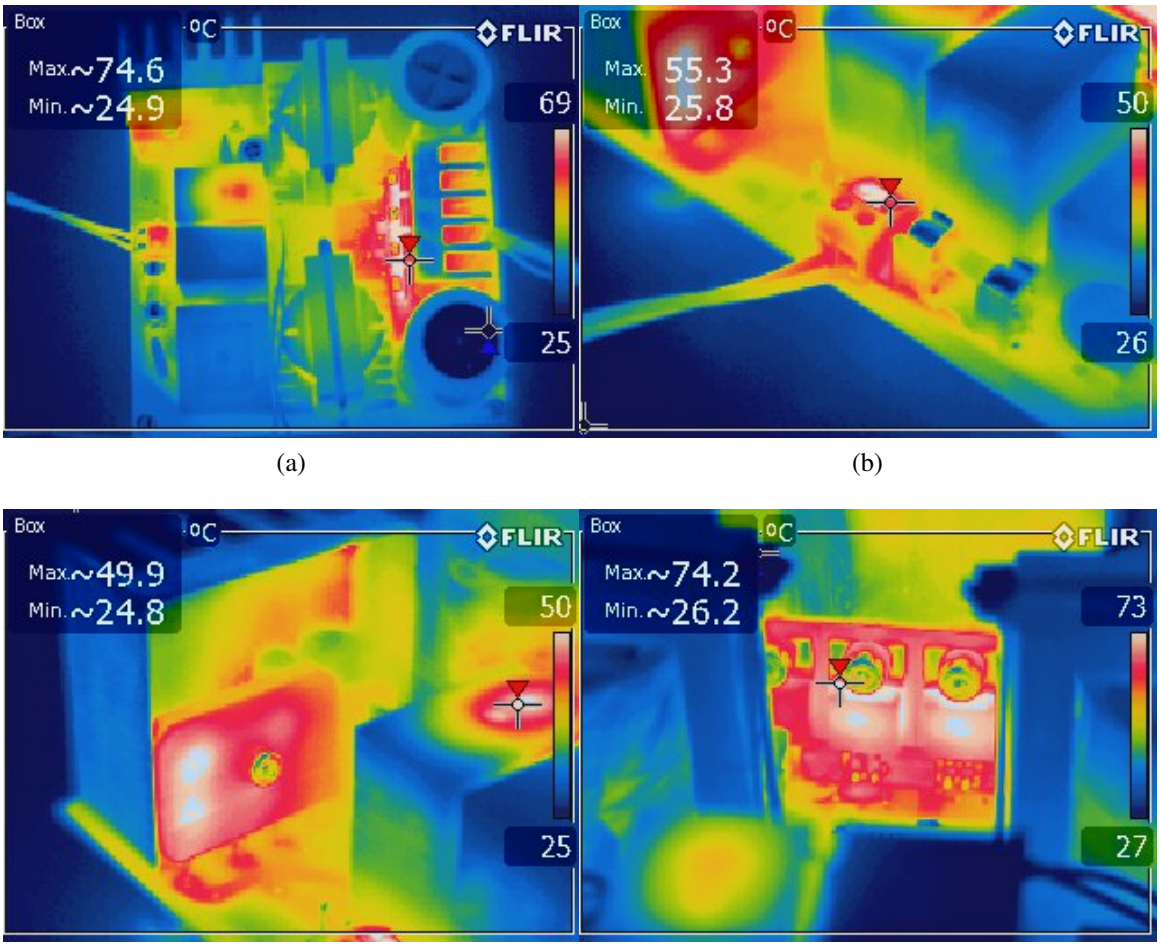
Fig. 9.24 Thermal image of the APFC based on UCC28070 which operates at 500 W output power without active cooling, a) top view, b) isometric view, c) view on the resistive load, d) thermal image of the MOSFET transistors.



(a) (b)

(c) (d)

Fig. 9.25 Thermal image of the APFC based on UCC28070 which operates at 900 W output power with active cooling, a) top view, b) isometric view, c) view on the rectifier bridge, d) thermal image of the MOSFET transistors.



(a) (b)

(c) (d)

Fig. 9.26 Thermal image of the APFC based on UCC28070 which operates at 900 W output power without active cooling, a) top view, b) thermal image of the input connector, c) thermal image of the rectifier bridge, d) thermal image of the MOSFET transistors.

Chapter 10

PFC based on the UCD3138 Controller

This chapter describes a digitally controlled APFC based on the $UCD3138$ microcontroller which was bought for evaluation reasons. The main aim of this chapter is a description of basic components of the circuit and algorithms used for control of the corrector. Information was obtained from application notes and data sheets of the manufacturer. The firmware was already implemented in the original design kit. Experimental results were compared with data of the other prototypes. These result provides a valuable information with is used for a evaluation process in the discussion chapter.

10.1 Block Diagram

A basic schema shows the conventional boost converter complemented by bridge rectifier and EMI filter. The EMI filter is used for switching noise elimination and rectifier is for line voltage rectification. The bulb capacitor is moved behind the converter. The main board allows to change single boost corrector topology to interleaved topology or bridgeless topology.

This change is possible by linking some terminals. If will connected terminals $E2$ and $E6$, and $E3$ and $E1$, the topology will be bridgeless. If will be connected together terminals $E6$ and $E4$, and $E1$ and $E5$, the interleaved topology allows to activate. The topology changes must be followed by firmware changes.

The basic single boost topology will be create when terminals E4 and E6 will be connected together (all terminal connections is described in [53])

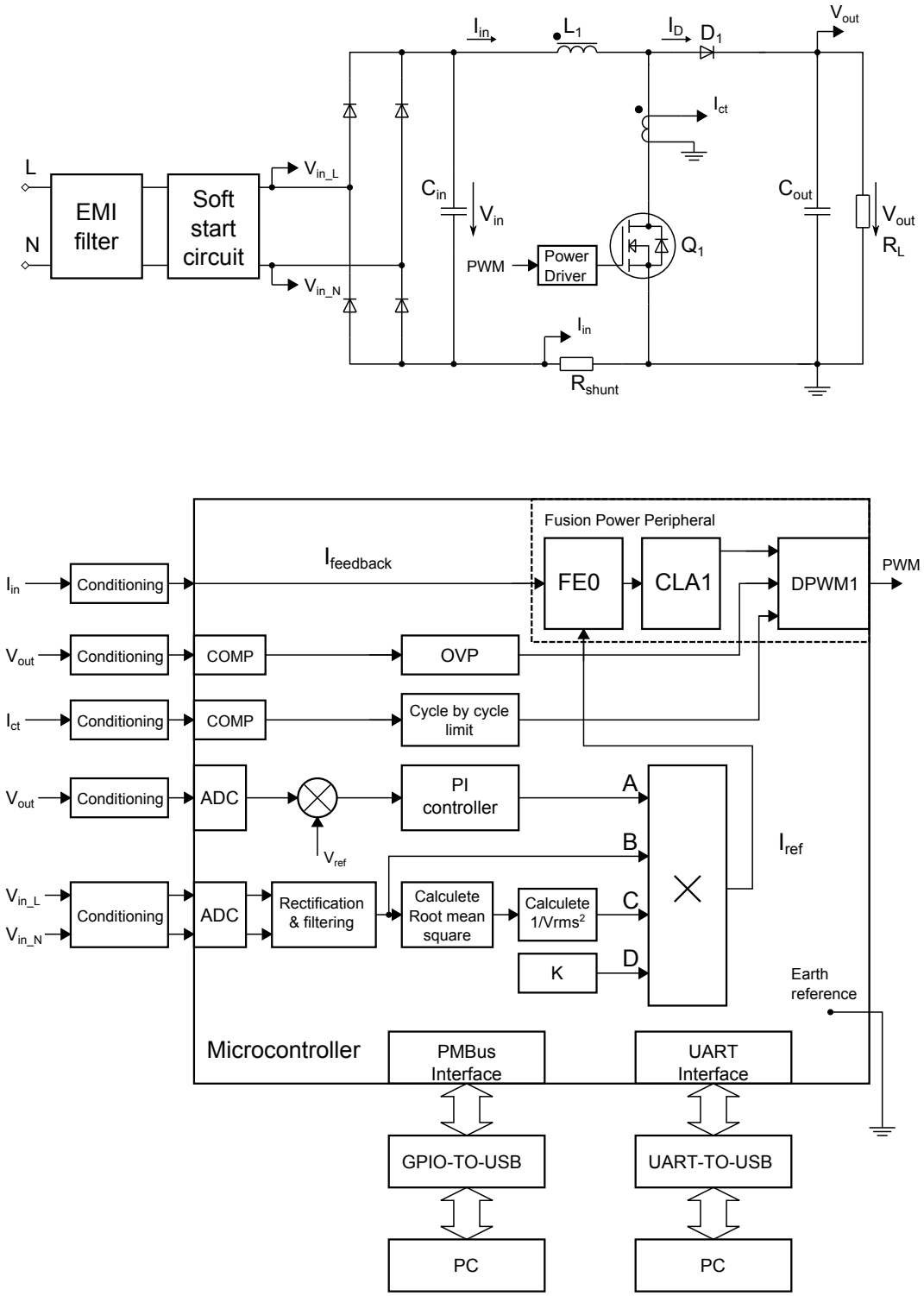


Fig. 10.1 Block diagram of the corrector.

10.2 Main Program

The main program includes variables, constant and function definitions. Then, it contains an initial setting of the microcontroller. Next, it has an infinite control loop which contains all non-time critical function callings for the control strategy [49].

10.3 Program Architecture

An program architecture is divided into background control loop, standard interrupts and fast interrupts. The background of the control loop includes system initialization, feed forward control loop, power metering, PMbus communication and system monitoring. The standard interrupt contains analog to digital conversion, PFC state machine control, calculation RMS value of the input voltage, output feedback loop and current reference calculation. The fast interrupts is used for time critical task as over voltage protection [49].

10.4 PFC State Machine Control

The PFC state machine control determines states of the operation depending on the previous state and control variables. The state machine can be illustrated by the following diagram 10.2. The diagram describes clearly start up and fault states. When the corrector is connected to the line voltage which is smaller than $85V$, the corrector is in a sleep mode. If the input voltage raises over this value, the APFC starts up. An inrush current relay is switched on with a delay. If the relay is switched on, the APFC is in the ramp up state. It means that the output voltage rises up to $390V$, then it is in the on-state.

Fault modes are also described in the diagram. If the output voltage exceeds $420V$ during a ramp up state or $435V$ during a normal operation, the PFC will be shutted down and latched. This fault state is caused by a serious hardware fault therefore it is served by a fast analog comparator. The state "hiccup" is provided by a software solution due to the reason of this state which is a load transient [55].

10.5 Signal Conditioning

Signals for analog to digital converters and comparators shall be properly set to maximal values so that the measured values will be in the range of ADC. The ADC measurement range is from 0 to $2.5V$ as well as in the case of comparators. The error ADC, which is used for a current feedback, has the measurement range from 0 to $1.6V$. A maximal usage of

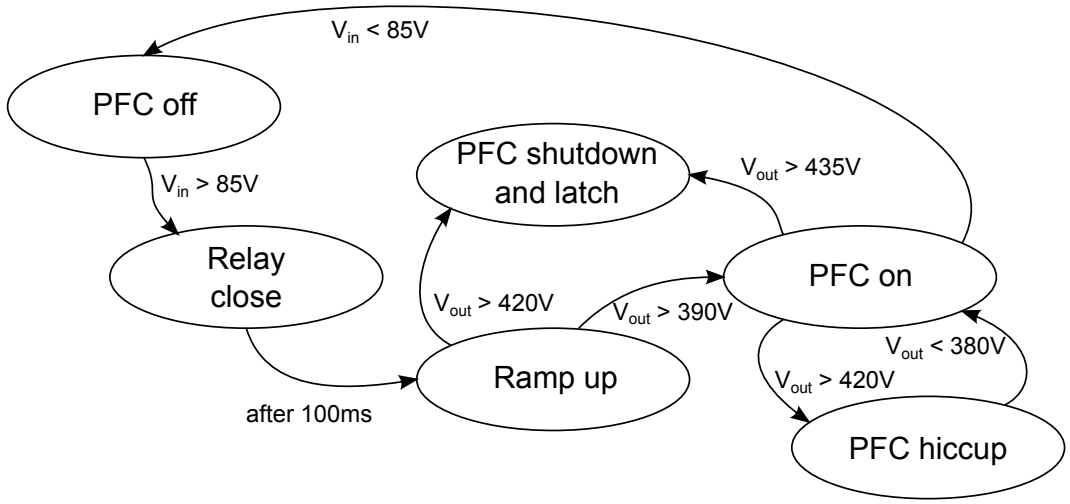


Fig. 10.2 Diagram of the PFC state machine.

the range is preferred due to the best signal-to-noise ratio. The constants are computed as follows:

$$K_{Vin} <= \frac{2.5}{\sqrt{2} \cdot V_{in,max}} \tag{10.1}$$

$$K_{Vout} <= \frac{2.5}{V_{out,max}} \tag{10.2}$$

$$K_i <= \frac{1.6}{I_{in,max} \cdot R_{shunt}} \tag{10.3}$$

The K_{Vin} constant represents the input voltage divider. K_{Vout} is the output voltage divider constant. The last constant K_i is a measuring constant for the input current [49].

10.6 Analog to Digital Converter

An analog to digital converter (ADC) is used for the conversion input and output voltages. A block diagram is shown in the figure 10.3. This converter is 12-bits successive approximation ADC with 16 channels. A typical conversion speed is $267ksps$. It has several features (averaging, variable trigger events, interrupt capability, digital comparators and many others). In spite of the fact that the ADC is high speed, it is suitable for monitoring and low speed control loops. For high speed purposes an error ADC shall be used. The error ADCs, which are a part of the digital power peripheral modules, are designed especially for high speed closed feedback loops [55], [49].

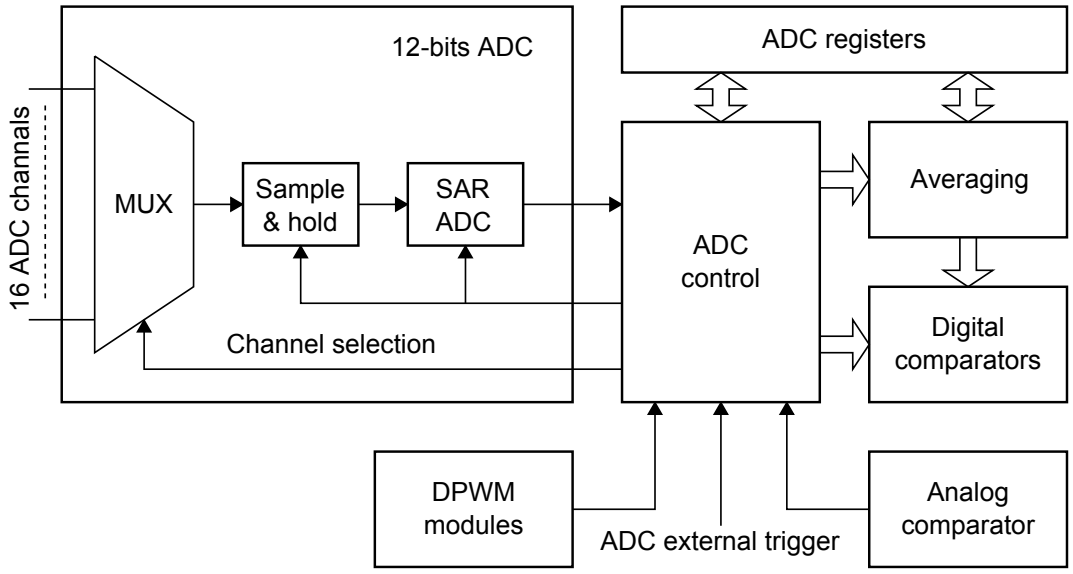


Fig. 10.3 Block diagram of the analog to digital converter.

10.7 Voltage Feedback Loop

A voltage feedback loop provides an output voltage regulation. The feedback loop has usually a very low bandwidth due to a volume capacitor at the PFC output. The low bandwidth allows to design a pure software solution of this loop. The output voltage sensing is given by the ADC. A converted value of the output voltage is compared with the output voltage target. The difference between them creates an error voltage signal which is modified by a proportional integral controller. It shall be able to cope with a load transients as well as a normal operation during a steady state owing to these requirements the controller is equipped by a non-linear gain.

If the error voltage crosses a determined level, the greater gain is applied. The situation is described by the flow diagram 10.4. The integrator has a memory therefore a firmware shall be protected against the overflow. For this reason, the integrator clam is applied. Additionally, the program includes an output voltage clamp which protects the output of this controller [49].

10.8 Feed Forward Loop

A feed forward loop regulates the current through the shunt resistor. The feed forward loop compares a reference signal with a voltage drop across the shunt resistor which is proportional to the input current. As it was mentioned before, the reference voltage is a product of the error signal from a voltage feedback, input voltage signal, compensating signal, and gain

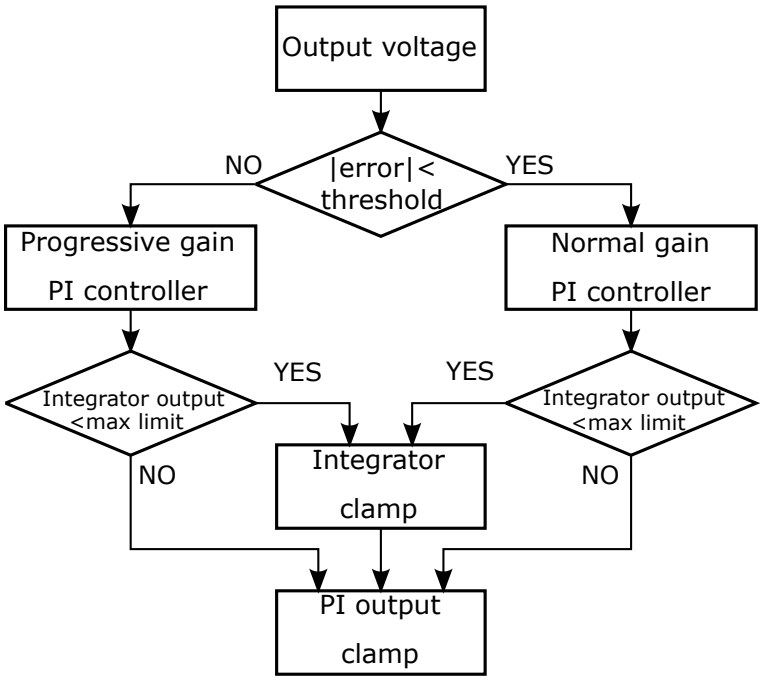


Fig. 10.4 Flow diagram of the PI controller.

constant. It is shown in the block diagram 10.7. The loop uses the error ADC, digital filter, and digital PWM module [49].

$$I_{ref} = A \cdot B \cdot C \cdot D \tag{10.4}$$

$$I_{ref} = \frac{V_V \cdot V_{in} \cdot K_{Vin} \cdot K}{V_{RMS}^2} \tag{10.5}$$

- A - represents the error feedback signal of the voltage loop (V_V)
- B - gives information about the input voltage waveform $(V_{in}K_{V_{in}})$
- C - symbolizes the compensating signal $(1/V_{RMS}^2)$
- D - corresponds to the gain constant (K)

The real numbers shall be converted to the digital representation. The floating point representation is characterized by an excellent accuracy but a poor performance at high speed applications. However, the using of the floating point is not necessary. For the high speed applications which are not accuracy critical, the fixed point representation can be preferably used.

The fixed point representation of the real numbers typifies the using for time critical tasks as digital signal processing where the accuracy is less than speed. The principle is using

some bits in the integer for a representation of the fraction of real numbers. In this case, the each signal is standardized so that the maximal value is 1 [49].

- $I_{ref,max} = 1$ at the maximal power and low line
- $V_{V,max} = 1$ at the maximal output voltage

The following equations are created by an inserting of the norm values into the original equation. The low line is represented by $V_{pk(min)}$.

$$K = I_{ref,max} \frac{V_{RMS(min)^2}}{V_{pk(min)} \cdot K_{Vin} \cdot V_{V,max}} = \frac{V_{RMS(min)}^2}{V_{pk(min)} \cdot K_{Vin}} \tag{10.6}$$

For the sinusoidal input voltage the next equations are valid.

$$V_{RMS} = \frac{V_{pk}}{\sqrt{2}} \tag{10.7}$$

$$V_{RMS(min)}^2 = \frac{V_{pk(min)}^2}{2} \tag{10.8}$$

$$K = \frac{K_{Vin}^2 \cdot \frac{V_{pk(min)}^2}{2}}{V_{pk(min)} \cdot K_{Vin}} = 0.5 \cdot K_{Vin} \cdot V_{pk(min)} \tag{10.9}$$

A sensing of the input voltage uses a differential measurement, in other word, it is measured by two separate ADC channels. The differential measurement is necessary due to the ground reference which is placed at the negative terminal of the capacitor. After that, the signal rectification is carried out in the firmware. The final value is brought to the one input of the multiplier. It gives information about a waveform shape of the input voltage [49].

As next step, the root mean square value is calculated. The root mean square value is defined by the equation (10.10). In the discrete case, it is modified to the equation (10.11) [49].

$$V_{RMS}^2 = \frac{1}{T_{ac}} \int V(t)^2 dt \tag{10.10}$$

$$V_{RMS}^2 = \frac{\sum V(n)^2}{N} \tag{10.11}$$

The flow diagram 10.6 shows a software implementation of this equation. At first, a calculation is carried out. After that, the positive flag is tested. The voltage is accumulated. It means that the actual voltage is summed with results during previous cycles. Simultaneously, the cycle counter is incremented. Finally, the accumulated value is divided by a number of the cycles [49].

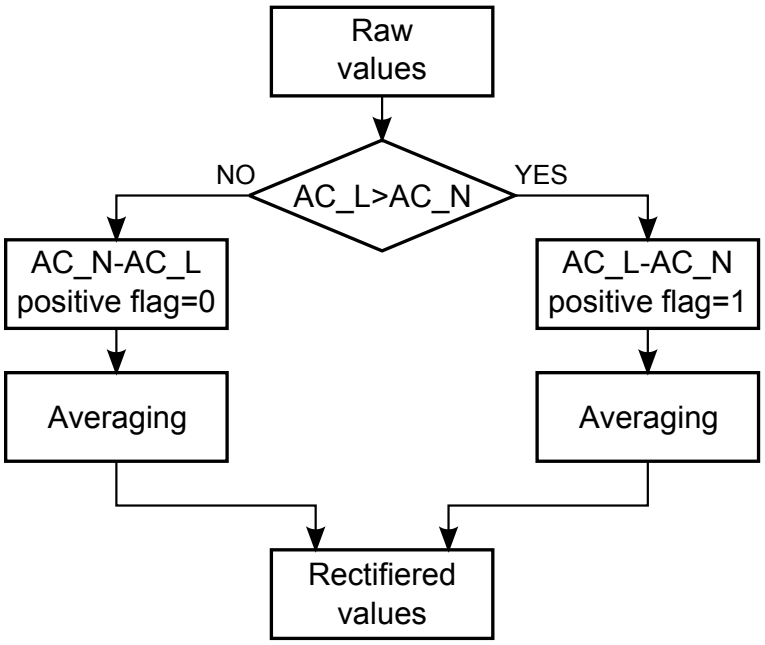


Fig. 10.5 Conditioning and rectification flow diagram.

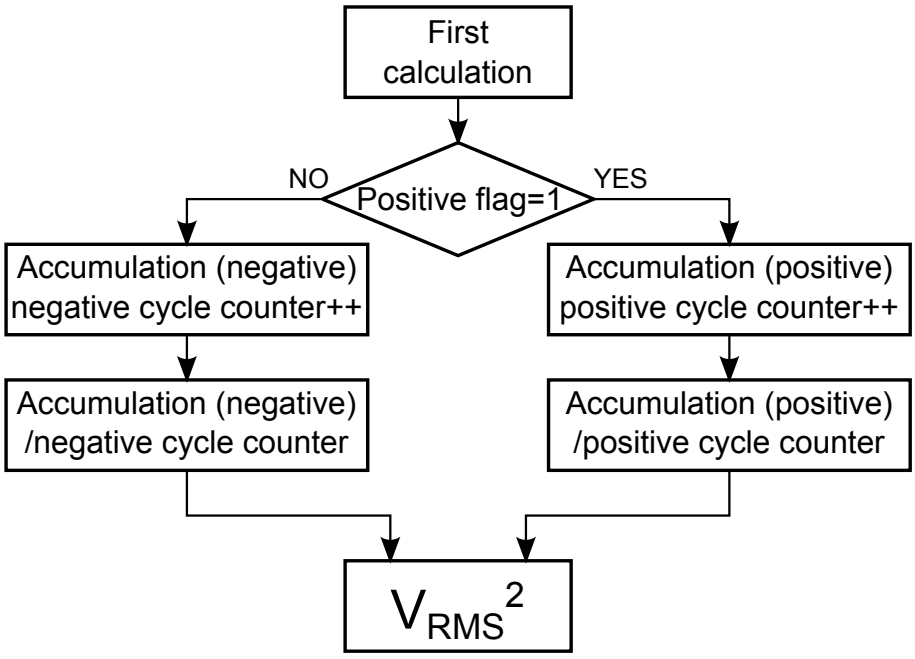


Fig. 10.6 Flow diagram of $VRMS^2$ calculation.

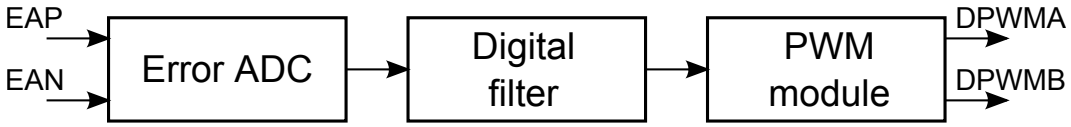


Fig. 10.7 Block diagram of the digital power peripherals.

10.9 Digital Power Peripherals

*UCD*3138 microcontroller takes advantages of digital power peripheral modules. This feature makes an easier design of power converters. Therefore this microcontroller is suitable for a digital control of PFC and other power topologies. This microcontroller includes three digital power peripheral modules. Each module contains an error ADC, digital filter, and digital PWM module. The modules can be interconnected between each other. In other words, any EADC can be connected to any digital filter and any digital filter can be connected to any PWM module [49].

10.10 Error Analog to Digital Converter Modules

EADC contains a differential analog amplifier at the input, which compares two signals connected to *EAN* and *EAP* inputs. The error amplifier output gives information about a difference between the current reference connected to *EAP* (positive terminal) and the feedback signal which is connected to *EAN* (negative terminal). Its gain is programmable by the block AFE_{gain}. The output is coupled with a next differential amplifier. This amplifier compares the error signal with the analog output from DAC.

It is a part of the successive approximation ADC as well as the 6-bit ADC. In other words, this amplifier provides a feedback between digital output from EADC and the analog error signal. EADC comprises other functional blocks for a power supply design simplification. The ramp block allows to create a ramp up or down function which can be used for a soft-start or soft-stop of converters.

If a bias is needed, the pre-bias control block will solve it easily. The module supports also a peak current detection which is provided by a comparator between the DAC output and *EAP* terminal. EADC offers also an averaging function, it can be used for a filtering of samples. The configuration allows to set $1x$, $2x$, $4x$, or $8x$ averaging, that means the output signal is average of the 1, 2, 4, or 8 samples [49].

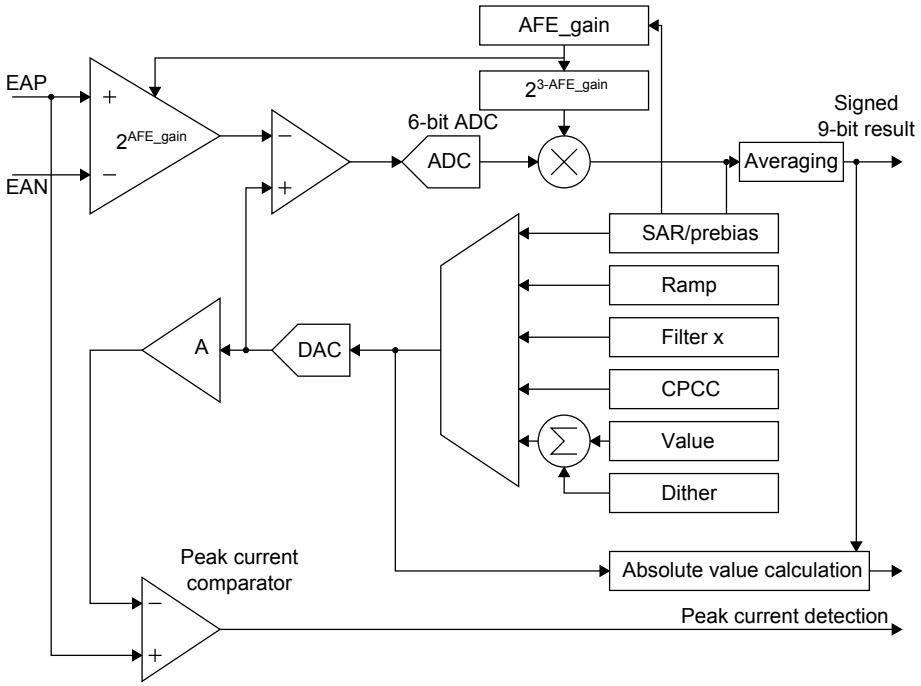


Fig. 10.8 Block diagram of the error analog to digital converter.

10.11 Digital Filter Modules

The digital filter is a second stage of the digital power peripheral modules. It contains proportional, integral, and differential branches. The filter is a complex system therefore it is not be described here in detail. The configuration of theses filters includes to configure a lots of registers. The filter allows to set all constants and gains. The configuration can provide a 2-pole and 2-zero digital compensator. The integral and differential branches contain also clams which protect an exceeding of the overflow limit. The proportional branch is limited by itself owing to it has no memory. The output signal is also clamped [55], [49].

10.12 Digital Pulse Width Modulation Modules

The last block of the digital power peripheral modules provides a PWM generation system. The compensated signal is connected to the PWM input. The PWM block has two outputs which control external power drivers. Finally, these drivers feed the power transistors. Output signals can be configured by several ways.

Each mode is suitable for a specific converter type. Configuration registers allow to set a large number of the functions (start events for a frame, generating signals, a synchronization

between channels, various fault actions, etc.). Additionally, the PWM modules offer a current balancing which can be preferably used for interleaved PFCs.

A normal operation mode is suitable for a single boost PFCs. A pulse width depends on the output signal from the digital filter. Sync FET Ramp and IDE Calculation modes provide a replacing diode rectifier by the MOSFETs. These improvements can improve the efficiency of PFCs by $1-2\%$. This mode is also useful for a synchronous boost single- or multi-phase PFCs, which should successfully improve an efficiency of correctors [49].

10.13 Over Voltage Protection

For safety reasons it shall be implemented an over voltage protection which protects the output capacitor against to a voltage overloading. As a consequence, it protects the other components owing to the interdependences between the output voltage and the input current. Two over voltage protection approaches provide a safety in two voltage thresholds.

The lower threshold is served by a full software solution. The output voltage is measured and filtered by ADC. The filtration is recommended for the noise and spikes immunity. The output of ADC is compared with an user programmable threshold. If this value is greater than the threshold, the corrector gets to shut down but the output voltage is further measured via ADC. It allows to turn on the PFC when the output voltage drops below the threshold due to this mode is called "hiccup". This mode is helpful when the operation conditions are changed by sudden load transient effects.

The hardware protection serves a higher threshold, which is faster than software approach therefore it is used for a protection against the hardware failure. A programmable on-chip analog comparator provides the fast and program independent solution. The threshold is determined in the configuration. It is chosen between $10-20$ volts above the software protection threshold. When this fast over voltage protection is once triggered, the PFC signal for power transistor is turned off. PFC is shutted down and latch for safety reason owing to the cause for the triggering which is most likely a serious hardware failure [49].

10.14 Cycle-by-cycle over Current Protection

An over current protection is implemented by an on-chip analog comparator as well as the fast over voltage protection. The protection is characterized by a cycle-by-cycle operation. That means, if the comparator is triggered during an one switching cycle, the PWM generation stops until the next cycle begins. In other words, the comparator undertakes continuously a testing of the over current during each switching cycle [49].

10.15 Graphical User Interface GUI

The graphical user interface developed by Texas Instruments is used for setting, monitoring and tuning of PFCs. Each process can be run on the fly. USB and PMbus are used for a communication between the personal computer and PFC. USB provides the communication interface between the personal computer and a USB to GPIO adapter. This adapter communicates with PFC through PMbus. GUI supports several PFC and other power converter topologies. [49].

10.16 Further Improvements

This section shows a possible improvements of the correctors. They includes a basic explanation of the issue and its solution. All of them have a direct impact on the performance. A burst mode is usually applied also in the analog control circuits. A frequency dithering is common used technique for EMI reduction.

10.16.1 Burst Mode

The most of PFCs have a poor correction performance at light load. It is caused by a precision of the current measurement. As a consequence, PFCs have inaccurate information about a waveform shape of the input current. Additionally, an efficiency is very low at light load due to the fact that the switching losses are same. The switching losses create a big amount of the total losses. The solution is a burst mode which is one or more dead time line periods after one normal operation line period. This technique get bigger input current. It provides a better current measurement, on the other hand it causes an enhances output voltage ripple [48], [49], [48].

10.16.2 X-cap Reactive Current Compensation

Generally, EMI filters shall be added into PFCs for a noise reduction. The EMI filters include in most cases two inductors for common and differential noise reduction, two Y-capacitors for differential noise reduction, and two X-capacitors for common noise reduction. The X-capacitors are connected between a power line (line or neutral) and earth terminal. These capacitors cause that the input current to lead the input voltage.

As a result, the power factor (PF) is negatively affected by this situation which plays a crucial role at light load or high line. This problem can be solved by a delaying of the inductor current so that the input current agrees with the input voltage. The delay can be

provided by a modification of the reference current signal for the feed forward current loop [55], [46].

10.16.3 Harmonic Injection

This method eliminates a second harmonic which shall be eliminated close to zero due to negative influences on telecommunications or other systems. The reference signal is sinusoidal in a case of conventional control techniques. The harmonic injection method applies a modification of the reference which is not sinusoidal. The signal has a flattened or concave top thus it reaches the elimination of the second harmonic. As a result, the input current spectrum does not include harmful harmonics. Conversely, other harmonics are enhanced. This method is suitable for higher power levels and applications which are sensitive to the one specific harmful harmonic [49], [47].

10.16.4 Valley Switching Control

A conventional control works under CCM properly at normal operation but at light load operates under DCM. Its weakness is the input current distortion. When a transistor is switched on, the line current goes up. After than, the transistor is switched off and the current drops back to zero at ideal situation.

The real situation is different. When the current crosses a zero voltage level, it continues to a negative region. This behaviour is caused by a resonating of the inductor current with MOSFETs parasitic capacitive current. The resonant current causes a significant distortion of the input current waveform. Since the resonant current is added to a switching current in a one switching cycle and subtracted from the switching current in the next cycle.

As a result, it creates a crucial current steps on the input current waveform. This phenomena has substantially a higher frequency than the feed forward loop bandwidth. As a consequence, the feed forward loop is not capable regulating current disturbances.

The solution of these current disturbances is solved if the transistor is switched on after the resonant current matches zero. In this case, the input current will not be affected by the resonant current. As a consequence, the current distortion is effectively removed [50], [49].

10.16.5 Frequency Dithering

This method uses a modulation of the switching frequency for a EMI noise reduction. This technique improves a capability of the EMI filters or allows an using of lower quality filters. Unfortunately, the frequency dithering is hand in hand with THD performance. THD drops

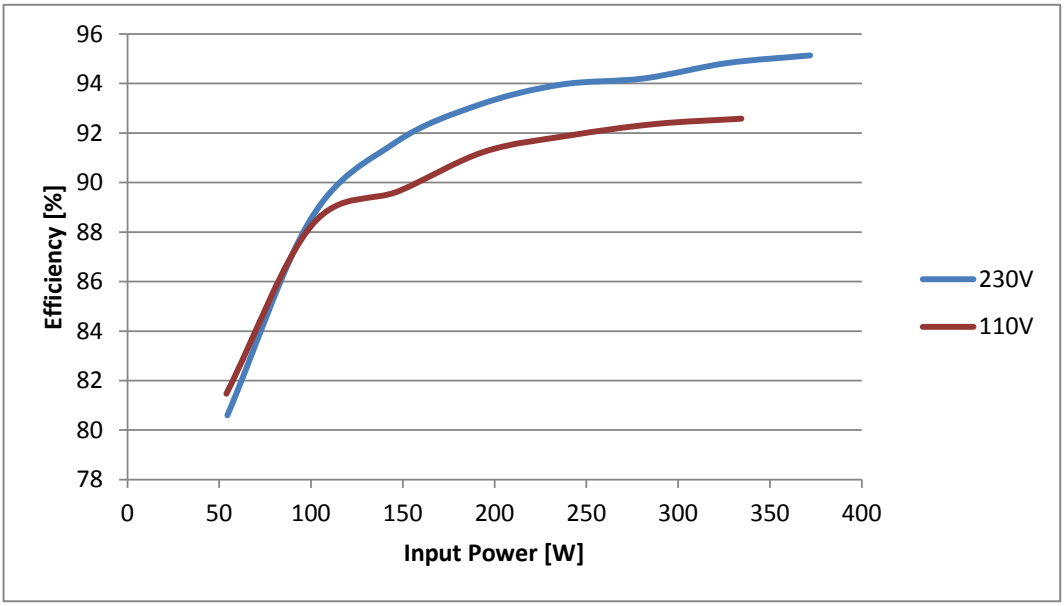
by 1% in average. A principle of the EMI reduction is based on the noise changing from narrowband to wideband.

The modulation signal has a triangular shape. An amplitude of the signal affects a dither magnitude. The dither magnitude defines the minimum and maximum switching frequency. The center of the switching frequency matches the nominal switching frequency of the PFC. The dither rate determines a frequency of the change between extremes (minimal and maximal frequencies). The dither rate equals to a frequency of the modulation signal. [49].

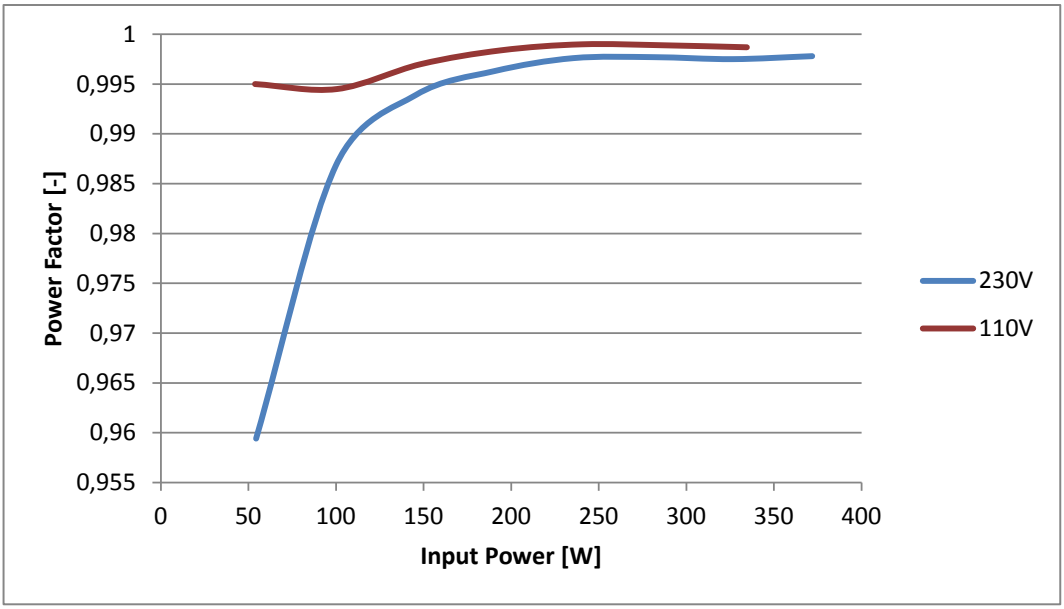
10.17 Experimental Results

10.17.1 Performance Measurement

The measurement was undertaken by the description in the section 6.5. The figure 10.9 a) depicts an efficiency of the corrector and correction performance. The efficiency exceeds 95.1% at 230V input voltage and 92.5% at 110V. The figure 10.9 b) represents a correction performance in a full operation range. The power factor at 50W input power reaches 0.95 in case of 230V line voltage and 0.995 in case of 110V line voltage. The PF peak at 110V reaches 0.999 at 240W. Whereas, the maximum at 230V line voltage is shifted to the 370W input power and reaches the 0.998 value.



(a)

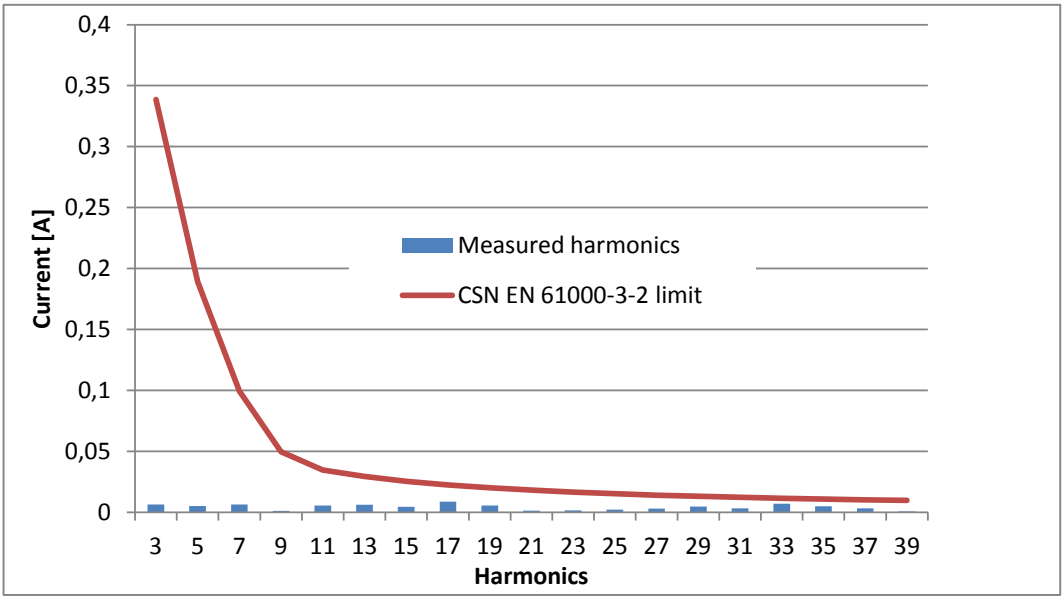


(b)

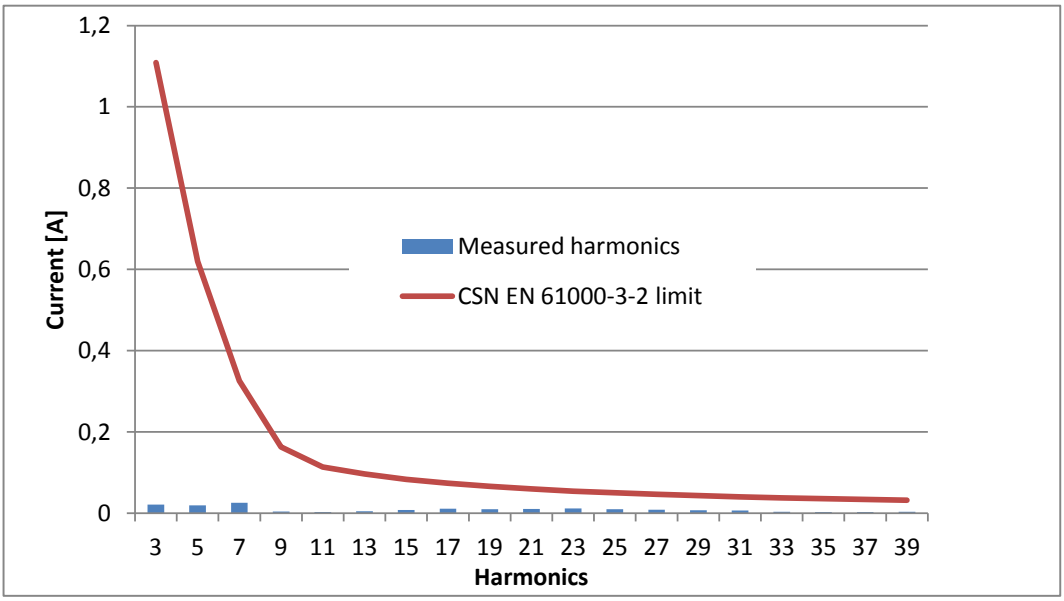
Fig. 10.9 Performance measurement of the corrector based on the UCD3138 controller a) efficiency, b) Power Factor.

10.17.2 Harmonic Content According to ČSN EN 61000-3-2 Standard

The corrector shall not overcome harmonic order limits for the line current. The measuring setup uses a same equipment and connection as the performance measurement. The obtained data describe a harmonic content at two input power values. The measurement was carried out at $100W$, and $300W$. The results are depicted in the figure 10.10. Both figures include a limit which respects the ČSN EN 61000-3-2 standard [42] for *D* class. For the graphs were used the more strict limit which is related to the current over the power (mA per W). The experimental results complies the limits which are defined according to the standard [42].



(a)



(b)

Fig. 10.10 Harmonics content of the corrector at different loads, a) 100W, b) 300W.

Chapter 11

Evaluation of the Prototypes

11.1 Experimental Results Comparison

This chapter is devoted to the overview of obtained experimental results. The measurement was performed in the four main parts which are performance measurements, harmonic content of the line current, conductive electromagnetic emission, and thermal measurement. The measured data of the first prototype is shown in the figure 7.24. Curves illustrate that the peak efficiency of the corrector is 96.6% at the $230V$ line voltage. The peak efficiency at $110V$ reaches 93.9%. The PF parameter is in the interval 0.95 to 0.998. If the results are compared with the data from second prototype with the $UCC28060$ controller. The efficiency peak reaches 95.5% at $230V$ and 92.5% at $110V$. These results reflect the power inductor construction and switching frequency of the corrector. On the other hand the efficiency curves are flat thanks to the power management. PF was during the whole measurement from 0.985 to 0.998. The experimental results of the corrector based on the $UCC28070$ controller indicate the maximal efficiency is 96.8% at $230V$ and 94.1% at $110V$. PF is in the range from 0.87 to 0.999. In case of the $UCD3138$ kit the efficiency reaches 95.2% at $230V$ and 92.6% at $110V$. The PF range is from 0.95 to 0.999. Summing up the results, it can be concluded that the performance of all correctors is sufficient, the best efficiency is reached at the corrector with $UCC28070$.

The measurement of the harmonic content indicates that the all prototypes pass the required standard. The graphs of the third prototype imply a higher content of the third harmonics at $100W$ load power. The better correction performance is observed at the higher load current. The prototype with digital controller demonstrates the main benefit which is a very low content of the higher harmonics at light load. These findings are also influenced by the determined output power of the correctors.

The conductive electromagnetic emission measurement verifies that the correctors comply the ČSN EN 61000-6-3 [43] or ČSN EN 61000-6-4 [44] standard. The final measurement was undertaken with the Schaffner FN2090-10-06 filter [40]. The first prototype with improvements complies the ČSN EN 61000-6-4 which is the industrial standard. The second prototype based on the *UCC*28060 should comply the industrial standard in the case of the direct grounding connection to the rack. Otherwise, this corrector does not comply this standard due to the highest frequencies overtake the limit. The prototype with the *UCC*28070 controller and additional improvements pass the limit according to the ČSN EN 61000-6-4 standard [44]. The commercial limit regarding the ČSN EN 61000-6-3 standard [43] was exceeded but it is expected that the more efficient grounding can solve this issue.

The thermographic measurement verifies the design of the power components. The investigation confirm that the temperature of the particular components does not exceed 80° only with one exception which is a NTC thermistor of the second prototype.

11.2 Corrector Costs Comparison

This section provides costs comparison of the prototypes. The figure 11.1 shows overall costs of each prototype. The *UCC*28180 corrector is a cheapest solution. Contrary, the *UCD*3138 is the most expensive member. It is caused due to this board was bought as a final kit. However, the power rating of the prototypes is differed therefore it is made up a second figure. The figure 11.2 respects the power rating of the correctors. The costs are tied to a unit of the power.

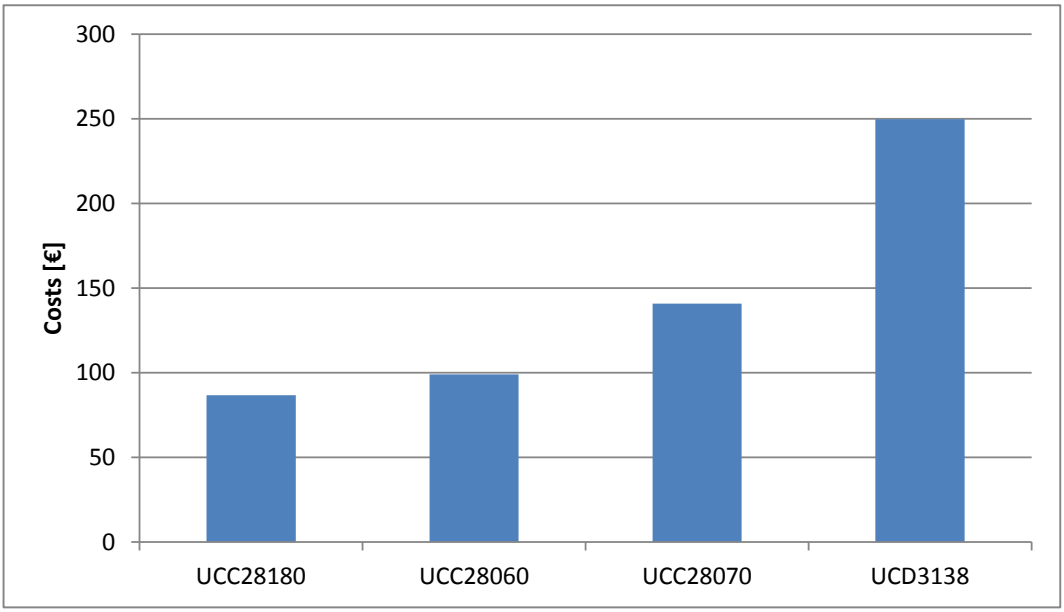


Fig. 11.1 Bar chart of the costs comparison.

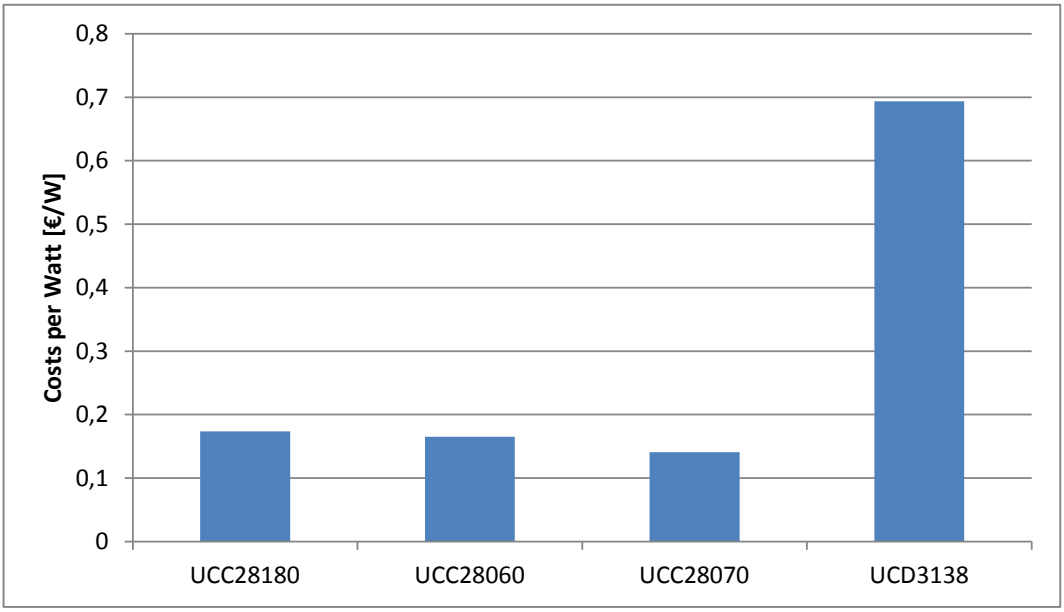


Fig. 11.2 Bar chart of the costs per watt comparison.

Chapter 12

Conclusion and Future Work

From the research that has been undertaken, it is possible to conclude that the experimental findings confirm expectations. All prototypes fulfilled the requirements which were established at the beginning of this thesis. The design methods used for prototypes provided a suitable approach with a direct practical relevance. The experimental results implied that the suggested techniques of APFCs provided a performance enhancement of the correctors. The theoretical background has contributed considerably as well due to it gives a comprehensive account of the power factor correction, physical principles, control techniques, current modes, and perspective corrector topologies which were directly linked with the final prototypes.

The most beneficial parts of this doctoral thesis are chapters devoted to design and verification which explain basic blocks of the controllers and describe a design process of the prototypes from the beginning. Each prototype takes one chapter about the design, improvements, and verification. Thank to this construction the dissertation covers a design complexity, cooling requirements, volume, PCB dimensions, component count, performance, and costs. All these aspects are taken into account in the discussion chapter which is devoted to the overall evaluation of the prototypes.

If we look at the design issue more closely, all prototypes are unique. Each prototype uses a different controller, topology, and output power rating. As a consequence, design calculations were performed individually.

The first prototype is based on the $UCC28180$ controller. The chapter explores a design process and consists of sections discussing about the possible improvements as well. These improvements were devoted to boost diodes replacement and frequency dithering. As a result, let's say that the SiC Schottky diodes are a suitable choice for correctors which operate over the $100kHz$ switching frequency. The advantages of these diodes are a lower power dissipation, smaller heatsink, very low junction capacitance. On the other hand, the cost is higher than the cost of the conventional solution with Si ultra fast diodes. During the

EMC testing was found out that the measured data overcomes the limit for the ČSN EN 61000-6-3 standard therefore the prototype was equipped by a relaxation oscillator which is able to sweep the switching frequency in the determined range. These improvements with other hardware adjusting as the switching frequency decreasing, gate resistor, and transistor replacement lead to the modification of the electromagnetic emissions results.

The next prototype is based on the $UCC28060$ controller. It is characterized by an unique flat construction which uses planar inductors, and embedded components. The solution provides a very low height of the prototype which is up to $22mm$. As a heatsinks of the power components were used copper polygons. They reduce the costs of the prototype. The most beneficial feature is the power management of the corrector. This solution opens a possibility of the using interleaved corrector in the application with the variable output power and line voltage. The experimental results indicate that the approach improves the efficiency and correction performance at light load. Contrary, for higher loads the corrector takes advantage of the interleaving.

The prototype based on the $UCC28070$ controller uses similar phase management control. The power management is not generally implemented in the controller. The feature is controlled by the superior control system. The control signals use an external transistors which provide a disabling function of a particular branch of the corrector. This feature of the controller is originally used for disabling of the corrector branch in case of a specific failure. The borders between enabling or disabling particular branch of the corrector is dependent on the line voltage and output power. The control signals allow to disable the corrector branches by grounding of the $CAOx$ pins. When the $CAOA$ pin is pulled low, the channel A is disabled. The experimental results show that the phase management optimizes the performance and efficiency under variable operation conditions. For a reduction of the electromagnetic emissions the corrector was adjusted. The switching time of the transistors was slowed down by an gate resistor increment. The inductors were equipped by a flux band. Finally, the switching frequency was reduced to $120kHz$ and the frequency dithering was also used.

The last APFC was characterized by $UCD3138$ controller which was bought as a kit. The corrector was used for evaluation purposes. The costs comparison across the correctors demonstrates that the most expensive solution is the kit with $UCD3138$. On the other hand, the distortion of the line current is considerably eliminated.

The future research will be devoted to use a FPGA as the PFC controller. The corrector will be designed as a six-phase corrector. The solution will use several internal or external ADCs. Based on this information FPGA will be able to control a power stage. The FPGA will produce six PWM signals which could be amplified by gate drivers. The main advantages

of this solution will be easy reconfiguration of the number of the phases, data logging, diagnostics, implementation of the phase management, and changeable control method. The disadvantages will be a longer developing time of the control algorithm, power amplification of the PWM signals, and costs.

The realized prototypes of the correctors can be practically applied as pre-converters of the conventional switch mode power supplies. They can be successfully used for a number of industry power supply applications. From the outcome of the investigation it is possible to conclude that the decision about a suitable topology and controller is a complex issue. However, single phase correctors are a suitable choice for the stable operational conditions. The digital controllers open an accurate correction of the line current. Unfortunately, their application is expensive and the implementation time is long. The interleaved correctors are flexible. They can works under single phase or interleaved operation according to the instantaneous conditions. Thanks to this feature they can operates always optimally.

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Appendix A

Appendix

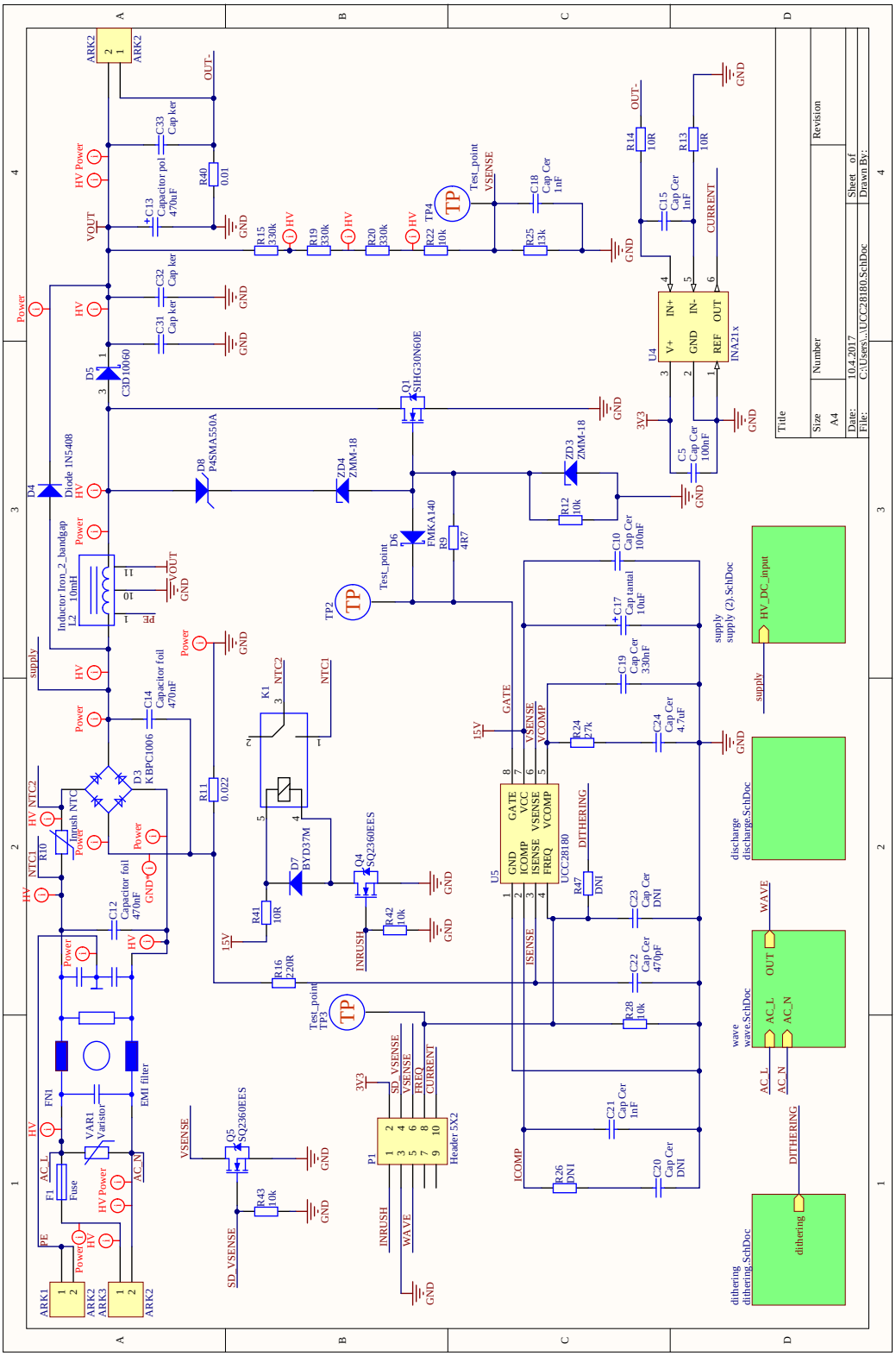

Fig. A.1 Schematic diagram of the single phase boost corrector with the UCC28180 controller.

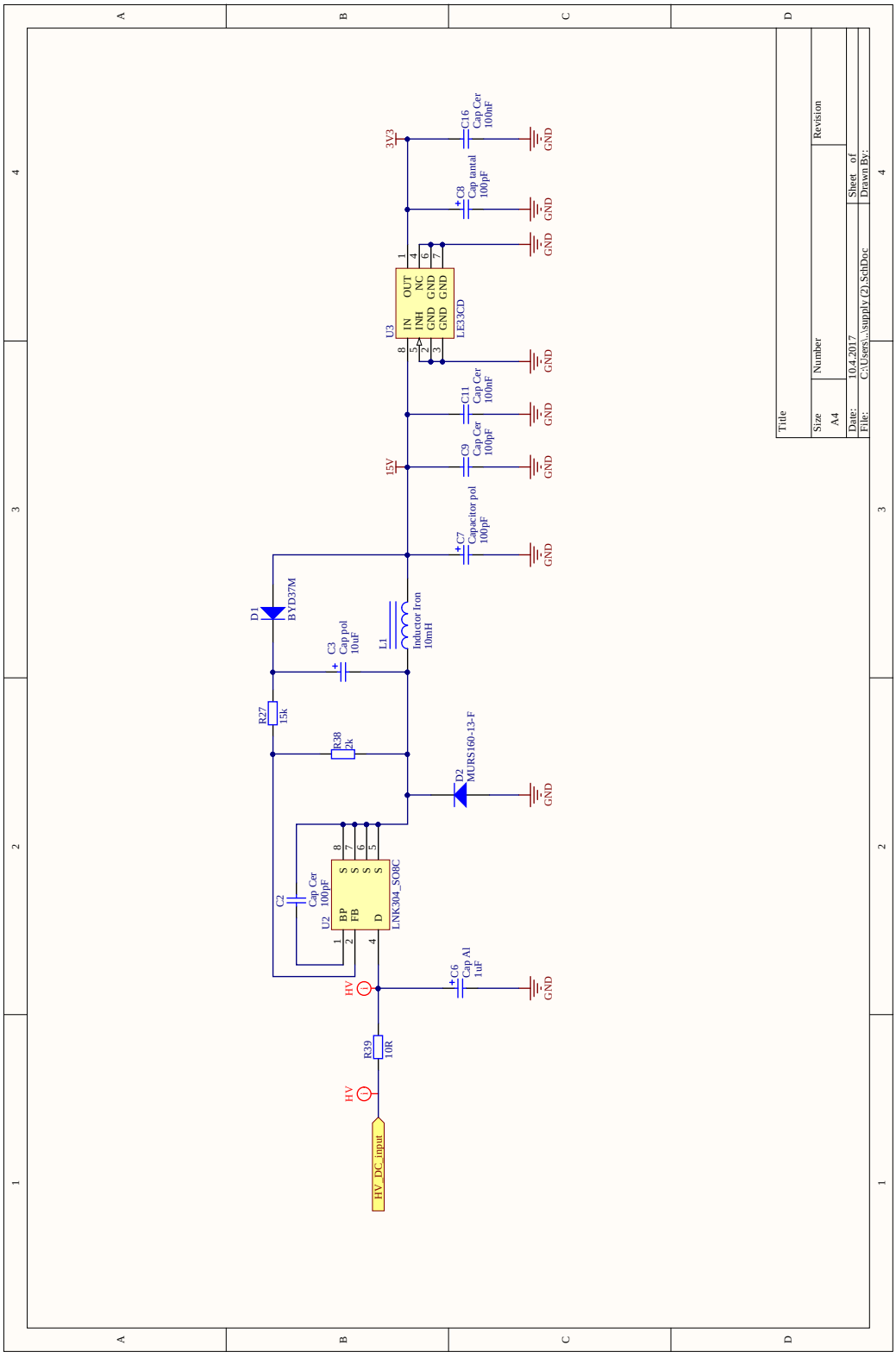

Fig. A.2 Schematic diagram of a supply for the single phase corrector (UCC28180).

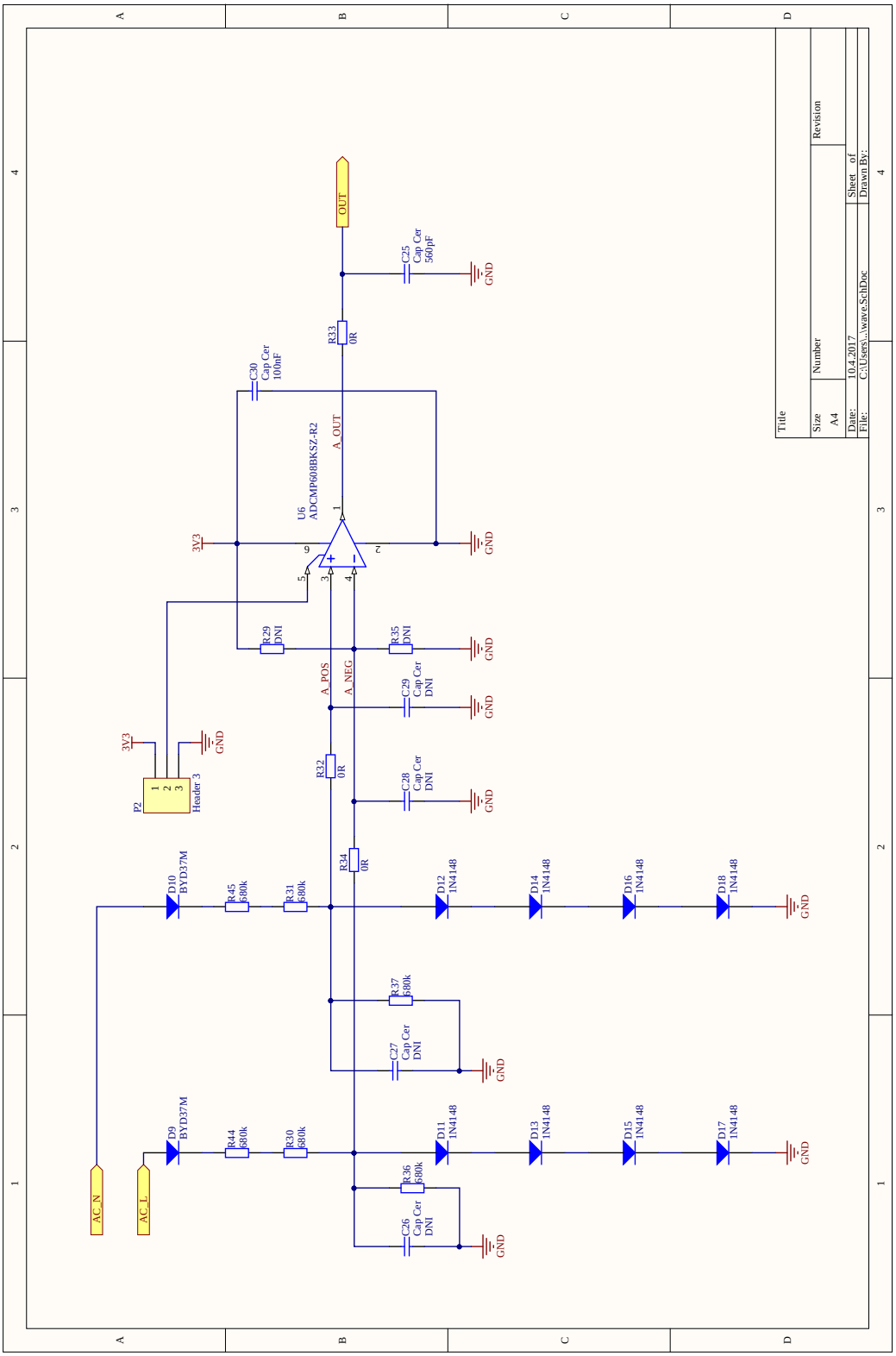

Fig. A.3 Schematic diagram of the positive wave detector (UCC28180).

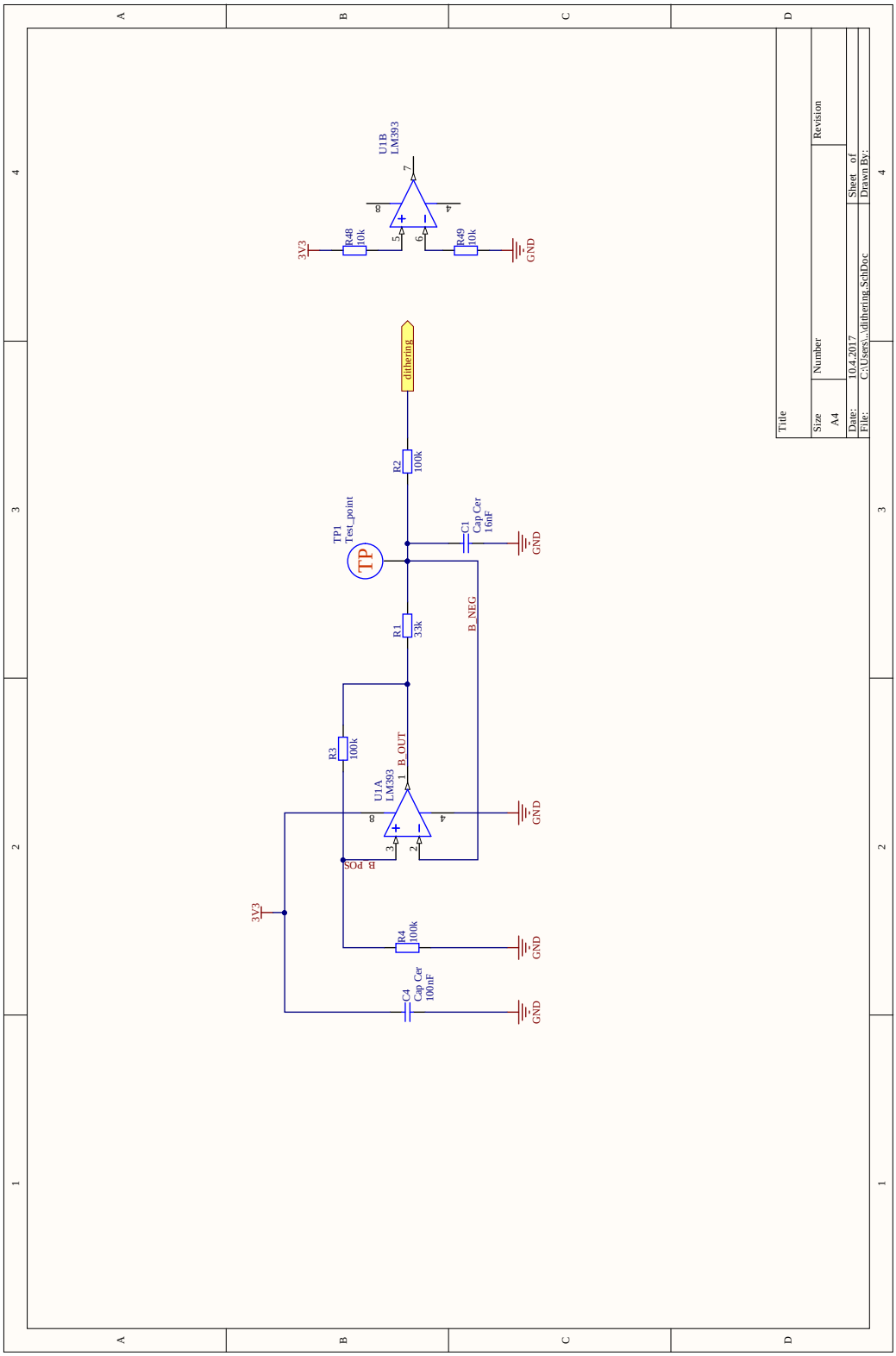

Fig. A.4 Schematic diagram of the dithering circuitry (UCC28180).

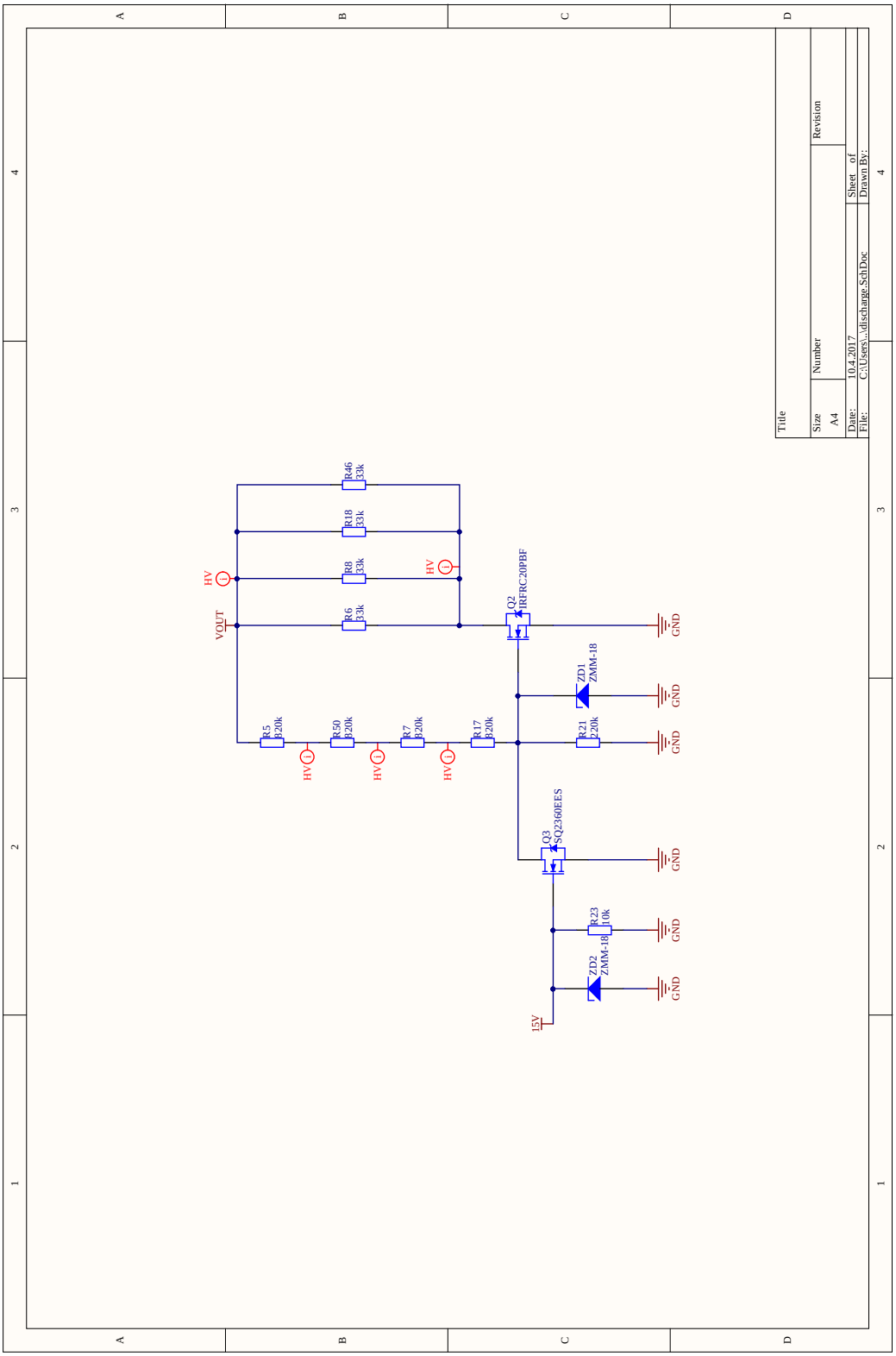

Fig. A.5 Schematic diagram of the bulk capacitor discharge circuitry (UCC28180).

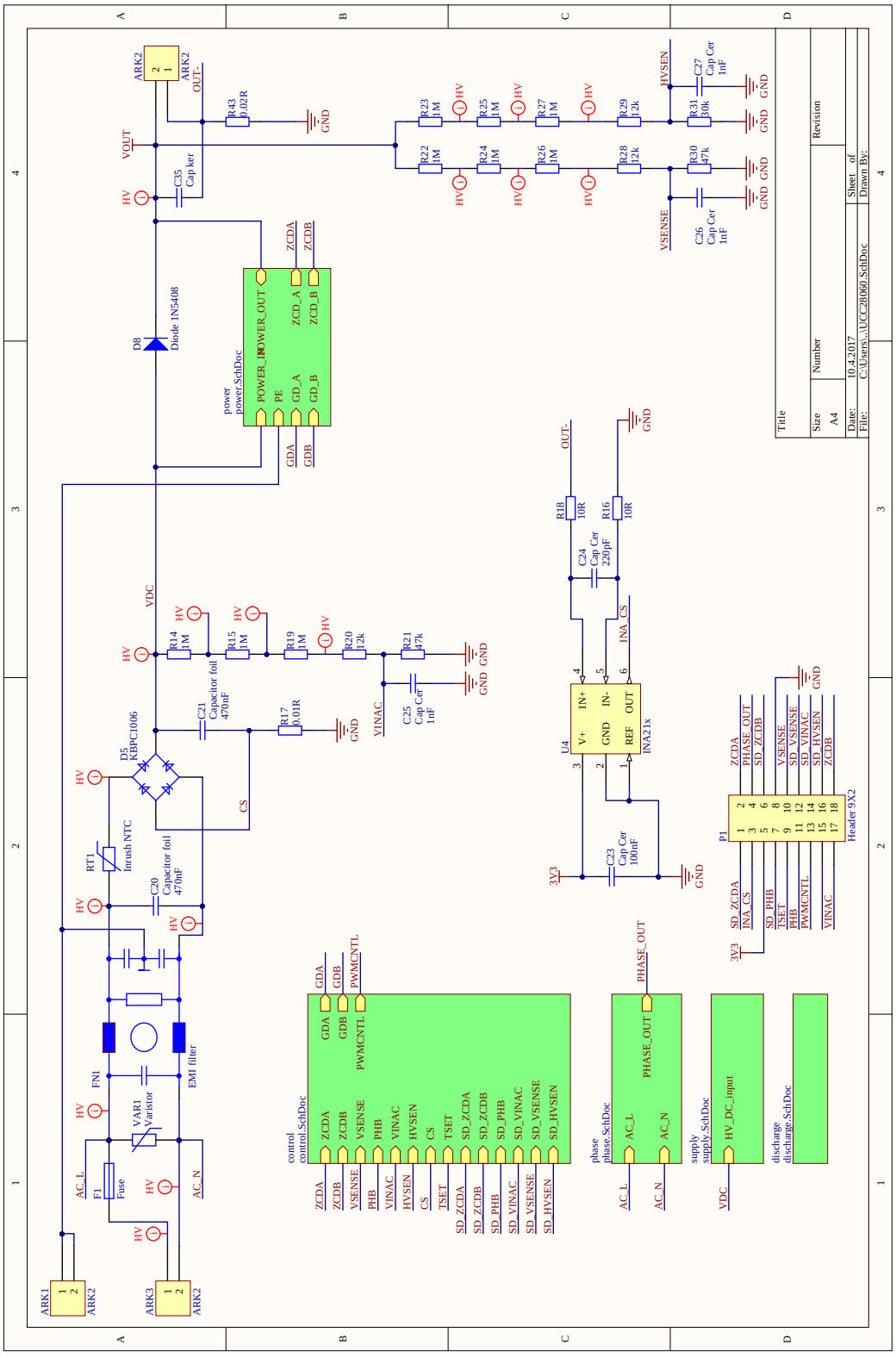

Fig. A.6 Schematic diagram of the interleaved dual phase corrector power stage based on the UCC28060 controller.

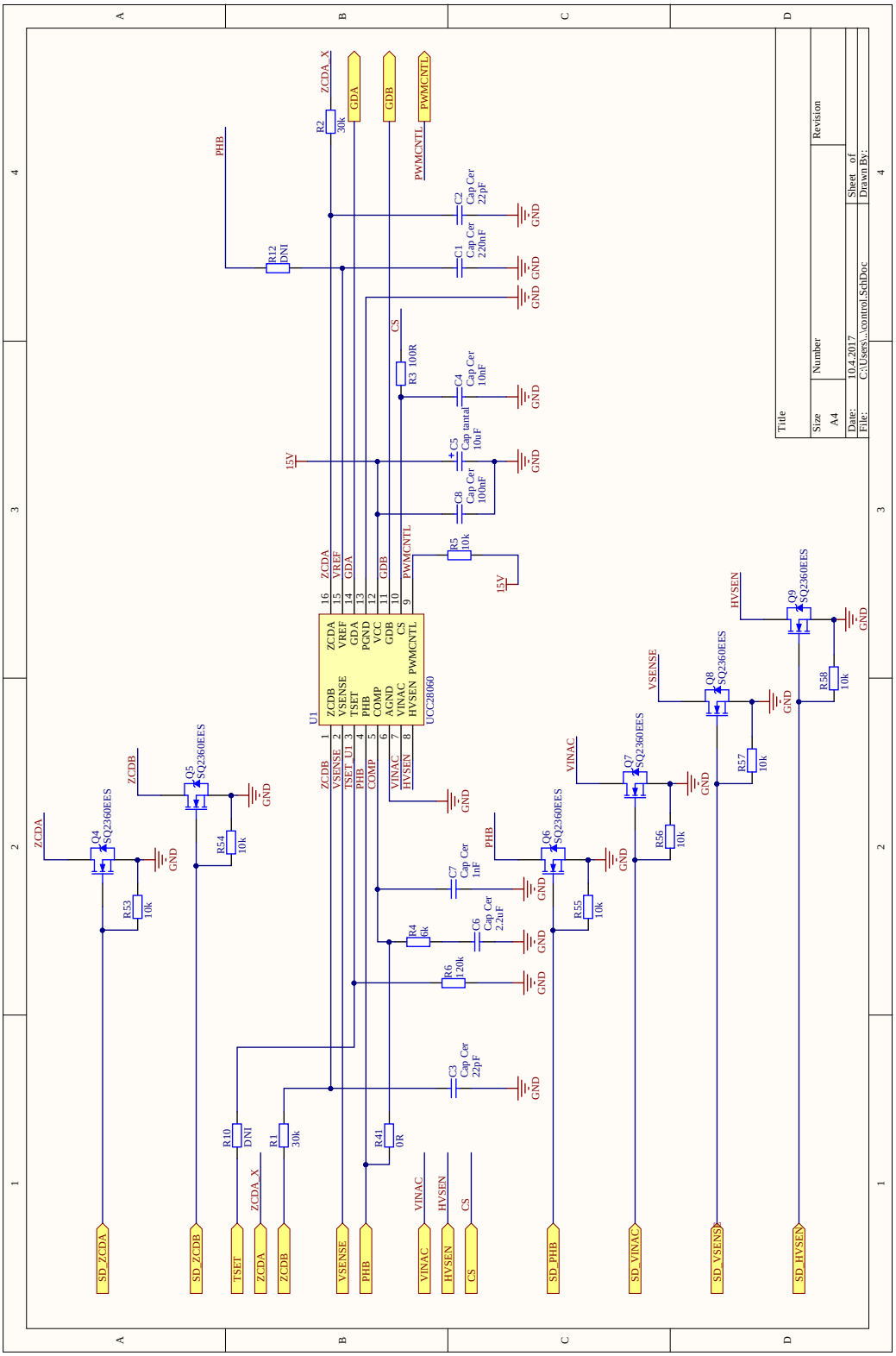

Fig. A.7 Schematic diagram of the control circuitry with UCC28060 controller.

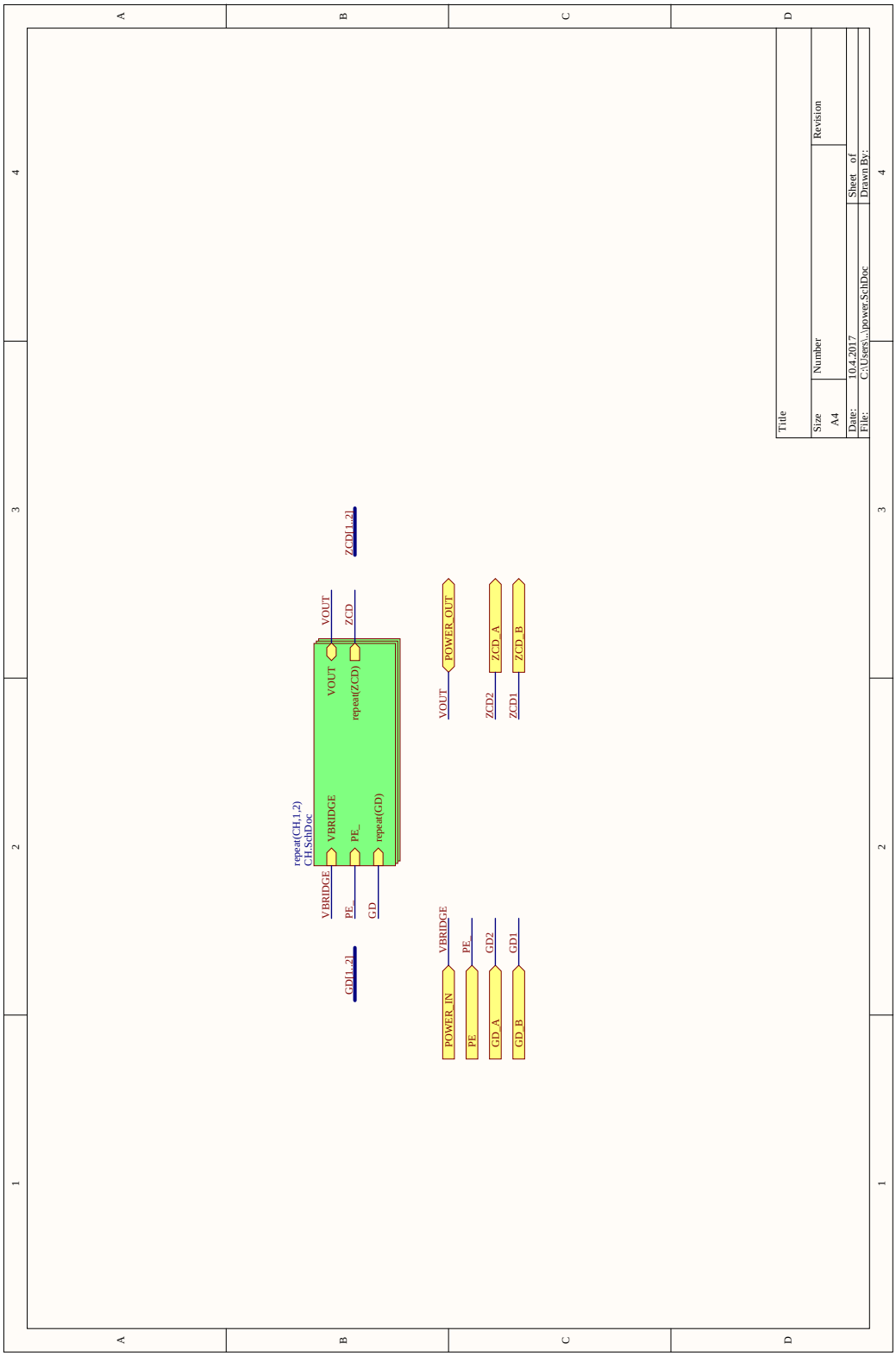

Fig. A.8 Block diagram of the power channel (UCC28060).

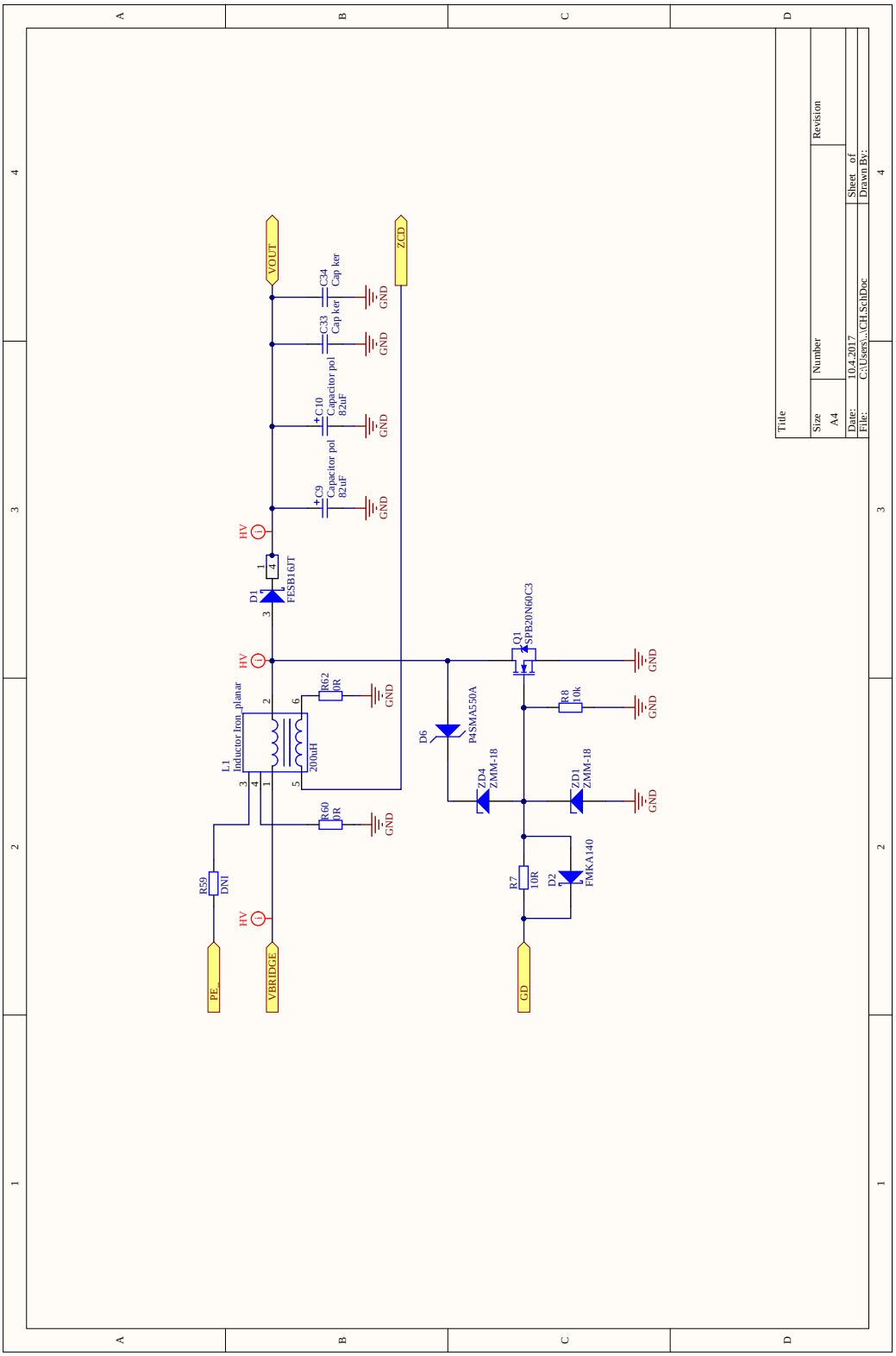

Fig. A.9 Schematic diagram of the power channel (UCC28060).

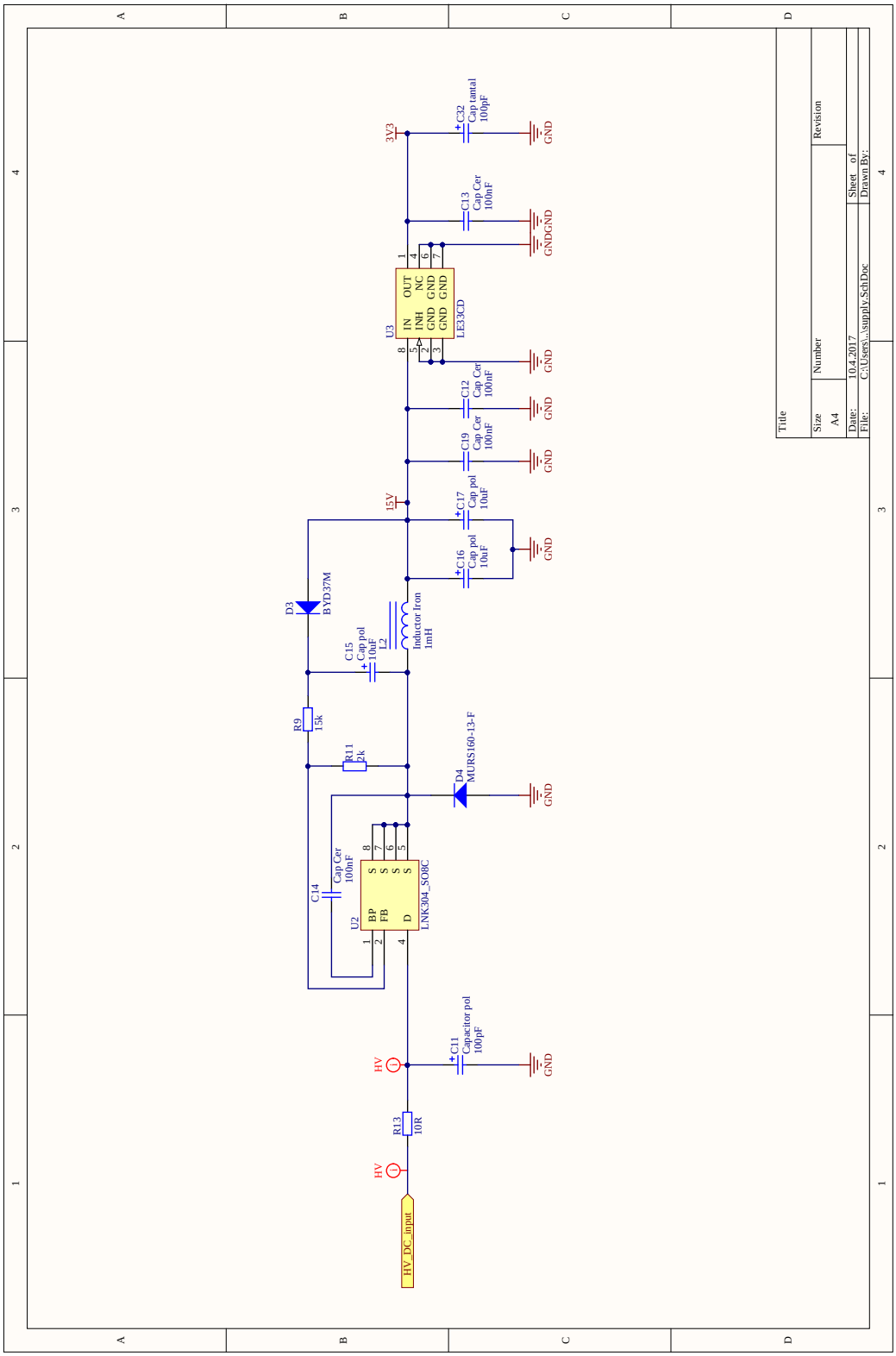

Fig. A.10 Schematic diagram of the power supply for the interleaved corrector (UCC28060).

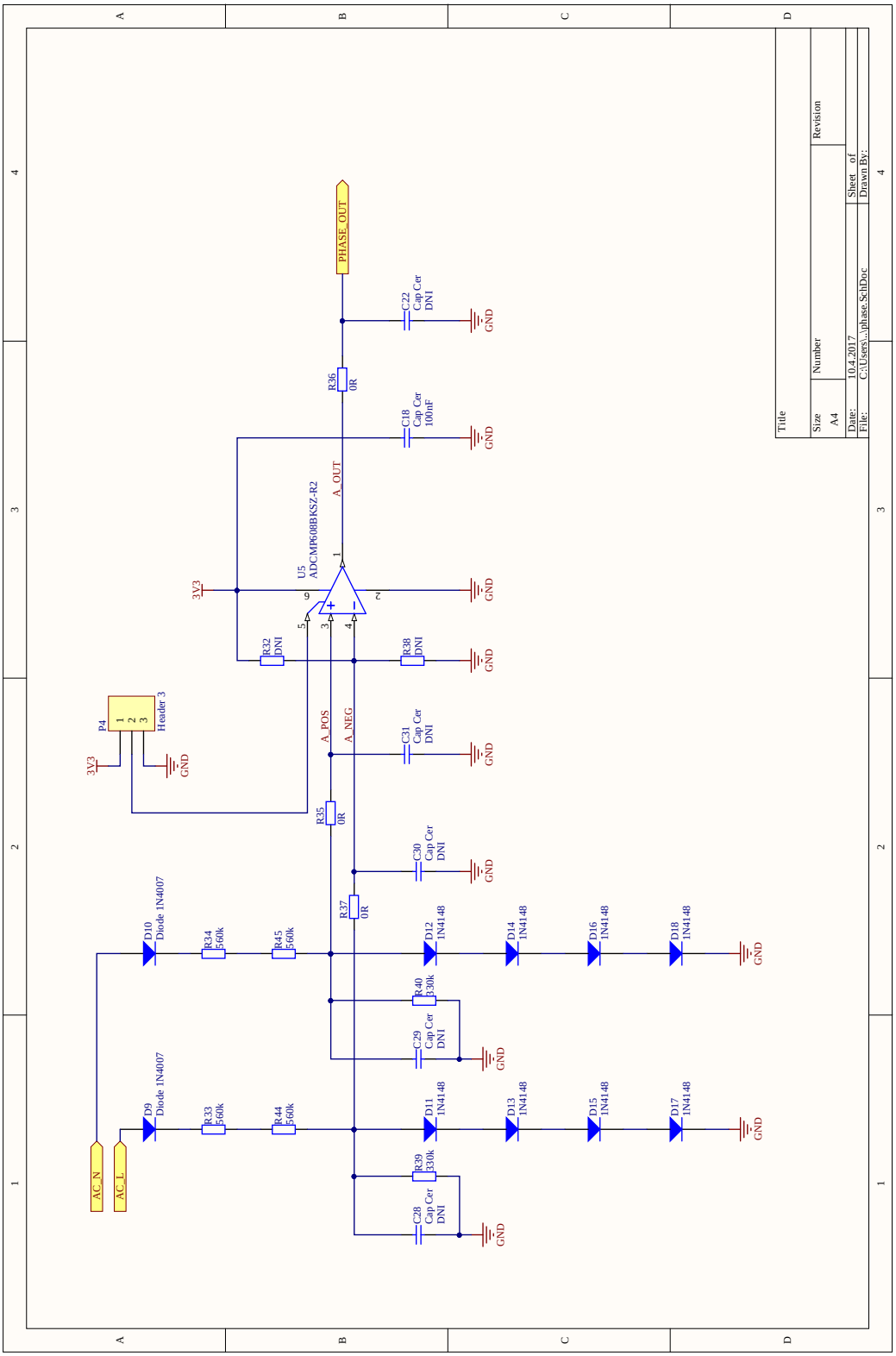

Fig. A.11 Schematic diagram of the positive wave detector (UCC28060).

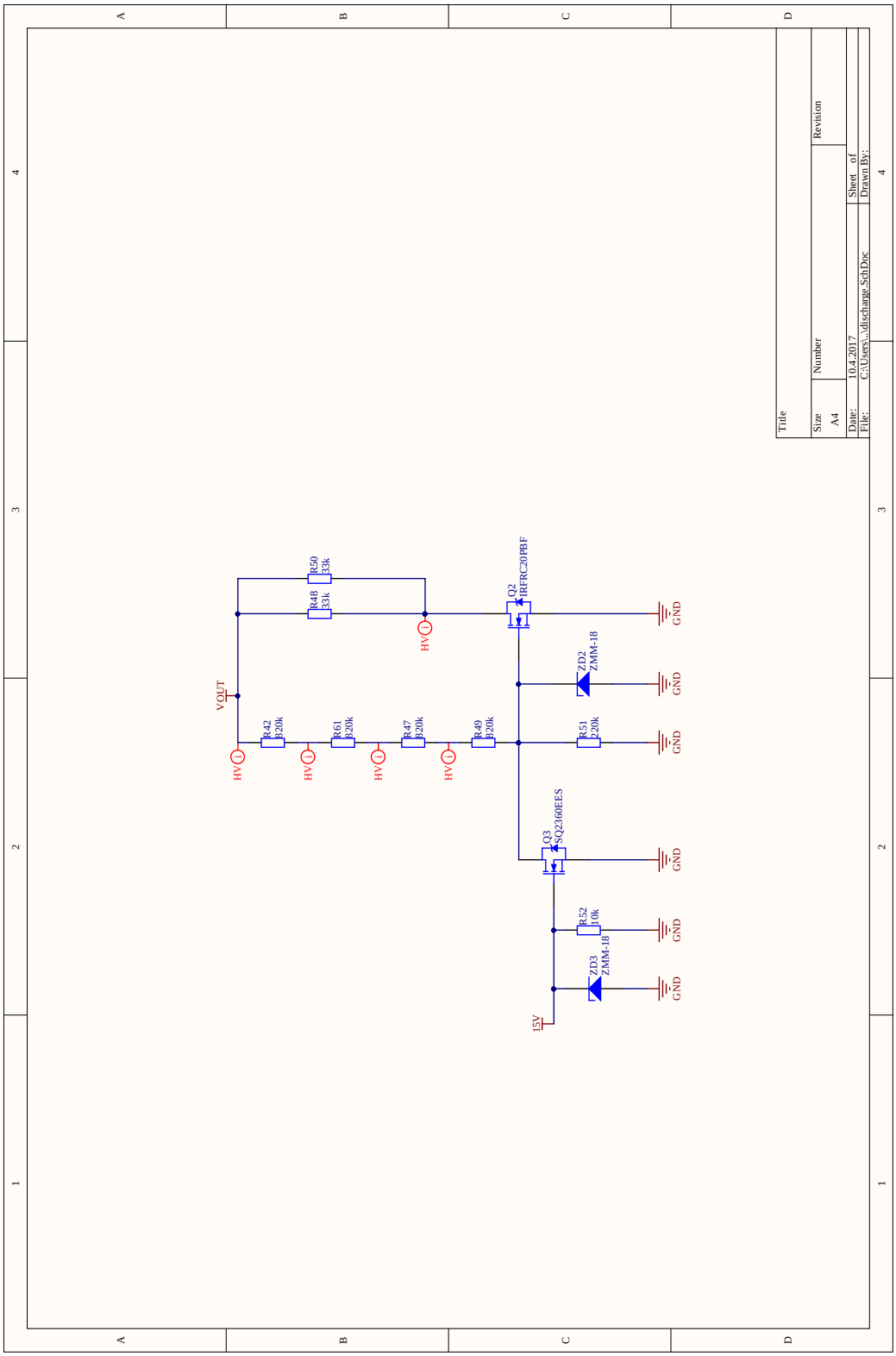

Fig. A.12 Schematic diagram of the bulk capacitor discharge circuitry (UCC28060).

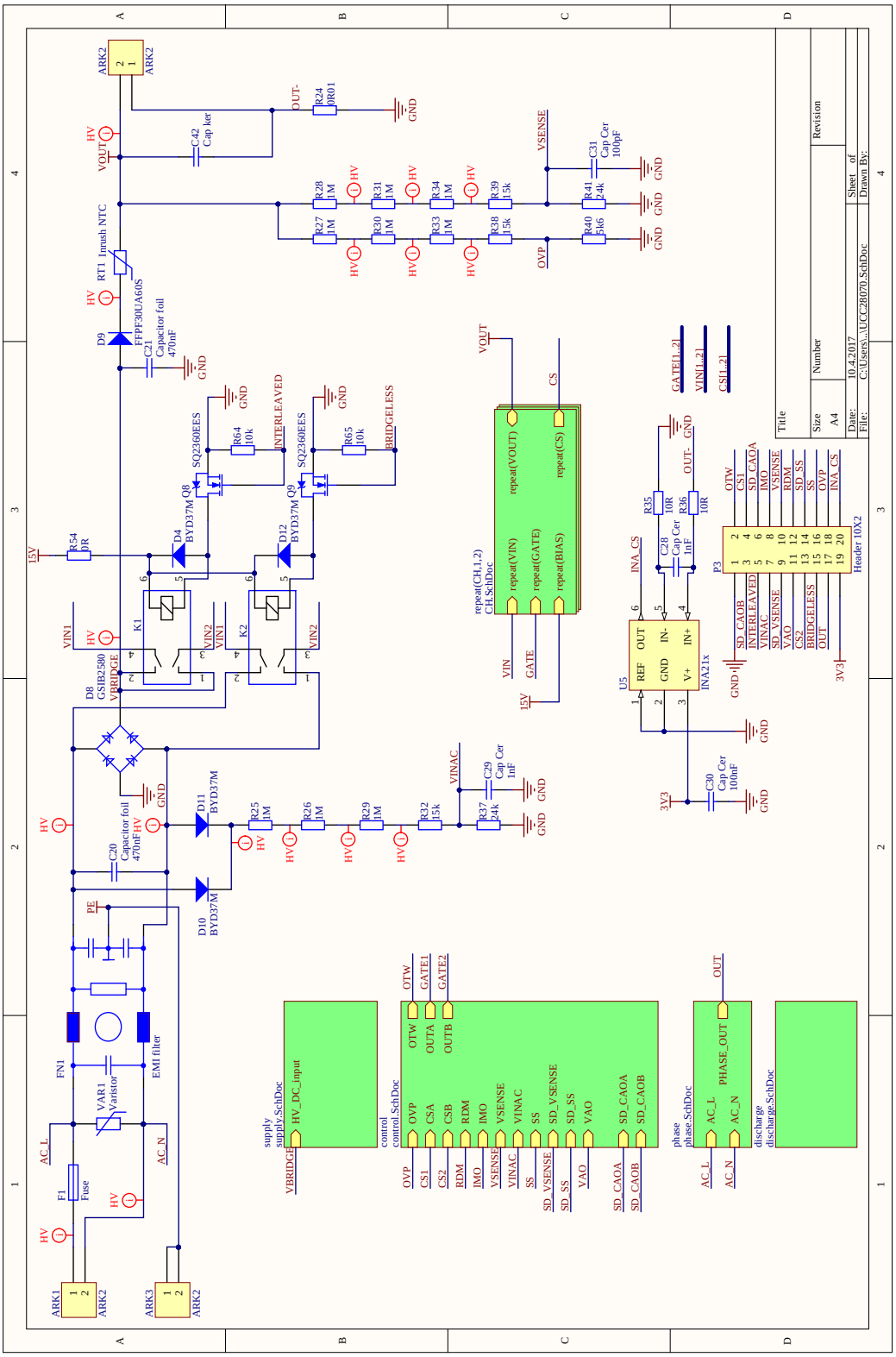

Fig. A.13 Schematic diagram of the interleaved dual phase corrector power stage based on the UCC28070 controller.

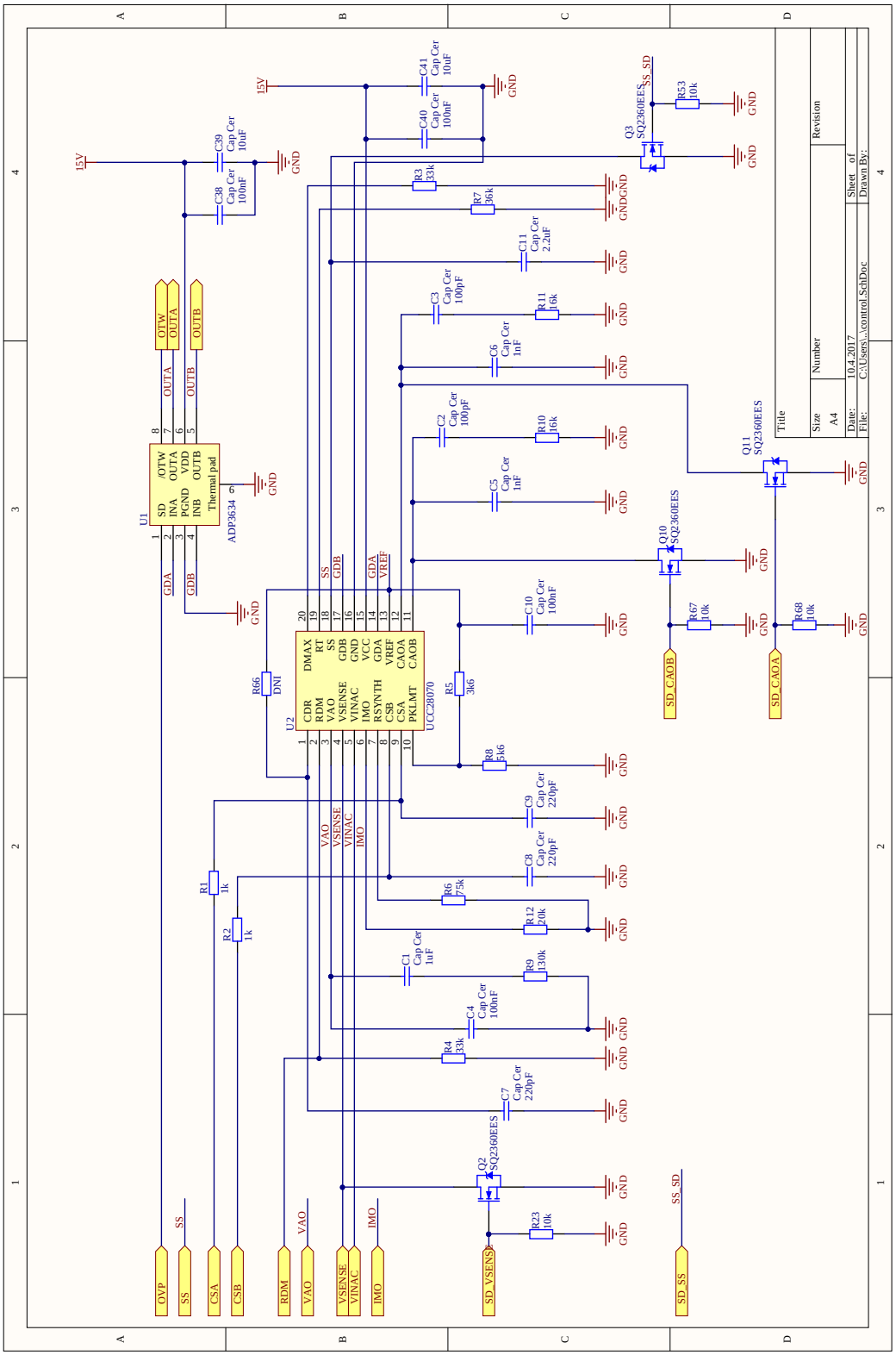

Fig. A.14 Schematic diagram of the control circuitry with the UCC28070 controller.

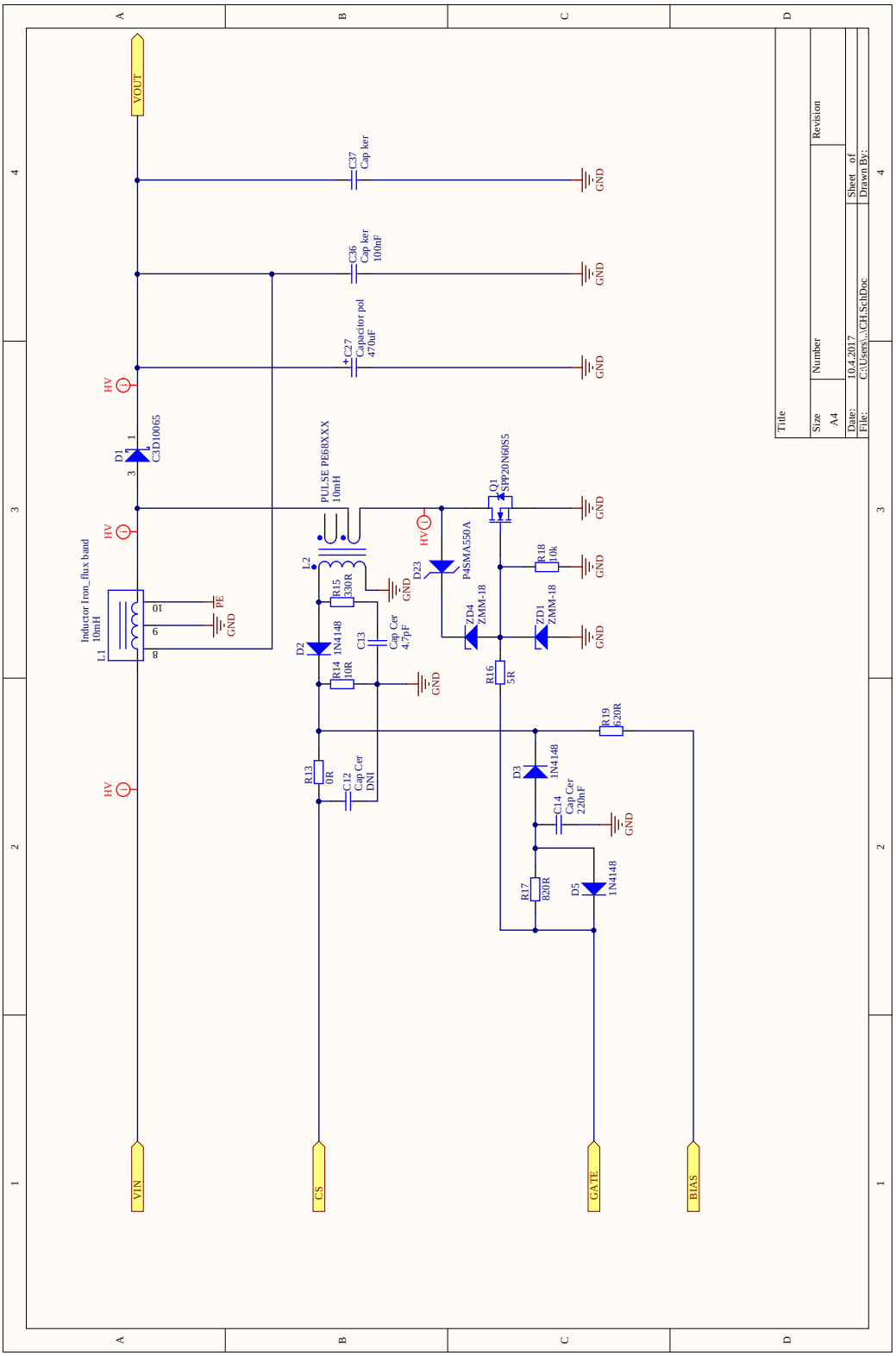

Fig. A.15 Schematic diagram of the power channel (UCC28070).

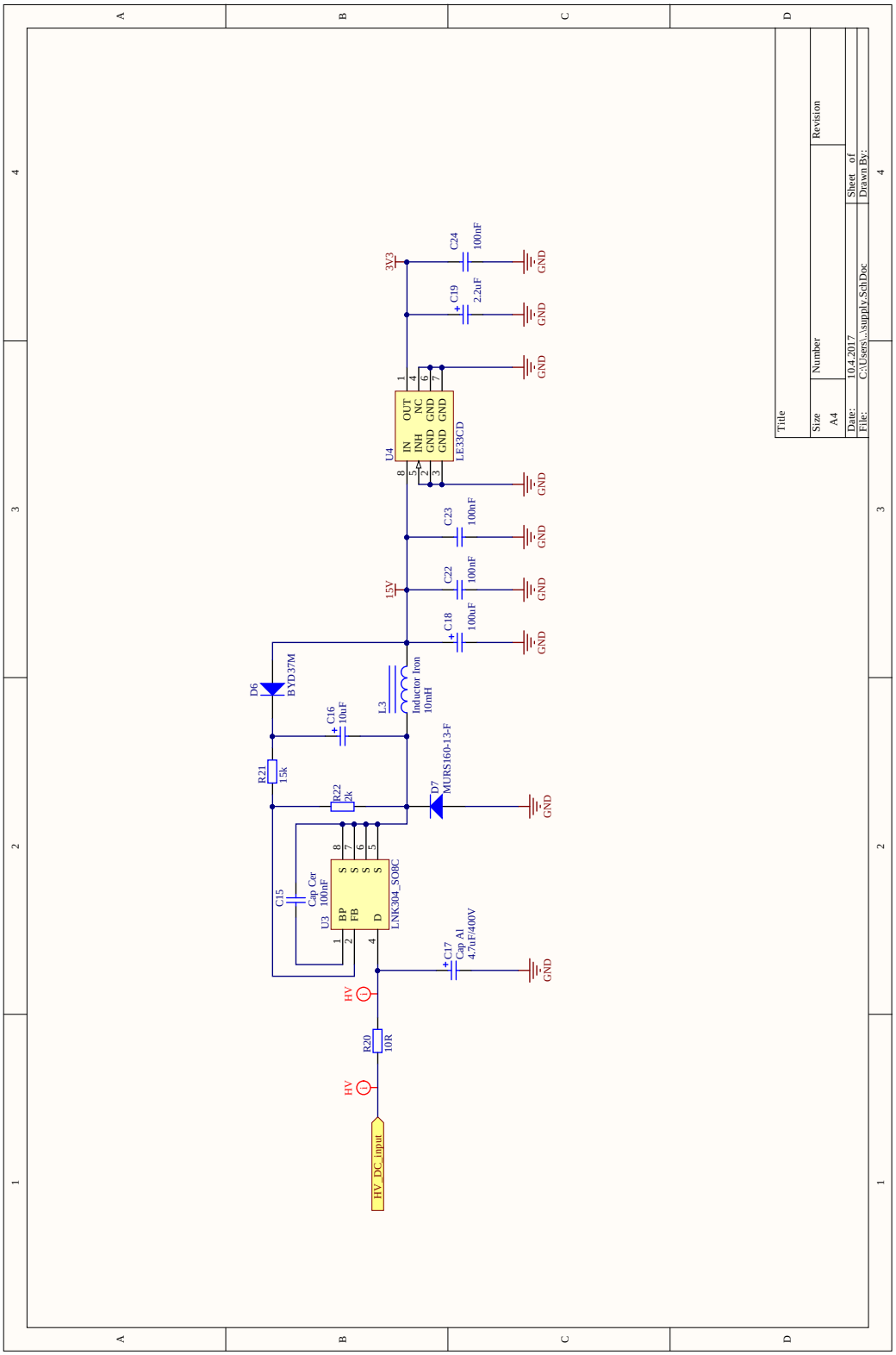

Fig. A.16 Schematic diagram of the power supply (UCC28070).

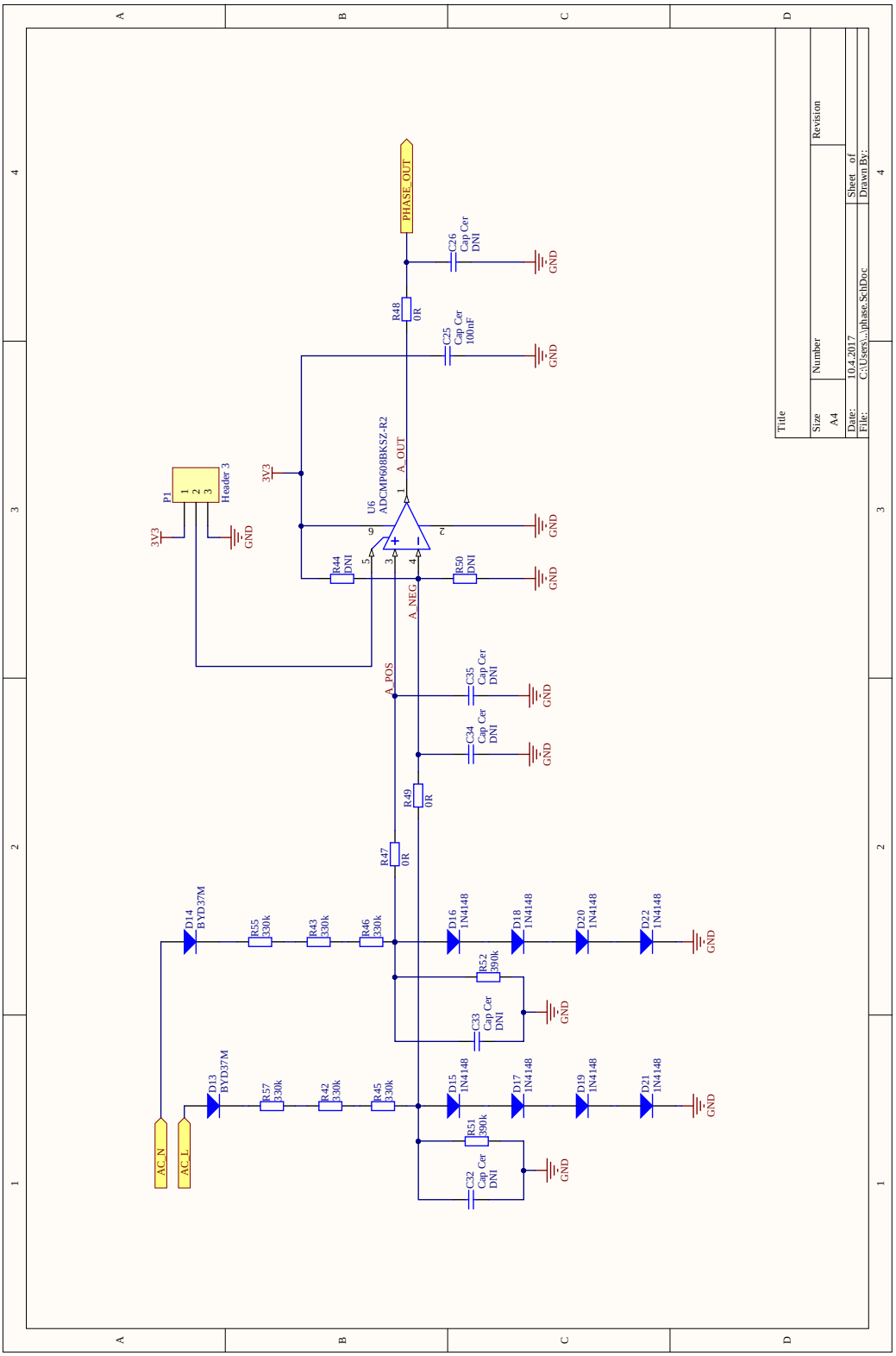

Fig. A.17 Schematic diagram of the positive wave detector (UCC28070).

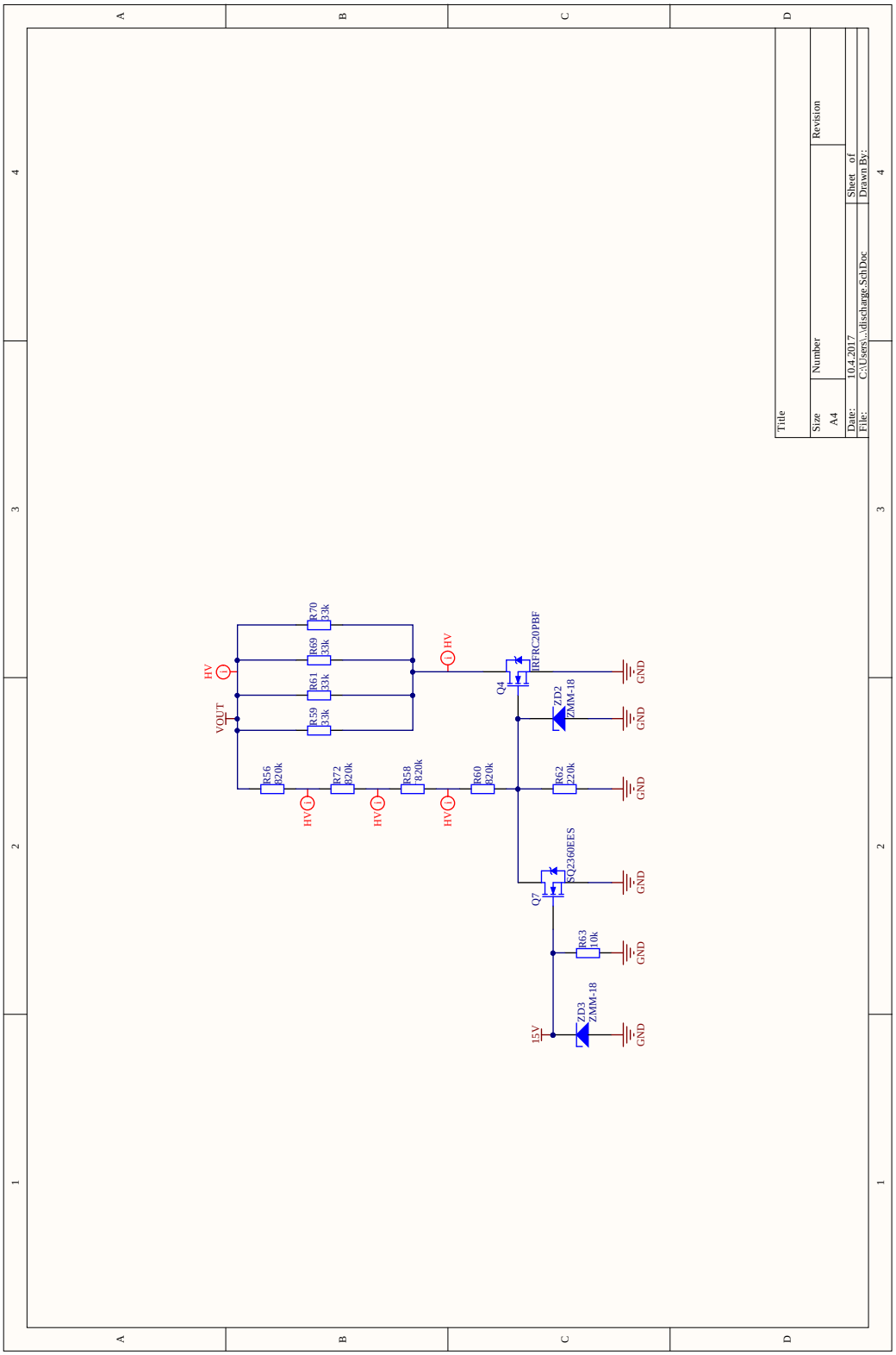

Fig. A.18 Schematic diagram of the bulk capacitor discharge circuitry (UCC28070).