The SVPWM Modulation Technique with Active Voltage Balancing Control for 3-level ANPC Inverter

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Abstract—**This paper presents advanced modulation technique for three-phase three-level ANPC inverter for drive applications. The Design of the converter allows actively balance the losses in the converter which results in higher power density, increase of reliability and lifetime of the converter. The control algorithm has to be able to secure the voltage control with proper capacitor voltage balancing as well as the active balancing of the losses in the converter. The proposed control is verified by experiments carried out on down-scale drive prototype of rated power 35kVA.**

Keywords—Multilevel converter, Converter control, SVPWM modulator, active balancing, DSP, FPGA.

I. INTRODUCTION

There are many papers dealing with topology of multilevel converters and their control strategies [1], [2], [3]. In this case we seek for advance control technique of three-level Active Neutral Point Clamped (ANPC) converter as an alternative way to complete the project of industrial company CKD ELEKTROTECHNIKA on mining machine drive design. For more details of ANPC topology see [2]. Thus we have chosen advanced simplified Space Vector Modulation (described in detail in [4]) which is supplemented by active balancing of the losses as a control technique of the ANPC inverter. This paper presents the continuation of our work on multilevel converters [5] and describes simple implementation solution of converter control of three-level ANPC inverter for medium-voltage drivers. The paper describes control of 3-level ANPC inverter which is based on simplified SVM with active balancing of the capacitor voltage and equal losses distribution control. Furthermore it describes the control implementation in our developed control unit MLC, which is in detail described in [6].

II. DESIGN OF THREE-LEVEL ANPC INVERTER CONTROL

The inverter control is based on simplified-SVM for the three-level ANPC inverter. The equivalent scheme of power circuit of the three-phase three-level ANPC is in Fig.1. Each phase of inverter consists of six IGBTs (S_1, S_2, ... , S_6). The total number of IGBTs is 18.

All phases are connected to dc-link which consists of two capacitors (C_1 and C_2). The voltage of those capacitors are actively balanced by the control algorithm.
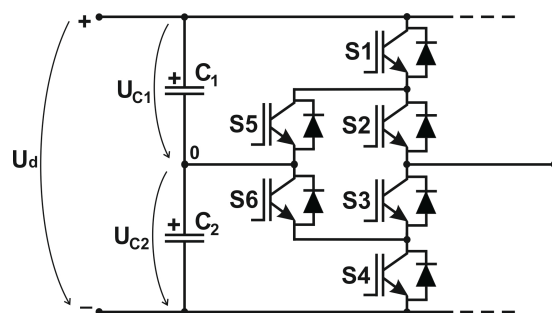

Fig. 1. A power circuit of developed prototype of three-phase three-level ANPC inverter (one phase of inverter) based on [2].

The simplified-SVM algorithm is suitable replacement for conventional modulators types for multilevel converter because of its simplicity and low computational demands. For more details see [4]. The input of the control algorithm is voltage space vector in *alpha beta* coordinate system (U_x, U_y). The algorithm outputs are three vectors which define triangle in the triangle net (see. 2) and three times for application (the duty cycles) of those vectors which. The algorithm has new convention where the triangle net is used to define the area where the input voltage space vector can appear (see Fig. 2).
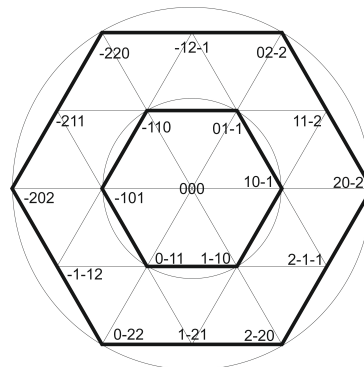

Fig. 2. Space vector diagram - triangles area for 3 level ANPC converter.

The second part of the algorithm is dedicated to the determination of the functions *floor* and *ceil* for all three voltage vectors V_a (1), V_b (2) and V_c (3). In this step the position of input voltage vector inside of one triangle is calculated. There are two shapes of triangles which depends on result of sum of floor functions ($f_{ab} + f_{bc} + f_{ca}$) see Fig. 3 and Table I.

$$f_{ab} = floor(V_a); \ c_{ab} = ceil(V_a) \quad (1)$$
$$f_{bc} = floor(V_b); \ c_{bc} = ceil(V_b) \quad (2)$$
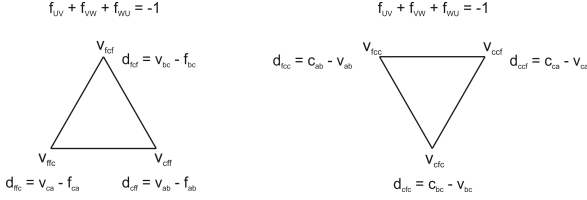$$f_{ca} = floor(V_c); \ c_{ca} = ceil(V_c) \quad (3)$$

Fig. 3. Triangle selections.

TABLE I. TRIANGLE SELECTIONS.

$f_{ab} + f_{bc} + f_{ca} = -1$	$f_{ab} + f_{bc} + f_{ca} \neq -1$
$V_{f_{ab}f_{bc}c_{ca}}$ (abbr. V_{ffc}) $d_{f_{ab}f_{bc}c_{ca}} = V_{ca} - f_{ca}$ (abbr. d_{ffc})	$V_{f_{ab}c_{bc}c_{ca}}$ (abbr. V_{fcc}) $d_{f_{ab}c_{bc}c_{ca}} = c_{ab} - V_{ab}$ (abbr. d_{fcc})
$V_{c_{ab}f_{bc}f_{ca}}$ (abbr. V_{cff}) $d_{c_{ab}f_{bc}f_{ca}} = V_{ab} - f_{ab}$ (abbr. d_{cff})	$V_{c_{ab}c_{bc}f_{ca}}$ (abbr. V_{ccf}) $d_{c_{ab}c_{bc}f_{ca}} = c_{ca} - V_{ca}$ (abbr. d_{ccf})
$V_{f_{ab}c_{bc}f_{ca}}$ (abbr. V_{fcf}) $d_{f_{ab}c_{bc}f_{ca}} = V_{bc} - f_{bc}$ (abbr. d_{fcf})	$V_{c_{ab}f_{bc}c_{ca}}$ (abbr. V_{cfc}) $d_{c_{ab}f_{bc}c_{ca}} = c_{bc} - V_{bc}$ (abbr. d_{cfc})

The MLC interface is based on combination of microcontroller and FPGA. Peripherals implemented in FPGA are mapped in memory into address space of used microcontroller thus they act as other peripherals which are located on chip. This new control system have great profit resulting from naturally parallel structure and universality of components which are created in FPGA. The microcontroller is the master control device and the FPGA works as a slave control device (Fig. 4) in our control system. Microcontroller computes control algorithm for inverter. The two dc-link capacitor voltages (C_1 and C_2) and the three currents are also measures by microcontroller.

On the output of microcontroller there are two voltage vectors components, which represent space vector for inverter (U_x, U_y), logic representation of condition of dc-link capacitor voltages (i.e. overvoltage or undervoltage of $\frac{1}{2}U_d$) and load currents directions. Those values are transmitted over parallel bus to the FPGA device, where the SVPWM modulator with active voltage balancing inverter is created.

The architecture created in FPGA can be split into seven main entities (see Fig. 5). The first entity *en_reg_2* represents synchronous input register for values (U_x, U_y) which are sending by microcontroller. The second entity *transform* transfers two input voltage vector components (U_x, U_y) in to three voltages (U_a, U_b, U_c). Each of those voltages represents modulation signal for the third entity. The entity *svm_alg*

calculate the Novel SVM algorithm and identify three closest vectors of the input voltage vector and theirs duty cycles. This three vectors defines switching index. The identification of switching index is made by entity *svm_maping*. The switching indexes and duty cycles are processed by entity *time_table*. This entity creates the switching sequence for one switching period. Switching sequence gradually switch all possible real switching combinations. For example of real switching combinations for sector 1 see fig. 6. The combinations which are balancing dc-link voltage are switched on 2/3 time and the combinations which are not balancing dc-link voltage are switched on 1/3 time. The next entity *timings_ANPC* ensures proper timing of switching sequence (e.g. timing for sector 1 and area 1 is in 7) as well as active clamping control. In this case the main difference between NPC is in zero switching combinations where we can choose the upper or lower clamping converter part to be inducting. In order to keep the design of the control as simple as possible we limited our choices to the combinations where always only two switches are switched on at the time (Table II). Thus when the current commutes from the upper part of the converter we chose the upper clamping switch to be conducting and vice versa. Thereby when the switching sequence contains zero switching combination, always both of clamping ways in the converter are used and the distribution of the losses is more balanced. The last entity *gate* sets up the final control signals for inverter.
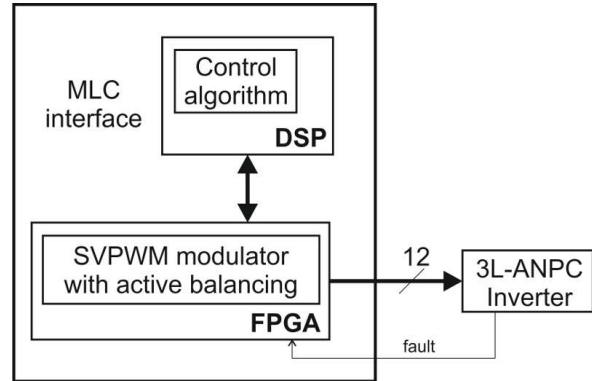

Fig. 4. Communication block-diagram

III. SIMULATION AND EXPERIMENTAL RESULTS

The active clamping control algorithm was tested in simulations with parameters: $R = 0.245[\Omega]$, $L = 0.0011[H]$, $V_{dc} = 700[V]$, $f_{PWM} = 800[Hz]$ (Fig. 9) and the results ware compared with classical NPC design (Fig. 8). Proposed control algorithm of three-level ANPC inverter has been implemented in the floating-point microcontroller Texas Instruments TMS320F28335. The SVPWM modulator with voltage balancing have been implemented in the FPGA Altera Cyclone III EP3C40F240C7. Proposed control has been tested on developed laboratory prototype of the APNC inverter of rated power 35kVA. Fig. 10 shows steady-state behaviour of outputs of unloaded three-level ANPC inverter. Fig. 11 shows frequency spectrum of phase current, THD is 7.08.
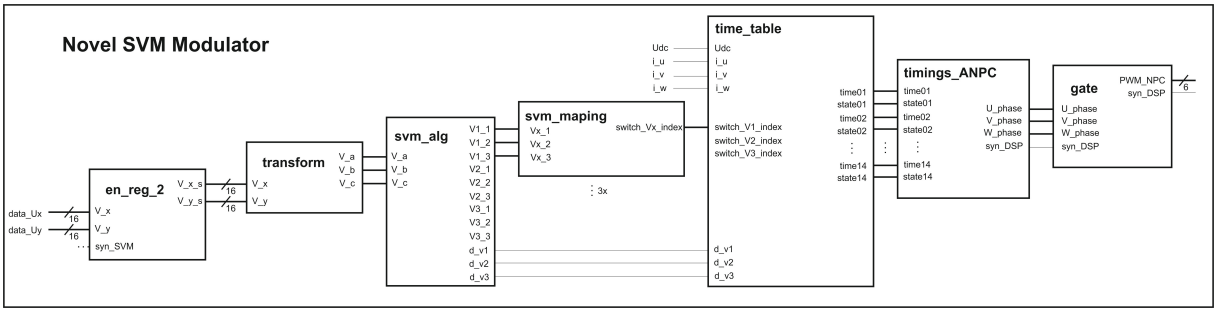
Fig. 5.   Architecture of SVPWM modulator entity in FPGA

TABLE II.   REAL SWITCHING COMBINATION.

Space vector diagram index	Real switching combination
0 0 0	-1 -1 -1 0 0 0 1 1 1
1 0 -1	1 0 0 0 -1 -1
0 1 -1	1 1 0 0 0 -1
-1 1 0	0 1 0 -1 1 -1
-1 0 1	0 1 1 -1 0 0
0 -1 1	0 0 1 -1 -1 0
1 -1 0	1 0 1 0 -1 0
2 0 -2	1 -1 -1
1 1 -2	1 0 -1
0 2 -2	1 1 -1
-1 2 -1	0 1 -1
-2 2 0	-1 1 -1
-2 1 1	-1 1 0
-2 0 2	-1 1 1
-1 -1 2	-1 0 1
0 -2 2	-1 -1 1
1 -2 1	0 -1 1
2 -2 0	1 -1 1
2 -1 -1	1 -1 0
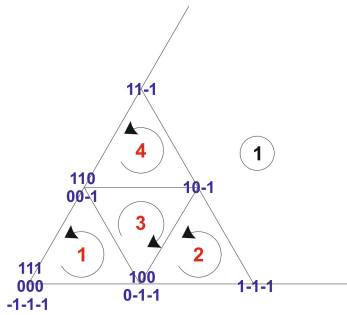
Fig. 6.   Switching combination for sector 1

IV.   CONCLUSION

In this paper, the control algorithm for three-phase three-level ANPC inverter ware presented. The design of the control algorithm is very simple and easy for implementation. Moreover as shown in the simulation and experimental results the proposed control algorithm is able to, effectively control the voltage, balance the voltage on single capacitors and secure the losses distribution control in the inverter. Furthermore splitting of proposed control into two separate entities (DSP, FPGA), brings several advantages. Control unit presented in this paper is able to simultaneously control two three phase circuits of full three-level ANPC converter. Another significant advantage of this configuration is modular composition of switching sequence, which allows easily change the parameters of the modulator (e.g. switching frequency, capacitor voltage balancing control etc.).

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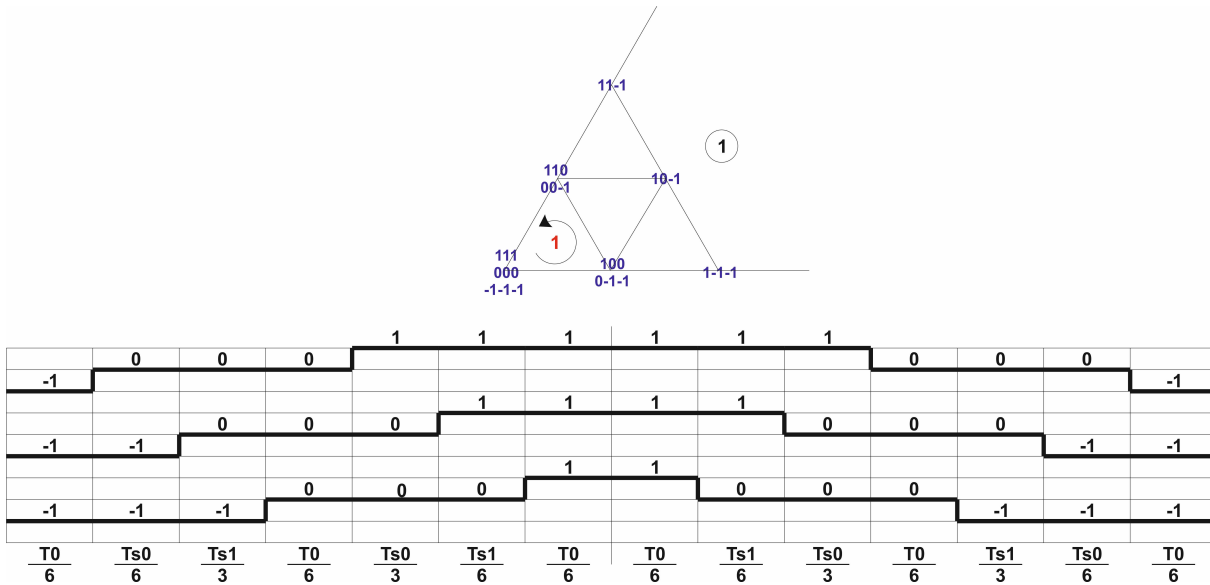
Fig. 7. Timing of switching combination for sector 1 and area 1
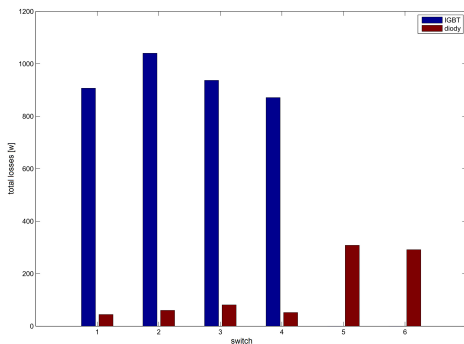

Fig. 8. Total losses distribution in the converter powering RL load with input voltage V_{dc}=700[V] modulation index 0.95 on single switches of the converter NPC
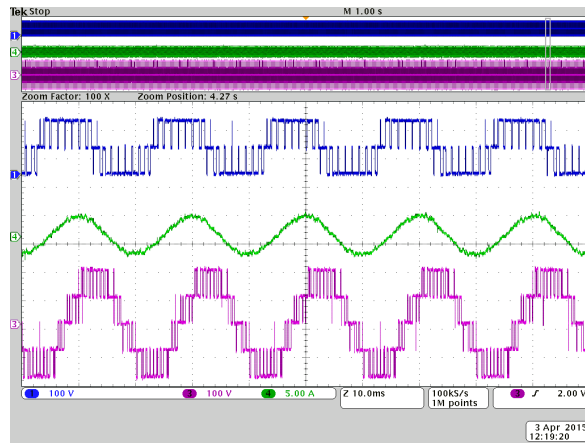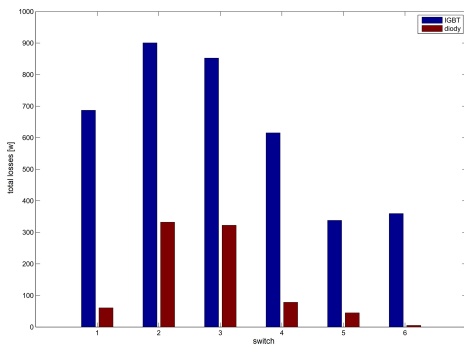

Fig. 10. Behaviour of three-level ANPC inverter unloaded (Udc=200 V), Ch1: three-level line voltage of inverter [100V/d], Ch2: line to line inverter voltage [100V/d], Ch4: inverter phase current [5A/d]

Fig. 9. Total losses distribution in the converter powering RL load with input voltage V_{dc}=700[V] modulation index 0.95 on single switches of the converter ANPC
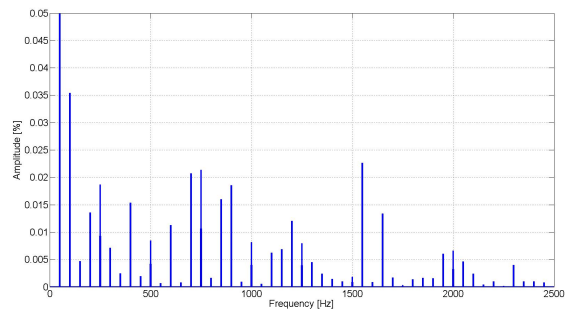

Fig. 11. Frequency spectrum of phase current, THD is 7.08%