Floating Capacitance Multiplier Simulator For Grounded RC Colpitts Oscillator Design

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Abstract – **Actively simulated grounded floating capacitance multipliers have been used in several applications ranging from filter to oscillator design as well as cancellation of parasitic capacitances. In this paper, a new electronically-controllable floating lossless capacitance multiplier (C-Multiplier) circuit is presented, which employs only one Voltage Differencing Current Conveyor (VDCC), one grounded capacitor and one grounded resistor. Since the new simulated C-Multiplier uses a grounded capacitor; accordingly, it is suitable for IC fabrication. A number of simulations with employing commercially available devices through PSPICE program are accomplished to demonstrate the workability, performance, and effectiveness. Functionality of the proposed circuit is verified through its application in a linearly tunable quadrature oscillator, which one is derived from Colpitts oscillator.**

Keywords-capacitance multiplier; Colpitts oscillator; quadrature oscillator; voltage differencing current conveyor, VDCC

I. INTRODUCTION

A circuit employing a minimum number of active and passive components is advantageous from the points of view of very large-scale integration (VLSI) implementation, area, power consumption, and cost. Also, it is well known that, in IC processes, the realization of grounded passive components, especially grounded capacitors [1], are more convenient than floating ones [2, 3]. Hence, the circuit designer should avoid using floating passive components and passive component-matching constraints as much as possible.

Recently, various active building blocks have been introduced in [4], where voltage differencing current conveyor (VDCC) is one of them. Since VDCC provides electronically tunable transconductance gain in addition to transferring both current and voltage in its relevant terminals, it is very suitable for the design of functional generators [5], inductor simulators [6, 7], triple-input single-output filter with independently adjustable filter parameters [8], reconfigurable reconnection-less first-order voltage-mode multifunctional filter [9], and single resistance controlled sinusoidal oscillator [10]. In order to increase the versatility of the VDCC, the aim of this paper is realize a capacitance multiplier with minimum number of elements and to show functionality of the proposed circuit through its application with inexpensive commercially active elements. PSPICE simulations are carried out to show the AC domain performances of the circuit. The floating C-Multiplier circuit is used in Colpitts oscillator modification instead of floating capacitor.

II. CIRCUIT DESCRIPTION

The block diagram of a VDCC, ideally characterized by equations $I_Z = g_m(V_P - V_N)$, $V_X = V_Z$, $I_{W_P} = I_X$, and $I_{W_N} = -I_X$, is demonstrated in Fig. 1, where P and N are input terminals, Z auxiliary terminal, X, W_P and W_N are output terminals. Except the X terminal, all of the terminals exhibit high impedance. This conception was used in [4, 7].

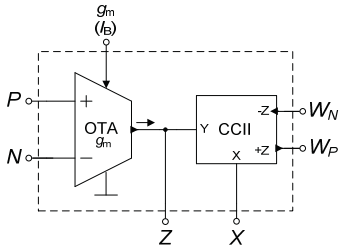

Figure 1. The block diagram of VDCC

The proposed circuit for realizing a floating lossless electronically-controllable C-Multiplier is shown in Fig. 2. The circuit is constructed with single VDCC, one grounded resistor, one grounded capacitor, and its short circuit impedance matrix can be written as:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = sC_{eq} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \qquad (1)$$

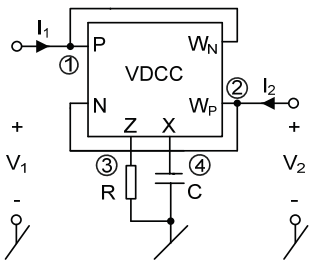

Figure 2. Proposed C-Multiplier circuit

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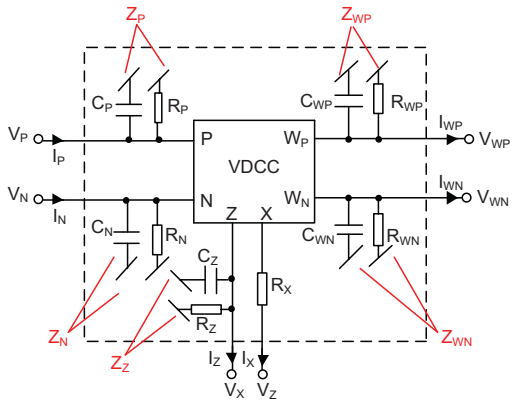

Figure 3. Model of the VDCC including parasitics elements

from which:

$$C_{eq} = CRg_{\mathrm{m}}. \tag{2}$$

From equations (1) and (2) it can be seen that the equivalent capacitance value is controllable electronically and linearly with transconductance gain of VDCC.

A. *Non-Ideal Analysis*

For a complete analysis, it is important to take into account parasitics of active element shown in Fig. 3: $I_{\mathrm{Z}} = g_{\mathrm{m}}(V_{\mathrm{P}} - V_{\mathrm{N}})$, $V_{\mathrm{X}} = \beta V_{\mathrm{Z}}$, $I_{\mathrm{W_P}} = \alpha_1 I_{\mathrm{X}}$, $I_{\mathrm{W_N}} = -\alpha_2 I_{\mathrm{X}}$, where α_j represents current gain and β represents voltage gain of the VDCC that differ from their ideal values by tracking errors ε_{ij} ve ε_{v} ($|\varepsilon_{ij}|$, $|\varepsilon_{\mathrm{v}}| << 1$), where $j = 1, 2$.

- The parasitic resistances R_{N}, R_{P} and parasitic capacitances C_{N}, C_{P} appear between the high-impedance N (1 MΩ // 2.1 pF) and P (455 kΩ // 2.1 pF) input terminals of the VDCC and ground, respectively.
- The parasitic resistance R_{Z}, and parasitic capacitance C_{Z} appear between high-impedance Z auxiliary terminal of the VDCC and ground, respectively and their typical values are 25 kΩ // 4.2 pF.
- The parasitic resistance R_{X} appears at the low-impedance terminal X of the VDCC and its typical value is 95 Ω.
- The parasitic resistances and capacitances $R_{\mathrm{W_P}}$, $R_{\mathrm{W_N}}$, and $C_{\mathrm{W_P}}$, $C_{\mathrm{W_N}}$ appear between the high-impedance $\mathrm{W_P}$ and $\mathrm{W_N}$ output terminals of the VDCC and ground, respectively and their typical values are 1 MΩ // 5 pF.

Considering the effect of aforementioned non-idealities on the proposed circuit implemented as shown in Fig. 4, the following useful analysis can be provided:

- At the node 1 and 2, the parasitic terminals of VDCC, *P*, W_{N} and *N*, W_{P} are parallel respectively, and in analysis they are shown as $Z_{\mathrm{PW_N}} = Z_{\mathrm{P}} // Z_{\mathrm{W_N}}$, and $Z_{\mathrm{NW_P}} = Z_{\mathrm{N}} // Z_{\mathrm{W_P}}$.
- At the node 3, the parasitic terminal Z of VDCC appears high resistance and this resistance is parallel with parasitic capacitance, described as $Z_{\mathrm{Z}} = R'_1 // sC_{\mathrm{Z}}$, while $R'_1 = R_{\mathrm{Z}} // R$.
- At the node 4, the parasitic terminal X of VDCC appears low resistance and this resistance is series with this terminal capacitance, described as $Z_{\mathrm{X}} = R_{\mathrm{X}} + 1/sC$.

Hence, the short circuit impedance matrix in Eq. (1) turns to:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{\beta g_{\mathrm{m}} Y_{\mathrm{X}}}{Y_{\mathrm{Z}}} \begin{bmatrix} \dfrac{Y_{\mathrm{PW_N}} Y_{\mathrm{Z}}}{\beta g_{\mathrm{m}} Y_{\mathrm{X}}} + \alpha_2 & -\alpha_1 \\ -\alpha_2 & \dfrac{Y_{\mathrm{NW_P}} Y_{\mathrm{Z}}}{\beta g_{\mathrm{m}} Y_{\mathrm{X}}} + \alpha_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{3}$$

The parasitic zero of the impedance at high frequencies can be seen from Fig. 5 as:

$$f_o = 1/2\pi CR_{\mathrm{X}}, \tag{4}$$

and the frequency dependent AC model of C-Multiplier can define as:

$$f_{\mathrm{p}} = 1/2\pi C\left(R_{\mathrm{X}} + R_{\mathrm{p1}} R g_{\mathrm{m}}\right), \tag{5}$$

where R_{p1} is parasitic resistance at terminals P and $\mathrm{W_N}$.

III. Circuit Implementation with Commercially Active Elements

Simulations were performed using commercially available active devices of VDCC shown in Fig. 4. We implemented well-known current-mode two-quadrant multiplier EL2082 [11] (known also as electronically controllable current conveyor of second generation - ECCII) with adjustable current gain (*B*), one diamond transistor (OPA660 [12]) and current-mode four-quadrant multiplier EL4083 [13] (serving as current follower/inverter) to build VDCC. The supply voltages are selected as $V_{\mathrm{DD}} = -V_{\mathrm{SS}} = 5\mathrm{V}$. Equation for equivalent capacitance available from behavioral model has form:

$$C_{eq} \cong CRBg_{\mathrm{m}} = \frac{CRB}{R_{\mathrm{d1}}}. \tag{6}$$

The proposed circuit shown in Fig. 4 is simulated with the following passive element values: $R_{\mathrm{a}} = 5$ kΩ, $R_{\mathrm{b}} = 10$ kΩ, $R_{\mathrm{x}} = 95$ Ω, $R = 20$ kΩ, $C = 50$ pF, $B = 0.5$ ($V_{\mathrm{SET\_B}} = 0.5$ V), where *B* is fine current gain adjusting, which results in $C_{\mathrm{eq}} = 220$ pF. The calculation from (6) provided $R_{\mathrm{d1}} = 1/g_{\mathrm{m}} = 2.3$ kΩ. Due to effects of parasite elements, value of *B* to 0.8 V was changed. The ideal and simulated impedance magnitudes and phase versus frequency for the proposed capacitance multiplier of Fig. 4 are shown in Fig. 5. It can be seen that the simulated and

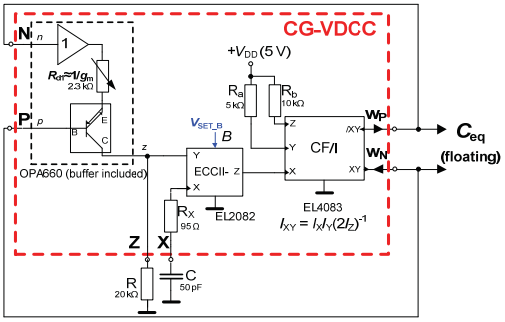

Figure 4. Circuit implementation with commercially available active devices

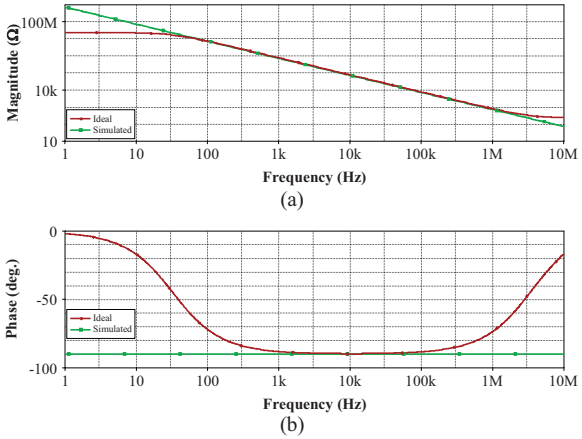

Figure 5. Magnitude and phase characteristics of the simulated capacitance multiplier using the behavioral model (Fig. 4)

ideal response are very close to each other in the frequency range of 100 Hz to 1 MHz.

IV. Replacement of Floating Capacitance in Colpitts Oscillator

To verify the theoretical analysis, the behavior of the floating capacitance multiplier circuit from Fig. 4 and equivalent LC Colpitts oscillator [14] (derived from idea presented in [15] shown in Fig. 6 have been verified by PSPICE simulations using commercially available active devices. Current-mode multiplier EL2082 [11] as adjustable current amplifier (B) and two diamond transistors (OPA660 [12]) to build operational transconductance amplifiers (OTAs) are used for implementation Fig. 6. Recommended supply voltage for the devices is ± 5 V. Values of passive elements are selected as: $C_1 = C_3 = C_{eq} = 220$ pF, $R_i = 910\ \Omega$. Verification of correct operation is given for two discrete frequencies of oscillations. Therefore, transconductances ($g_{m1} = g_{m2} = g_m$) of the OTAs were adjusted in two discrete values (0.2 mS and 1 mS). Theoretical values of frequency of oscillation (FO) ($\omega_0 = g_m\sqrt{2}/C$ [14]) are expected as: 204 kHz and 1.023 MHz.

Initial setting of the oscillator was given by: $g_{m1} = g_{m2} = 1$ mS. Steady state transient responses at all three nodes (V_1, V_2, V_3) are presented in Fig. 7 together. The FO had value $f_0 = 980$ kHz. Constant phase shift of signals V_2 and V_3 is approximately 87 degree.

Note that the V_1 is not suitable as output of the multiphase oscillator because phase shift between it

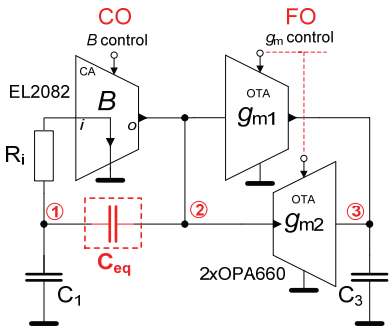

Figure 6. Derivation of Colpitts oscillator [14] where floating capacitance was replaced by proposed floating C-Multiplier

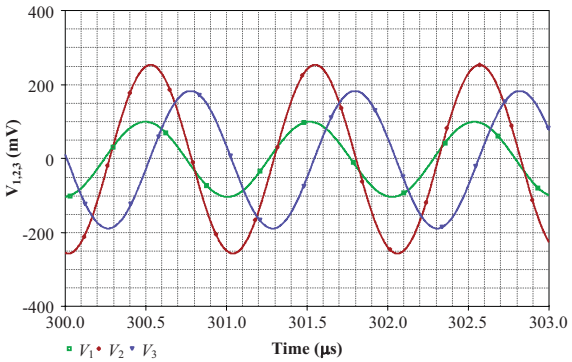

Figure 7. Steady state transient response of the output voltages for stable frequency

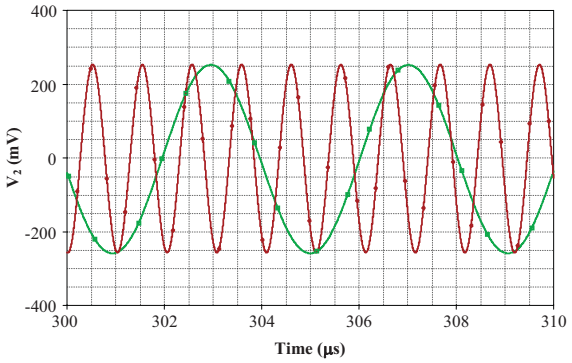

Figure 8. Steady state transient response for two discrere values of $g_m = 0.2$ and 1 mS at V_2

and V_2 and V_1 as well as amplitude relation depends on FO [14]. Nodes 2 and 3 are useful to obtain quadrature phase shift with constant amplitude level during the tuning process. Fig. 8 shows steady state transient response of V_2 for oscillation frequencies (246 kHz and 980 kHz for $g_{m1,2} = 0.2$ and 1 mS).

FFT analysis of the output voltage V_2 is shown in Fig. 9. Transconductance control of the commercially available active device OPA660 between 0.2 and 1 mS allows FO tuning in range from 246 to 980 kHz. Total harmonic distortion (THD) achieves values below 1% for 246 kHz ($g_m = 0.2$ mS) because higher harmonics components are suppressed more than 45 dBc. In the highest corner of frequency (980 kHz for $g_m = 1$ mS), we obtain even higher suppression more than 60 dBc, that yields THD lower than 0.1% Note that frequency utilization of the C-Multiplier is restricted (Fig. 5) by phase error in oscillator application especially. It limits usability of our behavioral model (including specified parameters in Fig. 4) up to 1 MHz maximally.

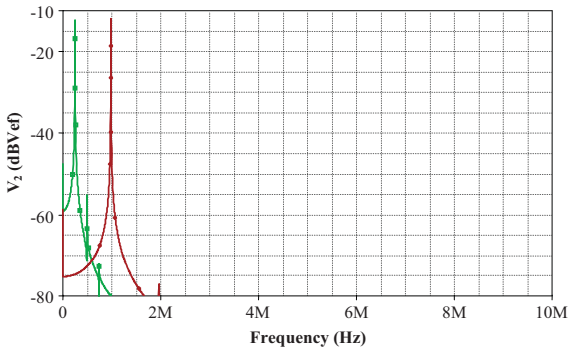

Figure 9. FFT spectrum of V_2 for both adjusted frequencies

V. Conclusion

Since in the literature available realizations of C-Multipliers are unsuccessful in one or more of the subjects as employing two or more active devices [16, 17], using lots of passive elements [18, 19], lack of tunability [20], the main topic of this paper is to propose a floating C-Multiplier and its implementation based on behavioral model (emulator) with commercially available active devices (Fig. 4). Range of floating capacitance simulation was obtained from 100 Hz to 1 MHz if phase error about 15 degree (Fig. 5b) is expected (for parameters of the circuit in Fig. 4). Operation with minimal phase error (less than 1-2 degrees) is allowed in range from 1 kHz to 100 kHz. These inaccuracies depend on specific design and real parasitic influences that can be significantly suppressed or emphasized for specific selection of values of parameters in Fig. 4.

Correct operation of the floating C-Multiplier was verified in quadrature oscillator [14] derived from Colpitts prototype [15]. The oscillator in Fig. 6 has several advantages like control of oscillation condition (CO) by B of used adjustable current amplifier, consists of availability of quadrature output signals based on transconductances (OTAs) and linear control of FO [14]. In this paper, the remaining one disadvantage of oscillator-floating capacitor, which one comes from the principle of the Colpitts oscillator, is improved with proposed capacitance multiplier. Commercially available active devices allowed construction of the behavioral representation (Fig. 4) of the circuit. Achieved range of tunability was obtained from 246 kHz to 980 kHz. THD below 1% was obtained in this range of frequency adjusting. Phase shift 87 degrees was obtained at stable frequency 980 kHz. The workability of the proposed circuit and application has been confirmed by PSPICE simulations.

Acknowledgment

Research described in this paper was financed by the National Sustainability Program under grant LO1401. For the research, infrastructure of the SIX Center was used. Ing. Norbert Herencsar, Ph.D. was supported by the project CZ.1.07/2.3.00/30.0039 of Brno University of Technology, and by the Czech Science Foundation under grant no. GP14-24186P. This research was also supported by the BUT project FEKT-S-14-2352.

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