A Universal Configurable Sinusoidal Modulator for H-bridge Based Converters Implemented in FPGA

Tomas Kosan[1], Martin Jara[2], Vojtech Blahnik[3], Zdenek Peroutka[4]

Regional Innovation Centre for Electrical Engineering (RICE), Faculty of Electrical Engineering,
University of West Bohemia, Univerzitni 26, 306 14 Pilsen, Czech Republic
[1]kosan@rice.zcu.cz, [2]jara@rice.zcu.cz, [3]lucke@rice.zcu.cz, [4]peroutka@ieee.org

***Abstract*—This paper describes a universal sinusoidal modulator developed primarily for the multilevel cascaded H-bridges converters. The modulator was implemented as a FPGA entity and its versatile features allows it to be easily reused in various topologies based on H-bridges. This includes the control of the H-bridge resonant converters by pulse frequency modulation so that it is well suitable for the power electronic transformer topologies. The modulator's performance is illustrated on a laboratory prototype of seven-level active front-end.**

***Index Terms*—cascaded H-bridges, active front end, filed programmable gate array (FPGA), multilevel converter**

I. Introduction

Multilevel converters become dominant solution in case of medium voltage high power converters thanks to their ability to operate directly of the distribution power grid [1], [2]. Among the basic topologies involving the neutral point clamped inverters, capacitor clamped (flying capacitor) inverters and cascaded H-bridges (CHB), the latter one gained large popularity as it well fits the high power regenerative type motor drives [3]. Also this topology is often employed in a various proposals of power electronics transformer (PET) blocks [4], [5] developed for heavy traction drives or photovoltaic systems [6]. An emerging application field of CHB presents the e-motive charging stations [7] and electric car low voltage on board DC/DC converters [8].

Though the CHB converters require the lowest count of components (in comparison with flying capacitor or neutral point clamped converters), the number of PWM control channels is still high. For example the seven-level single phase inverter based on CHB has twelve active switching devices. Therefore, in a practice, the control unit usually splits the control task into two subsystems [9], [10]. The first is a computational part, usually based on an appropriate DSP or DSC, which implements the control algorithm. The second subsystem provides the required number of modulators with appropriate number of the output PWM channels. This subsystem uses the values calculated by the first subsystem and mostly is implemented in FPGA.

This paper describes a FPGA implementation of a versatile modulator suitable for CHB inverters or active front-ends. Thanks to its configurability it can be used for the other H-bridge converters including the resonant ones. That is why the same modulator type can drive each block of complex topologies such as the PET which may simplify and speed-up the overall FPGA design.

II. Universal modulator for H-bridge

The main purpose of the modulator presented in this paper is to properly modulate a simple H-bridge power circuit shown on Fig. 1. The circuit consists of two complementary pairs of switches, DC-link and a pair of phase inputs or outputs. This simple structure is an elemental cell of the CHB converters with bidirectional power flow.

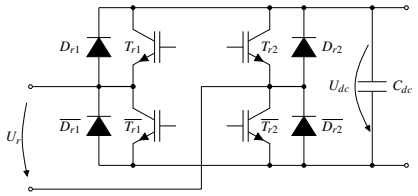

Fig. 1. Schematics of H-bridge

Generally the whole H-bridge can be controlled by a single modulation signal (u_m) because of the complementarity of the transistor pairs T_1, $\overline{T_1}$ and T_2, $\overline{T_2}$. Therefore the u_m signal with opposite sign controls the second pair. The resulting block diagram of the designed H-bridge modulator is shown on Fig. 2.

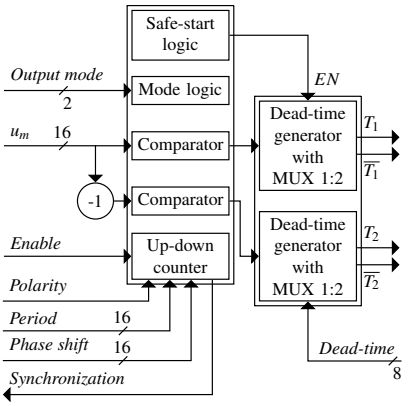

Fig. 2. Block schematics of H-bridge modulator

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Basic component of modulator entity is a fully symmetric up-down 16-bit wide counter which counts from $-N_p$ (negative value of period) to N_p (positive value of period). This results in a triangular waveform shown on Fig. 3 which acts as a carrier for the pulse-width modulated (PWM) signal. The value of N_p for the required carrier frequency of the PWM signal (f_{PWM}) can be calculated by (1), where f_{clk} is the FPGA clock frequency assigned to the entity within the FPGA design.

$$N_p = \frac{f_{clk}}{4.f_{PWM}} \tag{1}$$

The output PWM signals for the complementary pairs are generated by two comparators. They compare the input modulation signal u_m and its inverted value $-u_m$ with the actual counter value and thus create the PWM signals. These signals are consequently fed to the pair of dead-time generators. The generators transform the single bit signals into two bit signals where each bit drives one of the two transistors within a complementary pair (T_1 + $\overline{T_1}$ or T_2 + $\overline{T_2}$). A user defined dead-time is applied to the both output signal pairs.

The modulator is also able to shift the PWM triangular carrier in order to allow easy implementation of the phase-shift pulse-width modulation (PS-PWM). User can set N_s (phase shift) value within the range $\langle -N_p, +N_p \rangle$ where the values $-N_p$ and $+N_p$ correspond to the phase shift φ of -90 to +90 degrees according to (2) . This feature is available to any number of cascaded H-bridges.

$$N_s = \frac{\varphi}{90} N_p \tag{2}$$

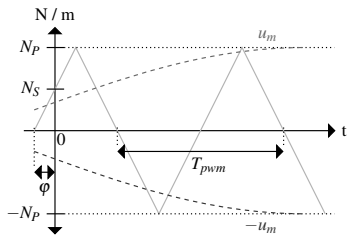

Fig. 3. Triangular carrier of modulator

The phase shifting capability is used together with *Enable* signal which enables the counter's operation and therefore it allows the synchronization of multiple instances of the modulator entity. *Polarity* signal sets the logical polarity of the PWM outputs. The *Synchronization* signal is generated anytime the PWM carrier reaches either top or bottom values. The signal is another mean to synchronize the modulator instances or it can be used to synchronize the FPGA design with the DSP.

The modulator supports four different modes of operation selectable by two bit *Output mode* signal as summarized in Table I. In the normal mode the output waveform follows input modulation signal u_m so that it controls the output frequency and amplitude as indicated in Fig. 4. This mode is dedicated to the multilevel CHB converters control. The resonant mode on the other hand supposes that frequency can be variable and programmed by *Period* input. The output waveforms achieve both polarities within a single period of the carrier (Fig. 5). So that it can conveniently control resonant mode converters as well with the pulse frequency modulation. Since the length of the output pulses is still controllable by u_m signal and zero vectors are inserted between the active periods this mode is also suitable for the phase shifted PWM converters. In the half-bridge modes the complementary pair with index 2 is forced to remain in state where T_2 is turned off and $\overline{T_2}$ is on. This feature can be employed during the soft-start of H-bridge converters as they are forced to operate as the half bridge converters.

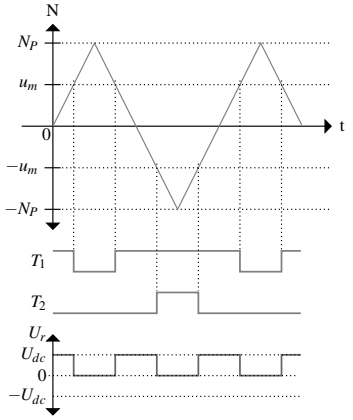

Fig. 4. U_r output waveform in normal mode

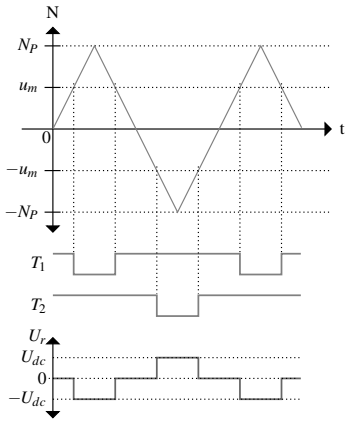

Fig. 5. U_r output waveform in resonant mode

A special attention was paid to the correct and safe start-up of the modulator's multiple instances structure. In order to enable the whole structure the proper *Phase shift* values should be loaded first for each instances. Then the common *Enable* signal should be asserted and the counters start to generate the carriers. Anyway there are still two conditions to be met in order to enable the PWM outputs. First, the carrier must reach either the top or the bottom of the triangle. And the second, there must be valid data in u_m (any non-zero values). Once met, the internal signal EN_n is

TABLE I
MODES OF OPERATION FOR H-BRIDGE MODULATOR

Mode	Description
00	Normal mode, full H-bridge active
01	Resonant mode, full H-bridge active
10	Normal mode, half H-bridge active
11	Resonant mode, half H-bridge active

generated and the entity's outputs are enabled (see Fig. 6). This approach prevents the CHB converter from uncontrollable start-up and highly probable over-currents.

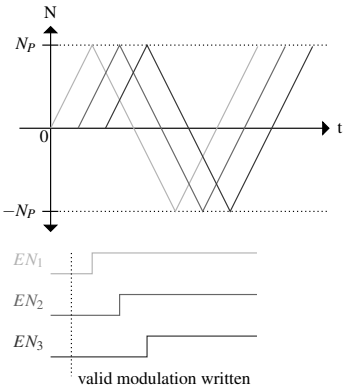

Fig. 6. Principle of safe-start feature

The modulator itself and supporting entities was implemented in pure VHDL code and with Altera's Cyclone III EP3C40 as a target. The control algorithm was implemented in DSP enabled microcontroller TMS320F28335. A development platform described in [10] containing both mentioned devices was employed.

III. PERFORMANCE OF THE MODULATOR IMPLEMENTATION

Initial functional test of proposed modulator was carried out with a single H-bridge inverter with R-L load. The dc-link of H-bridge was connected to dc power source of 38 V. The results shown on Fig. 7 confirm proper three level output voltage waveform u_{ui1} corresponding to the modulation signal u_{mi1}.

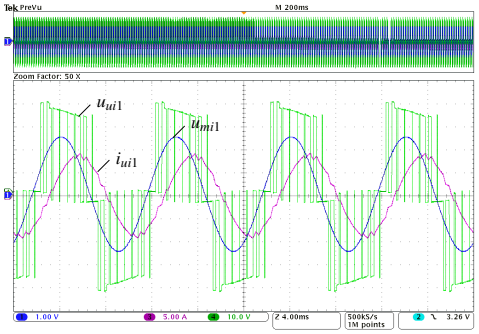

Fig. 7. Inverter mode of modulator with R-L load, U_{udc1}=38 V, R=6.5 Ω, L=1 mH, f=208 Hz, f_{PWM}=800 Hz CH1: u_{mi1} modulation signal [0.4/div], CH3: i_{ui1} inverter phase current [5 A/div], CH4: u_{ui1} inverter phase output voltage [10 V/div]

Consequently the modulators were incorporated into a control system of a single phase active fronted (AFE) consisting of six H-bridges. Schematics of the power circuit is pictured on Fig. 9. The H-bridges with index *r* act as AFE while index *i* marks inverter part of circuit.

Generally variable loads on each serially connected section's outputs allow testing various imbalance conditions of the three dc-links.

The Fig. 8 shows simplified block schematics of the FPGA design for the converter mentioned above. The design consists of six H-bridge modulators (HB-mod). Their inputs (N_p, u_m etc.) are connected to the entity which implements memory mapped registers (MM registers). This entity serves as a bridge between the particular modulators and the DSP/DSC. Synchronization pulses from each modulator entity are combined in the synchronization manager (Sync. manager) and the resulting interrupt signal is used to synchronize the FPGA design and the DSC control algorithm.

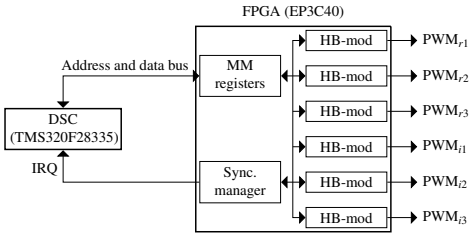

Fig. 8. Symplified block schematics of control design for 7L-CHB AFE and three separate inverters

The AFE's control algorithm was based on the work [11] and it was extended to support three cascaded H-bridges. This control method utilizes proportional-resonant regulators therefore its outputs (modulation signals u_m) are sinusoidal and can be directly fed to the modulators.

The Fig. 10 shows AFE no-load waveforms while Fig. 11 shows AFE input under the load of 1.6 kW. The proper performance of the modulators are confirmed by a regular seven-level voltage waveform u_{ur} under the both conditions.

IV. CONCLUSION

Presented universal H-bridge FPGA modulator was developed with a strong emphasis on reusability in the FPGA design and versatility. Though the primary target applications were the multilevel CHB based converters, the modulator can employ other modulation techniques such as PFM and PS-PWM. Special attention was paid to the safe and synchronized start-up of the multiple instances structure.

Proper functionality of the modulator's entity was thoroughly tested in several applications. The performance results of the modulator while built in a single-phase inverter and seven-level CHB converter are briefly described here.

V. ACKNOWLEDGMENT

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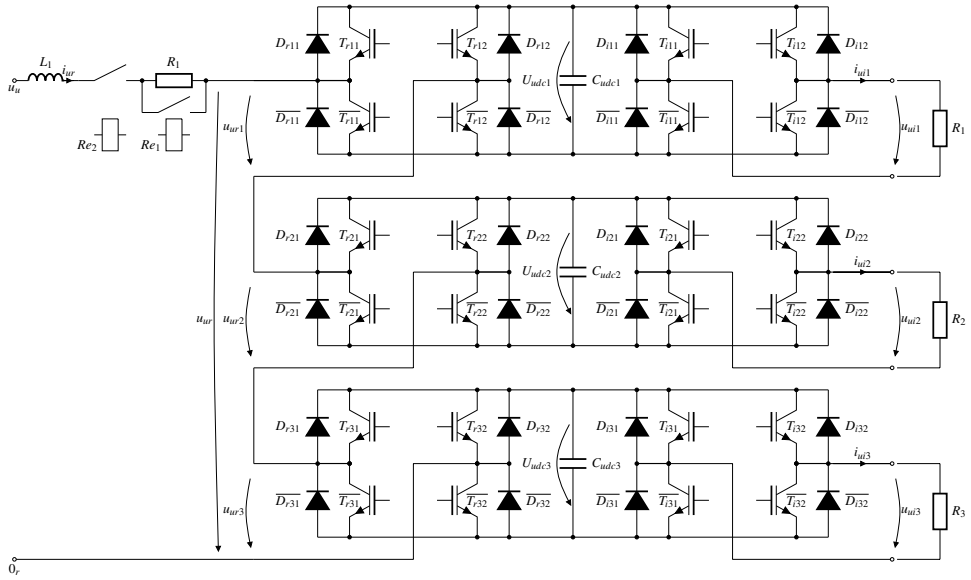

Fig. 9. Schematics of 7L-CHB AFE with three separate inverters

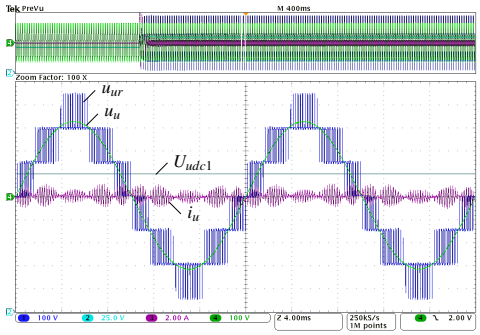

Fig. 10. Output waveforms of 7L-CHB active front end under no load, U_u=230 V, f=50 Hz, CH1: u_{ur}, output phase voltage of AFE [100 V/div], CH2: U_{udc1}, dc-link voltage of 1st H-bridge [25 V/div], CH3: i_{ur}, phase current of AFE [5 A/div], CH4: u_u, mains voltage [100 V/div]

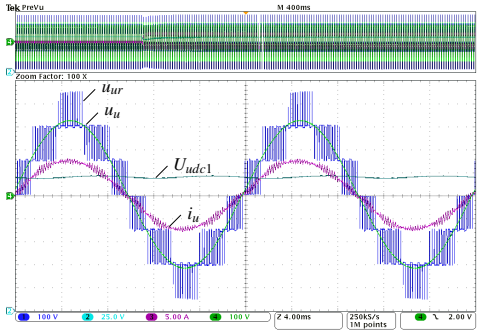

Fig. 11. Output waveforms of 7L-CHB active front end under load of 1.6 kW, U_u=230 V, f=50 Hz, CH1: u_{ur}, output phase voltage of AFE [100 V/div], CH2: U_{udc1}, dc-link voltage of 1st H-bridge [25 V/div], CH3: i_{ur}, phase current of AFE [5 A/div], CH4: u_u, mains voltage [100 V/div]

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