Broadband Bias Networks for Pulse Signal RF Amplifiers

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***Abstract* – This article describes one possible solution of bias networks for special broadband RF amplifiers. The purpose is amplification special pulse signals from particle detectors, which demands well defined time domain properties. The problem is demonstrated on two basic prototypes with different amplifier chips used in. Both are designed using standard components with poor results and using special broadband inductors which gave much better results. At last, design and verification of the broadband inductors is presented.**

Keywords- amplifier bias network; bias tee; broadband RF amplifier; pulse signal amplifier

I. INTRODUCTION

Using solid state detectors gives us possibility to get very accurate information about particle pass in a small and well defined space [1]. Also the space needed for the detector is quite small and ability to design the sensitive semiconductor chip in various dimension and electrode configuration is attractive. The disadvantage of these detectors is very small output signal, which has to be processed. Amplifiers need not only high signal gain, but also low distortion of pulsed signal, especially on its rising edges. This means special requirements on amplifier frequency response, both in the amplitude and in the phase.

For maintaining the pulse shape in the time domain having a linear phase response of the amplifier is necessary. Better measure of the phase linearity is group delay, which have to be constant over the operation bandwidth as much as possible. For best pulse shape, transfer functions near to standard filter approximations Gaussian or Bessel are needed at amplifiers or at other signal processing blocks [2].

This paper describes selected important points of the design and testing of solid state detector amplifier. Two approaches are presented, the first, standard lumped components are used and the priority was in an amplitude response and maximum operation bandwidth and the second, better phase response was obtained using special broadband inductors.

II. AMPLIFIER CONNECTION BASICS

The simplified schematic of the single chip amplifier is in Fig. 1. It consists of the amplifier chip AMP, coupling capacitors C and bias networks (bias tees) L, Cb. The input bias network is often integrated on the chip and the output one is used for the power supply connection.

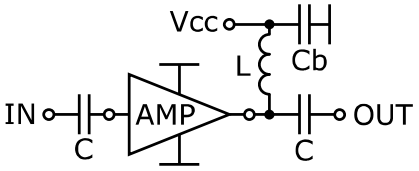

Figure 1. Simplified schematics of the single chip amplifier.

There are some basic rules of thumb about coupling capacitors and inductors used [3]. Capacitors should have a low reactance at the lower corner frequency when the amplifier has to operate, in range 1 to 10 Ω. The similar rule says inductors should have reactance about 200 - 500 Ω on the same frequency.

Broadband amplifiers have a problem with parasitic resonances of components. Ideally, components where the resonances are above the maximal frequency of operation should be selected, but this is not easy for too big bandwidth. In the case of correct damping, parasitic resonances will be hidden and will not distort the frequency response of the amplifier.

The goal of the design is the matching the transfer characteristics of the amplifier chip together with bias network and capacitors to application demands.

III. MULTI-STAGE LC NETWORK

The first design of the amplifier was done as multi stage LC network based on [4]. Two prototypes were built with different amplifier chips, the ABA-53563 (pr. 1) and the MGA-53589 (pr. 2), both AVAGO. Both networks were designed and tested in the circuit simulator and then tuned into the best performance as prototypes. The flat amplitude response with bandwidth as large as possible was desired. The ideal would be to maintain amplitude response similarly to the original chip shape given by the manufacturer. The common schematic diagram of the multistage output LC bias network is shown in the Fig. 2.

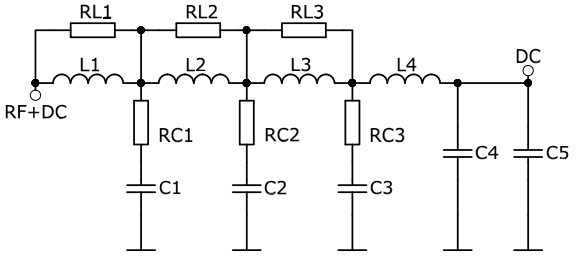

Figure 2. Schematic diagram of a multi-stage LC output bias tee.

The circuit has three resonant frequencies, spaced in multiples of number between 2 and 3. Final values were 120 MHz, 410 MHz and 970 MHz. Biggest frequency is affected mainly by components nearest the RF path, L1 and C1. All resonant peaks are made flat by adding resistors, which decreases a quality factor of L and C components. At capacitors, very low Q_C was set, between 0.02 and 0.03. At inductors, Q_L values were 40, 32 and 24, the smallest value was for 970 MHz at the beginning of the network (L1). As coupling capacitors, 1 nF were used. The final amplitude response of the RF path is in Fig. 3. One can see the useable bandwidth from 10 MHz to 3 GHz is below 1 dB amplitude error.

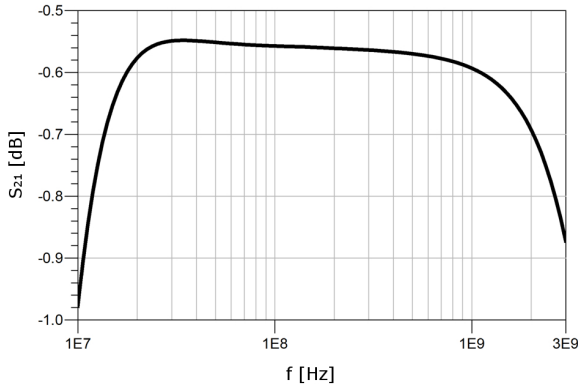

Figure 3. Simulated amplitude response represented by S_{21} of the multi-stage LC network RF path.

Amplitude responses of two amplifier prototypes are in Fig. 4, ABA-53563, prototype 1 and Fig. 5 MGA-53589, prototype 2 respectively, both in comparison with chip response given by AVAGO. The first chart in Fig. 4 shows unfinished resistors tuning, there are still three visible -6 dB drops. Operation bandwidth is from 6 MHz to 2.5 GHz, and maximal gain is 21 dB, is in a range of <1 dB below maximal gain given by AVAGO.

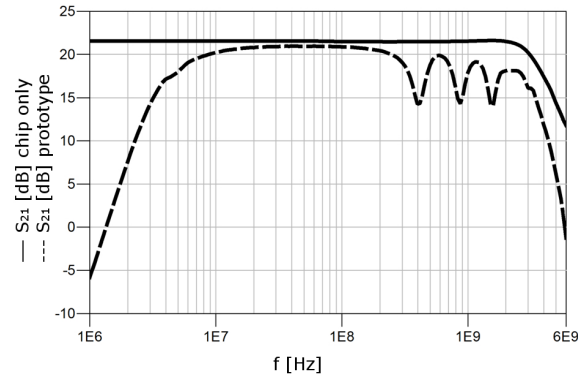

Figure 4. Comparison of amplitude responses of the ABA-31563 prototype 1, using multi-stage LC network with response given by the manufacturer. Resistors tunig is not finished.

The second prototype amplitude response with the MGA-53589 has more ragged shape due to chip parameters. Maximal gain achieved is approximately 25 dB, at 2 GHz there is a 10 dB drop. Data are valid above 8 MHz, below this frequency only the extrapolation is shown.

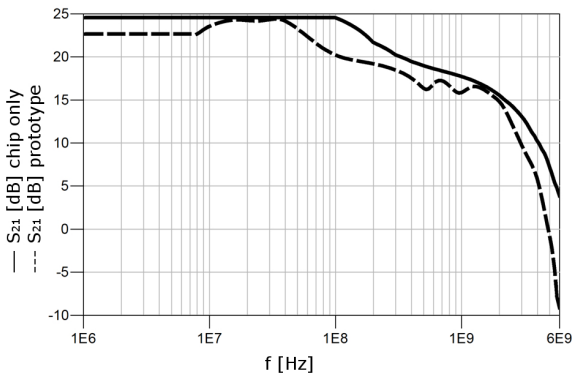

Figure 5. Comparison of amplitude responses of the MGA-53589 prototype 2, using multi-stage LC network, with response given by the manufacturer. Data are valid above 8 MHz.

The non-flat amplitude response was not the main problem in the first design. When tested on pulse signals, there was a big distortion in the output signal and a gain was significantly lower. Step responses of first amplifiers obtained from measured S_{21} are in Fig. 6. Both amplifiers consist of two stages, which are populated by the same chip, and bias network.

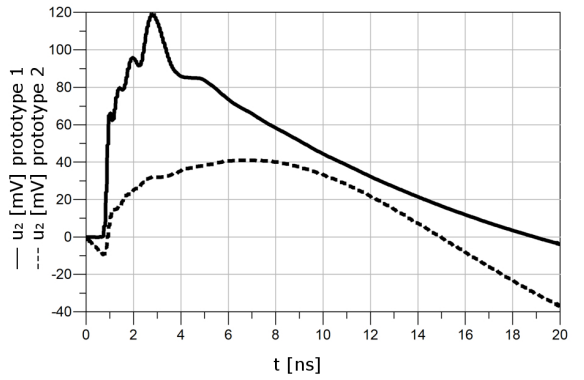

Figure 6. Step responses of both first set prototypes. Note the big distortion and low gain (pr. 1: ABA-53563, pr. 2: MGA-53589).

The last figure, Fig. 7, shows the group delay computed from prototypes 1 and 2 measured S_{21}. One can see the shape is corrugated badly. Problem with pulse signal distortion and with group delay is solved in the next amplifier sets.

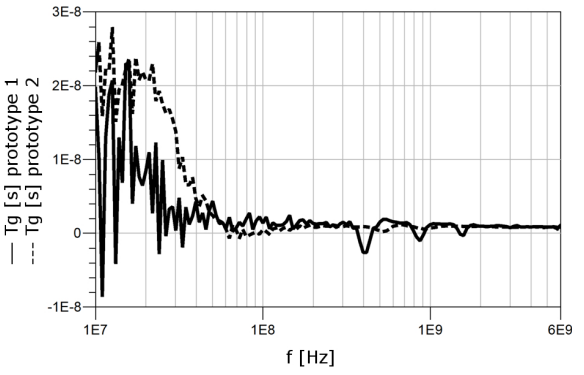

Figure 7. Group delay of the first set prototypes. The ripple is very high, especially on lower frequencies.

IV. BROADBAND INDUCTOR

The first set of amplifiers suffered with distortion and lower gain when used for pulse signals. There were many components used in the output bias network. It leads to difficult tuning up and need of many component models. Some of these were wrong. Another approach used for the next amplifier set uses a special broadband inductor. The inductor replaces all the RF-DC branch in the output bias network [5], [6].

The broadband inductor is wound on a cone and its inductance is given by (1). There L_H is inductance of a helical (cylindrical) inductor, L_S is inductance of a spiral inductor and α is angle depending on real inductor construction, 0° for a cylindrical construction and 90° for a flat spiral coil construction.

$$L = \sqrt{(L_H \cdot \sin\alpha)^2 + (L_S \cdot \cos\alpha)^2} \qquad (1)$$

Inductance of the helical inductor in μH is given by (2), where coil height H in mm similar to the conical inductor and radius R mm, as an average of radiuses on both cone ends were assumed.

$$L_H = \frac{1}{25.4} \cdot \frac{(N \cdot R)^2}{9R + 10H} \qquad (2)$$

Finally, inductance of the spiral inductor in μH is done using (3). The R is same as in previous case and Win mm is a radius difference on both cone ends. All dimensions are highlighted in Fig. 8.

$$L_S = \frac{1}{25.4} \cdot \frac{(N \cdot R)^2}{8R + 11W} \qquad (3)$$

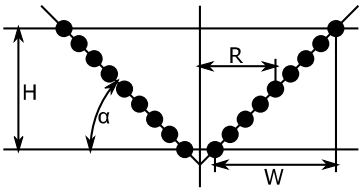

Figure 8. The broadband inductor dimensions.

Broadband inductors for the second amplifier set were designed to L = 500 nH. They were wound on 4 mm non ferromagnetic core in length 14 mm. The inductor in measurement setup is in Fig. 9.

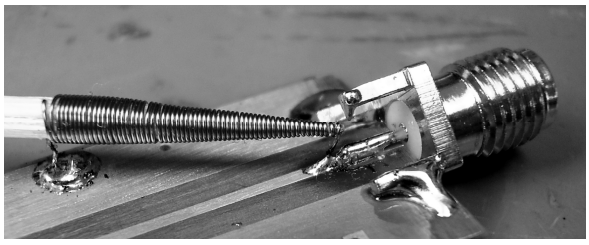

Figure 9. The broadband 500 nH inductor in the test fixture.

Final parameters of the broadband inductor are in the Fig. 10, in comparison with ideal inductor 500 nH. The measured inductor was connected in shunt configuration between ground and the 50 Ω transmission line. The difference is very small, below 0.8 dB in S_{21} up to 8 GHz in this example.

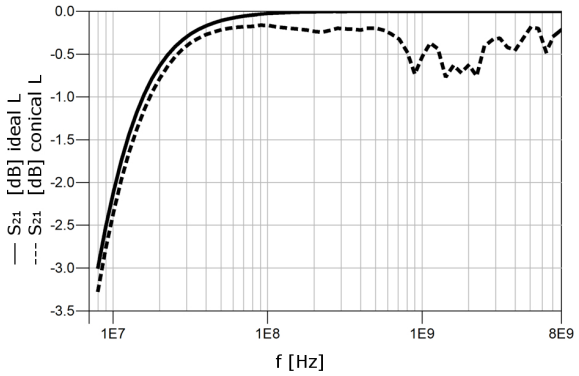

Figure 10. The measured S_{21} of boradband inductor in shunt configuration in comparison with ideal inductor 500 nH.

V. RESULTS WITH BORADBAND INDUCTORS

Two-stage amplifier prototypes, one with ABA-53563 amplifier chip (pr. 1) and one with MGA-53589 (pr. 2) were modified to use broadband inductors instead the output bias network. The comparison of real measured S_{21} with chip only S_{21} is in Fig. 11 and Fig. 12 for both amplifier prototypes.

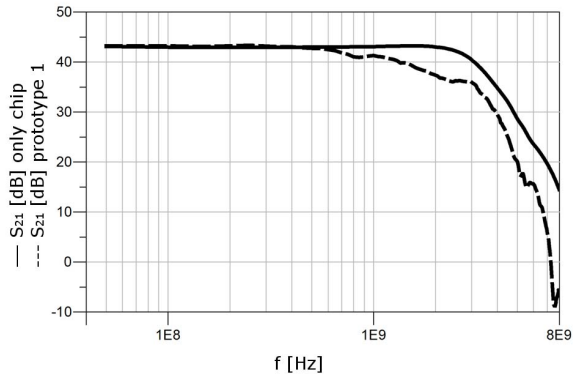

Figure 11. Comparison S_{21} of the amplifier prototype 1 using boradband inductor with chip only S_{21} given by the manufacturer.

One can see the drop in S_{21} on low frequencies at prototype 2. The chip parameters are defined above 100 MHz. Below this frequency, amplifier operation was on a risk.

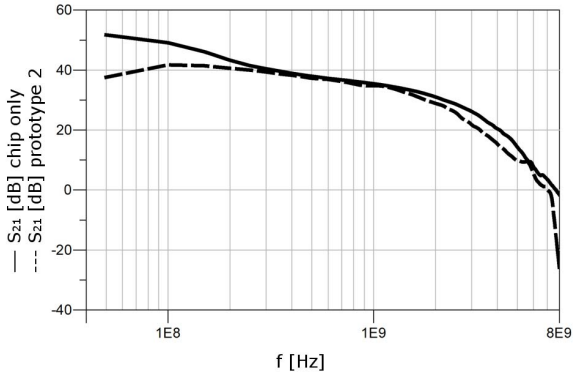

Figure 12. Comparison S_{21} of the amplifier prototype 2 using broadband inductor with chip only response from the manufacturer.

As at the first amplifier set, the group delay and the step response were analyzed. The group delay Fig. 13 has much lower ripple than at the first set, the drop at low frequencies at amplifier prototype 2 (MGA-53589) is only observed. The curve belonging to prototype 1 (ABA-53563) is very similar to ideal case.

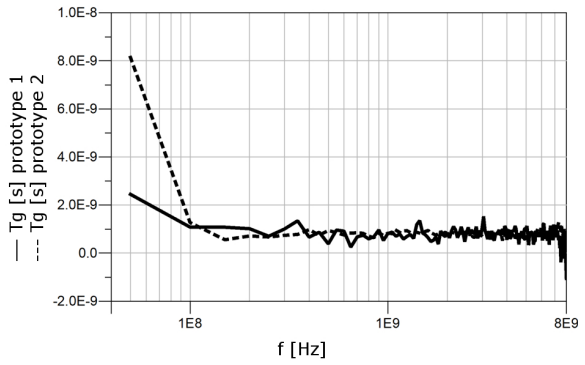

Figure 13. Group delay of second set prototypes. The ripple is much lower than at the first set.

Also the step response computed from the real measured data (Fig. 14) looks much better than at first amplifier set. The prototype 1 (ABA-53563) gives the best response with the steepest rising edge, gain in peak corresponding to the AC gain and pulse decay in accordance to the low frequency limit of the amplifier.

The prototype 2 (MGA-53589) gives better response than at first prototype set, but the curve is shifted below zero partially due to bad amplifier chip performance at low frequencies.

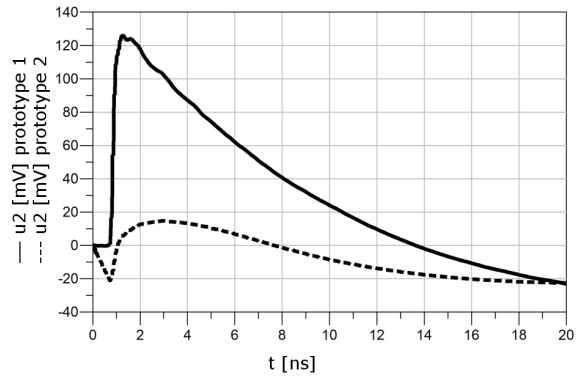

Figure 14. Step responses of second set prototypes. Distortion is much lower and gain is higher. Prototype 1 (ABA-53563) gives the best results.

VI. CONCLUSIONS

The best performance was measured at prototype 1 from second amplifier set. This version of the amplifier has used a broadband inductor 500 nH wounded on a conical non-ferromagnetic core in the bias network. The amplifier chip ABA-53563, used in a circuitry, has well defined parameters on low frequencies. It brings us good low frequency performance. Using this approach a 21 dB gain in one stage was obtained, 1 dB lower than AC value given by the chip manufacturer AVAGO. The 320 ps rising edge, measured from 10 % to 90 % of pulse amplitude, was another benefit of the design. For this part of design results are very good and well suitable for the final application.

The prototype 2 step response was also advanced by using the broadband inductor, but the performance is poor on low frequencies. The chip used in, MGA-53589 from AVAGO has not defined parameters at low frequencies and using it f below 100 MHz was experiment only.

Just another approach can be shown on a case of two amplifier sets designed, built and tuned up. When the low distortion in a time domain is desired, the flat amplitude frequency response of the amplifier is not most important goal of the design. Crucial parameters for the component selection and network construction, established from the design and experiments, are the linear phase response and the flat group delay.

The broadband inductor design and construction were also tested. Formulas stated above, derived for conical, cup shaped inductors were used for our sharp conical inductors. It was used for fast calculations of the broadband inductor inductance. Results were verified using the electromagnetic simulation and the measurement on several real samples. Simulation and measurement is needed also for obtaining resonant frequencies and their impact to final frequency response.

The final result of this part of work is verified successful design of amplifier optimized to minimal distortion in time domain. The rising edge 230 ps and gain 42 dB were reached.

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