Using VHDL-AMS to simulate aging behavior of electronic components

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***Abstract*: Reliability of electronics is in the automotive industry very important. The average age of cars in Germany was 9 years at 2015.[i] Normally the life time is evaluated by the environmental test according ISO 16750. The content of this paper is to contribute that computer simulation of aging is a possible way to evaluate electronic circuits in the define phase. For this reason a VHDL-AMS simulation models is used to model aging behavior of a resistor.**

Keywords: VHDL-AMS, aging, resistor

I. Introduction

The amount of electronics increases in the automotive sector in recent years rapidly and is expected to grow from the current 20% to 30% in 2020.[ii] The resulting rise in electronics not only increases the complexity, but also the possibility of a failure over the lifetime of a vehicle - usually up to 15 years. According to statistics from the German Federal Motor Transport Authority 37% of de-registered cars in 2014 were older than twelve years.[iii]

Thus, the vehicle user experiences no outages over the twelve years of life, extensive environmental testing is carried out; represent a sort of time-lapse over the lifetime. These tests are described in part in standards such as ISO 16750 or OEM specific specifications. However, since real tests represent only a sample, it is the objective of this paper to provide a contribution; the aging effects can be treated at an early stage through a computer simulation.

In the first step the examination of resistors is done in this paper.

II. Basics VHDL-AMS

VHDL-AMS is a standardized description language by the IEEE "for digital, analogue and mixed signal applications"[1]. It "support(s) the description of both behavior and structure"[1] Not only analogue and digital circuits can be described, but also complex systems from other areas of physics, such as the mechanics or thermodynamics. This is the reason why VHDL was chosen as a simulation language, because for further simulation it opens the opportunity also to include temperature dependencies.

VHDL-AMS is the abbreviation for "VHSIC Hardware Description Language - Analogue and Mixed Signal, where VHSIC for Very High Speed Integrated Circuit"[2] "VHDL-AMS is an informal name for the combination of the IEEE standards: VHDL 1076-1993 and VHDL 1076.1-1999.[1].

"VHDL-AMS is the result of an IEEE effort to extend the VHDL language to support the modelling and the simulation of analogue and mixed-signal systems."[3] It uses differential algebraic equations to describe different systems.[4]

VHDL AMS allows a top-down approach. It can be described at a system level (high abstraction level), without knowing the details already. For this purpose, in the **entities** (interfaces) are specified. When a detailing of the function is happening in the continued later development process, this is mapped in the **architectures** further in a refined or detailed way.

The functionality in the architectures can either be described by the structure or the behavior. "It may be coded using a structural style of description, a behavioral style, or a style combining structural and behavioral elements". [4]
With the modular design it is also possible to reuse the models and thus to create a comprehensive simulation environment and libraries.

III. Aging Simulation Concept

The proposed simulation concept of aging is to compose an aging function and wrap the existing model into it. The idea is described in a figure 1.
Any MODEL specified and compatible with given simulator is instantiated (first PORT MAP) in MODEL_AGING architecture. The necessary libraries and parameters are declared. The second component in architecture is AGING_FUNC which is instantiated just after the MODEL_AGING instantiation. The output of MODEL (shared_par) is passed to AGING_FUNC which represents the aging behavior and stored back in shared_par. An output from the AGING_FUNC is the final result we need for aging analyses.

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```
LIBRARY IEEE;
USE IEEE.ELECTRICAL_SYSTEMS.ALL;
use work;

ENTITY MODEL_AGING IS
GENERIC(
        PARAM1 : real := 1.000000;       -- AS MANY
PARAMS AS NEEDED
        PARAM2 : real := 1.000000);
PORT(
        TERMINAL P : ELECTRICAL;
        TERMINAL N : ELECTRICAL);
END ENTITY MODEL_AGING;

ARCHITECTURE BHY OF MODEL_AGING IS

  -- Signals
  signal shared_par : real;

        BEGIN
  MODEL_inst : entity work.MODEL
    GENERIC MAP
        (PARAM_A1 => PARAM1,
         PARAM_A2 => PARAM2)
    PORT MAP
        (
         P => P,
         N => N,
         value => shared_par
         );

  AGING_inst : entity work.AGING_FUNC
  GENERIC MAP
      (PARAM_B1 => 1.0,
       PARAM_B2 => -1.0,
      )
  PORT MAP
     (
      aged_value => shared_par
     );

END ARCHITECTURE BEH;
```

Figure 1. The aging concept VHDL AMS code

The concept was applied on a simple resistor. Physical reason for aging dependencies lies in “stress relief, internal oxidation, and perhaps precipitation are dominant mechanisms in producing resistance change”[5] There is not a general formula which describes these mechanisms. So investigations from earlier papers like “aging Behaviour of commercial thick-film resistors” were used.

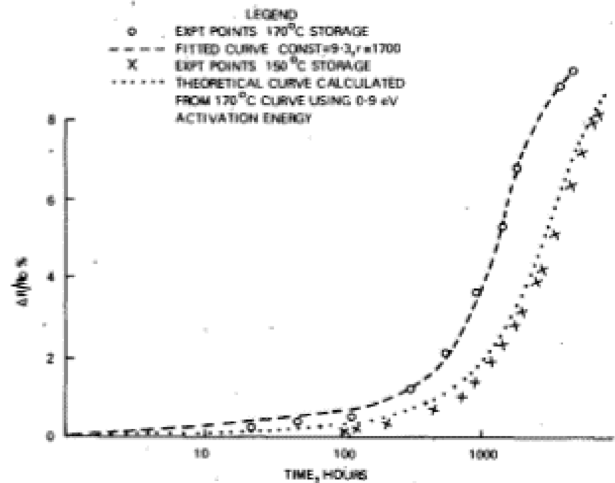

Figure 2. Thick-Film Resitors change over time [8]

IV. Resistor Aging Simulation

a) Generate mathematical model of aging

The standard model of a resistor AGING_FUNC is extend by the result of Sinnadurai. In order to get the coefficients of the proposed formula following approach was chosen (see equation 1.1).

$$\frac{\Delta R}{R_0} = a * \left(1 - e^{\frac{-t}{b}}\right) \qquad \text{equation 1.1}$$

In the first step a table was created to get pairs of data out of the diagram. The original diagram is a semi logarithmic diagram and it looks different in a linear scale.

In the next step the curve fitting toolbox from Matlab was used to calculate the missing coefficients (see figure 2). This gave following results:

a= 409.6

b=2.495e+05.

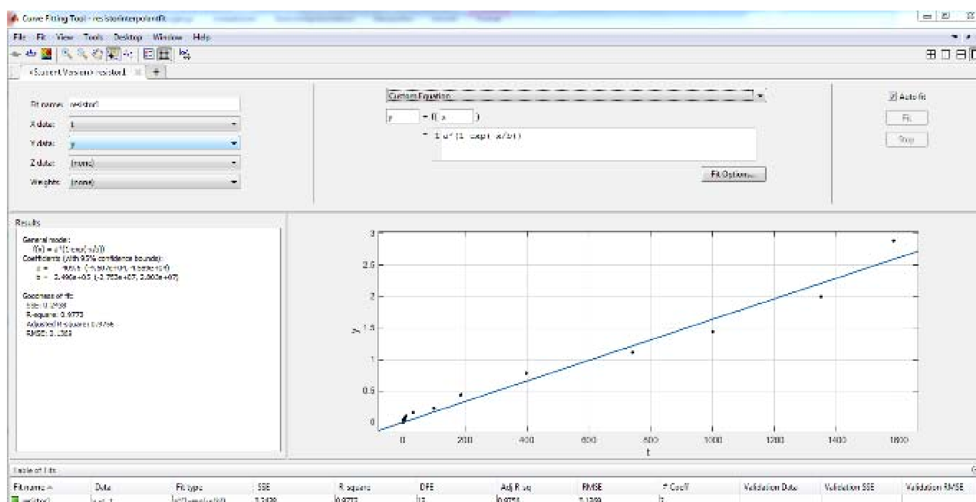

Figure 2. Curve fitting toolbox from Matlab to find the coefficient

On the other hand an evaluation through the numerical fit results can be done, by using [6]
a) 95% confidence bounds of the fitted coefficients is used by the toolbox
b) Goodness of fit statistics, here the SSE (sum of squares due to errors) and the adjusted R-square statistic are the best indicator to evaluate the fitting.

b) Generate Simulation model

At the beginning a simple test bench structure was defined in which the aging resistor model behaviour is checked out. In order to read the changes of the resistor we have to do the voltage measurement. A simple current source and aging resistor was used. (see figure 3)

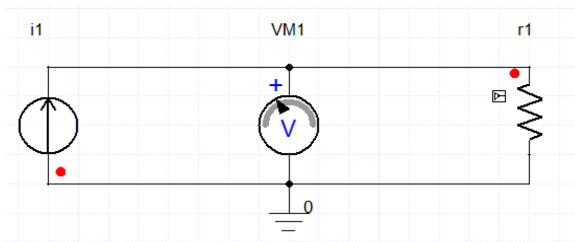

Figure 3. Simple Test Bench for ideal resistor aging model

Different approaches to modelling of aging function were tested. In the first approach to simulate the time dependency the attribute time'pos (now) was used. And as the original unit of time was in ns a correction by dividing with 3600 10E-9 was necessary. And it works only for small simulation times in the ms area because of data types used. After increasing the simulation time to 1500 hours the simulator could not converged and stopped with an error.

In a second approach the e-function was approximated by a polynomial function, which would be not so accurate but close to the original function.
Here the problem occurred that the accuracy of the solver found its limits, so it responded for example with a negative number, which should be positive.

The final solution was simulating the time with a one additional counter. For this reason a process was included with the “Wait until” statement. A process was necessary to get a sequential behavior and to use the wait function. The wait until function waits to the specified time. As if it is a continuous curve it is okay and the accuracy can be increased by lowering the constant “waiting time”. Another problem than was observed, because the used variables could not be transferred to main architectural behavior, because they are only valid inside the process. To solve this problem a signal “sigRvar” was introduced, because with signals a communication to the rest of the architecture is possible. The process is actually aging function and it was turned into an entity agingfunc to be usable not only by one component. The library model of ideal resistor was used as an aging component.
In Figure 4 is the VHDL Code for this solution.

```
LIBRARY IEEE;
USE IEEE.ELECTRICAL_SYSTEMS.ALL;
USE IEEE.MATH_REAL.ALL;
ENTITY          aging_func IS
  port
                (
                 aged_value : out real
                );
END ENTITY aging_func;

ARCHITECTURE arch_aging_func OF aging_func
IS
CONSTANT Ragingcoeffa: real := 409.6;
CONSTANT Ragingcoeffb: real := 2.495e+05;
CONSTANT Rstart: real := 1.0e+03;
SIGNAL    sigRvar: real :=0.0; -- signal which is
modifided in process p1

BEGIN
  P1: PROCESS
    VARIABLE B : boolean := false;
    VARIABLE zeit : integer :=0;
         BEGIN
         WAIT for 1 hr;    -- optional time
         zeit := zeit+1;
         sigRvar<=Rstart*Ragingcoeffa*(1-exp(-
         real(zeit)/Ragingcoeffb));
         Assert B
         report "time ="& integer'image(zeit) & "h
" &" sigRvar in process = "&real'image(sigRvar)
         severity note;
         end PROCESS;
aged_value <= sigRvar;
END ARCHITECTURE arch_aging_func;

-- VHDLAMS MODEL aging_res --
LIBRARY IEEE;
USE          IEEE.ELECTRICAL_SYSTEMS.ALL;

USE SIMPLORER_ELEMENTS.ALL;
ENTITY          aging_res IS
PORT(
         TERMINAL P : ELECTRICAL;
         TERMINAL N : ELECTRICAL);
END ENTITY aging_res;

ARCHITECTURE arch_aging_res OF aging_res IS
  signal shared_par : real;

BEGIN
    MODEL_inst : entity R
      PORT MAP
           (
            P => p,
            N => m,
            R => shared_par
            );

   AGING_inst : entity AGING_FUNC
```

```
    PORT MAP
        (
         aged_value => shared_par
         );
END ARCHITECTURE arch_aging_res;
-- END VHDLAMS MODEL aging_res -
```

Figure 4.Simple VHDL AMS Model of a aging resistor

For the simulation 2000 hours are used and the results is shown in figure 5. Here the differnce to the linear time is used to show the effect of the aging model.

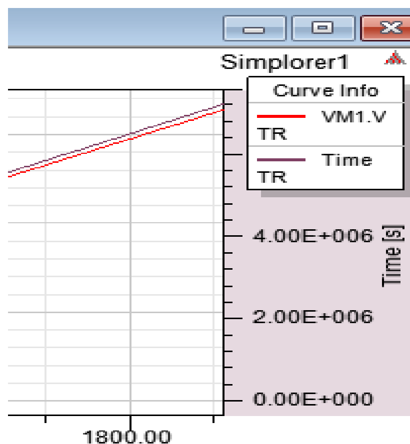

Figure 5: Simulationresults of resistor aging model compared with the linear time

V. Aging Models with PSpice

A. Aging model in PSpice

"Pspice is known as a powerful general purpose analog circuit simulator that isused to verify circuit designs and to predict circuit behavior."[9] PSpice models are very widely used. PSpice is based on a netlist and reliability simulator with work on spice require a 2nd run. "This requires that before running an aging analysis, a circuit simulation is needed to obtain the operating points of all the nodes in the circuit."[10] For example this method is used in the Berkeley Reliability Tool (BERT) [11]

Especially for semiconductors aging models exist, which try to simulate the hot carrier degradation effect [12].

B. Using PSpice models in VHDL-AMS

As some aging models exist it would be worth to consider the possibility to use PSpice models in VHDL-AMS. In general this is possible to import PSpice models with the ANSYS Simplorer under the Project tools you can choose Spice files.

IV. Conclusion

This work has shown that real effects of aging can be simulated via simulations. This work is intended to encourage future work in this field, to investigate the aging effects of other electronics components. The aim is to build up the library of aging models composed from existing models and different aging functions and to use the simulation as an additional method for assessing the effects of aging.

Further it was shown, that it is possible to use VHDL-AMS to simulate not only resistor aging effects and extend that methodology to other components.

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