Output Voltage and Efficiency of Novelty Architecture of Charge Pump versus Clock Frequency and MOSFETs Sizes

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***Abstract* – Charge pump is circuit that produces voltage higher than supply voltage or negative voltage. Today, charge pumps became an essential parts of electronic equipment. The integration of charge pumps directly into the target system allows manufacturers to feed a complex system with many specific power requirements from a single source. However, charge pump efficiency is relatively small. This paper is devoted to questions of efficiency of presented variant of charge pump. Thus efficiency as dependence on number of stages, clock frequency, output current and MOSFETs sizes of presented charge pump was simulated. The aim of this study is determination of MOSFETs sizes and theirs influence to efficiency and output voltage. Complex optimization of this circuit will follow in the next period.**

Keywords-2-phase Charge Pump; efficiency; switch size determination.

I. INTRODUCTION

Generally known variant of charge pump is Dickson Charge Pump (DCP) [1]. Design rules for DCP are summarized in [2]. The differential voltage ΔV between nodes n and $n+1$ is

$$\Delta V = V_{n+1} - V_n = V_E - V_T \tag{1}$$

where V_E is voltage gain, V_T is threshold voltage.

Value of voltage gain decreased by stray capacitance of node as follows

$$V_E = \left(\frac{C_T}{C_T + C_S} \right) \cdot V_{CLK} \tag{2}$$

where V_E is voltage gain, C_T is transfer capacitance, C_S is stray capacitance, V_{CLK} is amplitude of clocks.

Since the output voltage applies according

$$V_{OUT} = V_{IN} + N \cdot \left(V_E - V_T \right) - V_T \tag{3}$$

where V_{OUT} is output voltage, V_{IN} is input voltage, N is number of stages, V_E is voltage gain, V_T is threshold voltage.

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The threshold voltage of used transistors has usually cardinal effect to resulted value of the output voltage. This parameter limits the DCP implementation, especially for supply voltage lower than *1 V*. Therefore, sub-volt applications must use other circuit solutions of charge pumps [3], [4].

Generally used principle for the threshold effect suppression is a change of connection of the transfer transistor from diode mode to switch mode [5], [6], [7]. For this solution, voltage drop between two nodes is decreased from the threshold gate-source voltage to the saturation voltage of channel, only.

II. PRESENTED VARIANT OF CHARGE PUMP

Presented variant of charge pump [8] uses 2-phase clocks. One cell of this charge pump is shown in Fig. 1. The cell consists of five transistors (M_1 to M_5) and transfer capacitor (C_T).

This block is driven by clock signals according to Fig. 2.

In the first phase (CLK1 = V_{DD}, CLK2 = V_{DD}), transistors M_1, M_3 and M_5 are closed. Thus transfer capacitor C_T is biased to supply voltage V_{DD}.

In the second phase (CLK1 = GND, CLK2 = GND), transistors M_2 and M_4 are closed. Thus transistor M_2 holds bias transistor M_5 in disconnected state. Transistor M_4 connects the transfer capacitor C_T between input and output of cell. Therefore, input voltage is increased by a voltage of transfer capacitor from previous (biased) phase.

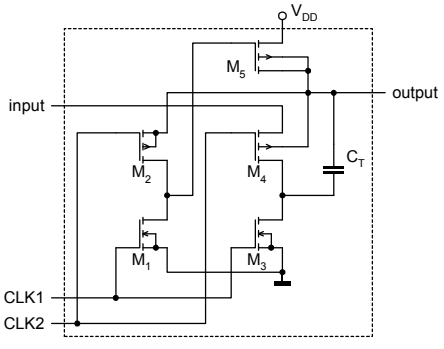

Figure 1. One cell of proposed charge pump [8].

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In the last phase (CLK1 = GND, CLK2 = V_{DD}), all transistors are opened.

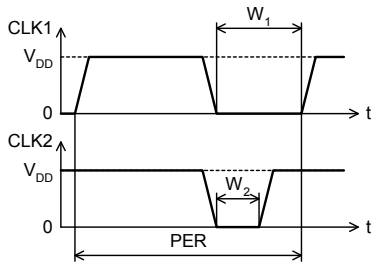

Figure 2. Waveforms of 2-phase clocks.

Driving clocks from Fig. 2 have overlapped character. Symbols W_1 and W_2 mark width of pulses both clock signals. *PER* is period. The optimal values of W_1, W_2 were estimated in previous period [8].

III. Design Algorithm

The design rules for estimation of parameters of presented charge pump is summarized to undermentioned steps. We consider these charge pump specifications:

- Power supply voltage V_{DD} = 0.7 V, minimal steady output voltage V_{OUT} = 4 V,
- Output load capacitance C_L = 300 pF, output current I_L = 4 µA,
- Maximal output voltage ramp-up time t_r = 150 µs.

A. The number of stages

Number of stages N was calculated as ratio of output voltage V_{OUT} and voltage gain of one stage V_E. Result value had to be an integer:

$$N = \frac{V_{OUT}}{V_E} = \frac{4}{0.7} = 5.714 \doteq 6 \tag{4}$$

B. The clock frequency

Initial clock frequency was selected as $f_{CLK} = 20\ MHz$.

C. The size of transfer capacitor

Value of transfer capacitance C_T we calculated from known load capacitance C_L, number of stages N, ramp-up time t_r and clock frequency f_{CLK} [2]:

$$C_T = C_L \frac{N}{t_r \cdot f_{CLK}} = \\ = 300 \cdot 10^{-12} \frac{6}{150 \cdot 10^{-6} \cdot 20 \cdot 10^{6}} = 0.6\ \text{pF} \tag{5}$$

D. The W/L of used transistors

The MOSFETs M_3 to M_5 and M_D are used for transfer charge. Thus these transistors should have conductance at least ten times higher than conductance matched to the output current [2]. Initial size of these MOSFETs must be estimated from I-V characteristics, only.

The MOSFETs M_1 to M_2 cause losses of charge, but these MOSFETs are used for driving transistor M_5 only. Therefore, these MOSFETs must be designed relatively narrow.

Parameters of used transistors are summarized in Table I.

TABLE I. Parameters of Transistors

Transistor	W (µm)	L (µm)	model
M_1	0.2	0.1	nmos_hvt
M_2	1	0.1	pmos_hvt
M_3	0.5	0.1	nmos_hvt
M_4	2.5	0.1	pmos_hvt
M_5	2.5	0.1	pmos_hvt
M_{CT}	30	10	nmos_hvt
M_D	20	0.8	nmos_na18v
M_{BUFA}	5	0.1	nmos_hvt
M_{BUFB}	12.5	0.1	pmos_hvt

Transfer capacitor C_T is realized as transistor M_{CT} (we do not use MIM capacitors), thus capacity of this MOSFET must be calculated from derivation of I-V characteristics.

M_{BUFA} and M_{BUFB} are used as clock buffers. Models nmos_hvt and pmos_hvt correspond to "high voltage" transistors with relatively high value of V_T. Model nmos_na18v corresponds to native transistor for 1.8 V technology.

Estimated area of chip for realization of proposed charge pump is listed in Table II, where N is number of stages, A_{STAGES} is area for realization of stages, A_{BUFDET} is area for realization clock buffers and output detector, A_{TOTAL} is area for realization proposed charge pump with required number of stages.

TABLE II. Estimated Area for Realization of Charge Pump

N	A_{STAGES} (µm²)	A_{BUFDET} (µm²)	A_{TOTAL} (µm²)
1	469	30	499
2	998	30	1028
3	1497	30	1527
4	1996	30	2026
5	2495	30	2525
6	2994	30	3024

IV. Study of Clock Frequency Influence to Efficiency and Output Voltage

The aim of this part of simulations is to determine the influence of clock frequency to efficiency and output voltage.

Block diagram of simulated charge pump is shown in Fig. 3. It is 6-stage charge pump (N=6). For other cases, number of stages are changed, only. Both clock signals are buffered by invertors with strong output stage. The last stage is a diode detector based on transistor M_D. Output load is modeled by resistor R_L and capacitor C_L. Presented charge pump was powered from $V_{DD} = 0.7\ V$ and both clock signals had the same amplitude $0.7\ V$, too. Symbol I_S marks consumed current. Output voltage at load is marked V_{OUT}.

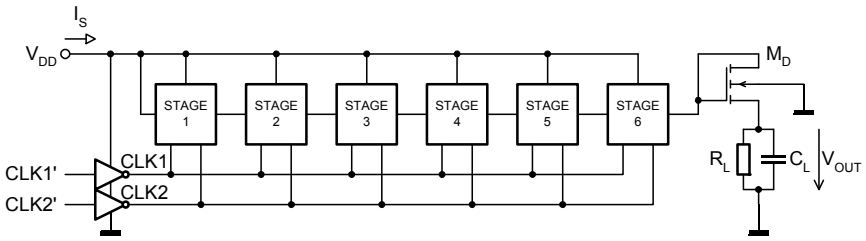

Figure 3. Simplified schematic diagram of simulated charge pump for N=6.

Number of stages N was varied from 1 to 6, clock frequency was set to values 10, 13.3, 20, 27, 40 MHz.

Efficiency and output voltage dependency to the clock frequency and output current I_L are shown in Fig. 4 and Fig. 5.

Total efficiency calculates by (6)

$$\zeta = \frac{V_{OUT}^2}{V_{DD} \cdot I_S \cdot R_L} \cdot 100\,\%, \qquad (6)$$

where V_{OUT} is output voltage, V_{DD} is power voltage, I_S is consumed current, R_L is output load.

Efficiency was varied from 38.47 % at frequency 10 MHz to 28.64 % at frequency 40 MHz for nominal value of output current $I_L = 4\ \mu A$. For the same conditions, output voltage varies from 3.741 V to 4.051 V.

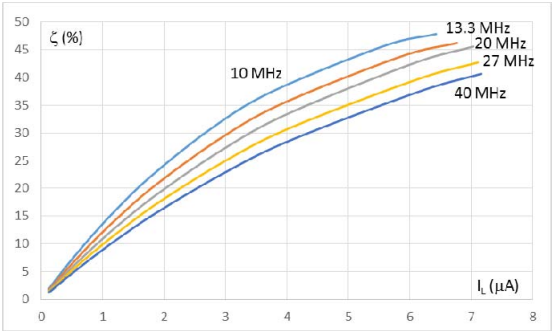

Figure 4. Efficiency as function of I_L for N=6.

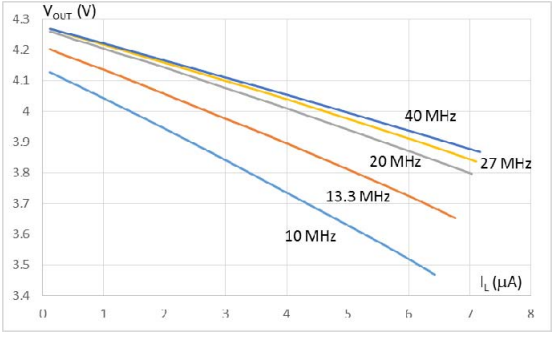

Figure 5. Output voltage as function of I_L for N=6.

Simulation results for other number of stages (N varies from 1 to 6) of charge pump are summarized in Table III.

TABLE III. EFFICIENCY AND OUTPUT VOLTAGE FOR VARIOUS NUMBER OF STAGES AT OUTPUT CURRENT 4 μA

N	ζ(%)	V_{OUT} (V)
1	69.53 to 59.33	1.275 to 1.290
2	64.63 to 43.26	1.919 to 1.950
3	60.06 to 47.07	2.540 to 2.590
4	53.75 to 42.02	3.130 to 3.120
5	47.79 to 37.30	3.638 to 3.762
6	37.47 to 28.64	3.671 to 4.051

V. MOSFETs Size Influence to Efficiency and Output Voltage

The aim of this part of simulations is to determine influence of MOSFETs size to efficiency and output voltage. Thus sizes of all transistors were swept, but only one parameter was changed in one time, other sizes according Table I were left unchanged. Output load was set to constant value $R_L = 1$ MΩ. These simulations were performed for 6-stage charge pump only.

Next, the six variants of simulations are performed to determine influence of transistor dimensions.

Variant #1: widths of transistors M_4 and M_5 were swept from 0.5 μm to 50 μm. The sizes of these transistors has the key influence to output voltage and efficiency, see Fig. 6.

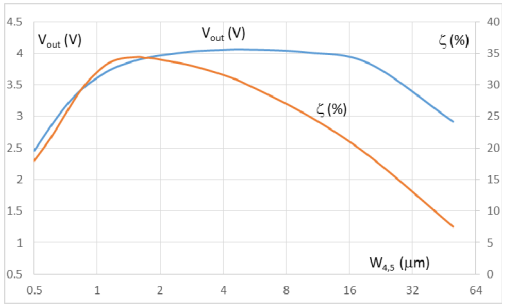

Figure 6. Variant 1: Efficiency and output voltage as functions of $W_{4,5}$.

Variant #2: width of detector M_D was swept from 0.5 μm to 50 μm. The size of this transistor has primarily influence to the efficiency, see Fig. 7.

Variant #3: width of transistor M_3 was swept from 0.2 μm to 10 μm. The size of this transistor has primarily influence to the output voltage, see Fig. 8.

Variant #4 and #5: widths of transistors M_1 and M_2 were swept from 0.2 µm to 10 µm or from 0.2 µm to 20 µm respectively. It is clear evident that transistors M_1 and M_2 must be narrowed, see Fig. 9.

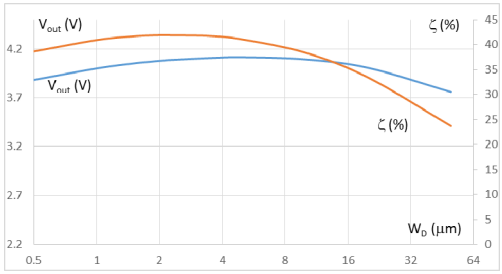

Figure 7. Variant 2: Efficiency and output voltage as functions of W_D.

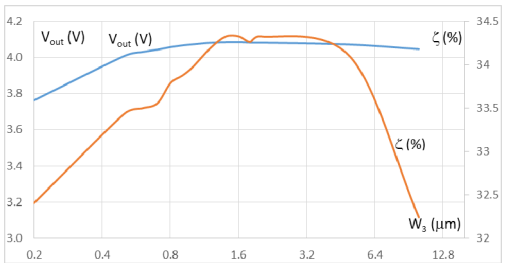

Figure 8. Variant 3: Efficiency and output voltage as functions of W_3.

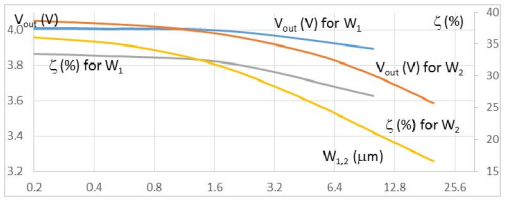

Figure 9. Variant 4, 5: Efficiency and output voltage as functions of $W_{1,2}$.

Variant #6: width of transistor M_{CT} was swept from 6 µm to 60 µm. The optimal size of this transistor is a compromise between efficiency and output voltage, see Fig. 10.

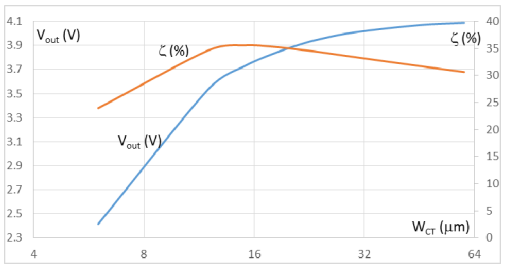

Figure 10. Variant 6: Efficiency and output voltage as functions of W_{CT}.

Variant #7: width of transistor M_{BUFA} was swept from 1 µm to 20 µm and simultaneously width of transistor M_{BUFB} was swept from 5 µm to 100 µm. Maximal value of efficiency $\zeta = 33.67\ \%$ for $V_{OUT} = 4.006\ V$ occurs for $W_{BUFA}=1\ \mu m$ and $W_{BUFB}=5\ \mu m$. This variant isn't plotted, because differences of values of efficiency and output voltage were relatively small.

VI. Conclusion

Study of efficiency and output voltage versus clock frequency and MOSFETs sizing for proposed charge pump was performed. Results from this study can be used for complex optimization study performed in the next period.

Parameters of MOSFETs and clock scheme were chosen according to previous study [8]. Analysis were performed by Eldo simulator version 2010.2b from Mentor Graphics Corporation.

From the first part of simulations we can see that the efficiency increases with increasing load current and decreasing clock frequency. And reversely, the output voltage increases with decreasing load current and increasing clock frequency.

Results from the second part of simulations is the key for optimization efficiency of presented charge pump. Values of efficiency and output voltage are $\zeta = 33.43\ \%$ and $V_{OUT} = 4.008\ V$ for original sizes of MOSFETs according to Table I and load $R_L = 1\ M\Omega$.

The transistor sizing technique allows to improve the efficiency about ten percent. Dimensions of transistors M_4, M_5, M_D and M_{CT} have the key effect to efficiency, M_3 has important effect to the output voltage. Effect of other transistors has predictable character and we may neglect effect of size of these transistors.

The presented results are limited to pre-layout simulations only. The parasitic effects of higher orders (e.g. interlayer capacitance, metallic interconnection capacitance etc.) are neglected.

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