Towards Automatic Gain Control Low-Power Amplifier in 130 nm CMOS Technology

Lukáš Nagy, Daniel Arbet, Martin Kováč and Viera Stopjaková

Institute of Electronics and Photonics
Slovak University of Technology
Ilkovicova 3, 812 19 Bratislava, Slovakia
e-mail: lukas.nagy@stuba.sk

***Abstract*—The paper addresses the design of a bulk-driven variable gain amplifier (VGA) in 130 nm general purpose CMOS technology. The VGA is intended to be employed within a low-power automatic gain control (AGC) block, which requires an examination of possible gain setting approaches. The mentioned investigation as well as the evaluation and comparison of the obtained results are presented. The amplifier has been designed to work with the power supply voltage of only 0.6 V, which introduces a whole series of challenges and obstacles. However, it also eliminates one of the main problems associated with bulk-driven circuits – the latch-up effect.**

***Index Terms*—Automatic Gain Control, Variable Gain Amplifier, Bulk-Driven, Low-Power**

I. INTRODUCTION

The current trend of shrinking the minimum channel length of MOS transistors avails a tremendous scale of integration for digital circuits and also a higher operation speed for analog and RF circuits. However, it also introduces numerous drawbacks from the analog design point of view such as the necessity of low value of the power supply voltage, greater fabrication process variations, exponentially rising values of subthreshold leakage current and others [1], [2]. These phenomena negatively affect the dynamic range of processable input signal, noise properties, power supply rejection and other parameters, since the threshold voltage of MOS transistors does not follow the trend of supply voltage downscaling [3]. In addition, the lowered supply voltage also limits the implementation of conventional circuit topologies in analog IC design. Therefore, different approaches have to be applied for analog low-voltage and low-power circuits designed in deep sub-micron CMOS technologies in order to overcome mentioned challenges.

The presented work is based on so-called *bulk-driven* MOS transistor used as a basic building block instead of conventional gate-driven devices [4], [5]. The main advantage of bulk-driven transistors is the eliminated threshold voltage V_{TH} of the device and also their ability to work with so-called rail-to-rail voltage swing. Despite the fact that these circuits have been developed some time ago, their popularity has never reached the level of their gate-driven counterparts. Recently, a research in this area represents an attractive scientific topic.

The variable gain amplifier represents an electronic circuit with very broad spectrum of applications. Its main field of implementation has been predestined as a part of automatic gain control circuit, which is widely used in wireless communication, medical applications, RF circuits and many more. The amplifier gain can be modified within the given limits with various dependences on controlling voltage by means of an interposing block. This block is responsible for generating appropriate control voltage based on required gain dependence.

II. AUTOMATIC GAIN CONTROL

As the name suggests, the gain of the amplifier is expected to automatically modify in order to maintain the amplitude of the output signal at a constant level within a given range of the input voltage. This can be achieved by several techniques but each can be categorized into either *feedforward* topology or *feedback* topology [6]. Both approaches are described in the following sections of the paper.

A. Feedback topology

The feedback topology of AGC circuitry is depicted in Fig. 1. The block diagram consists of VGA along with the envelope detector and voltage comparator employed in the feedback loop. In this case, the actual

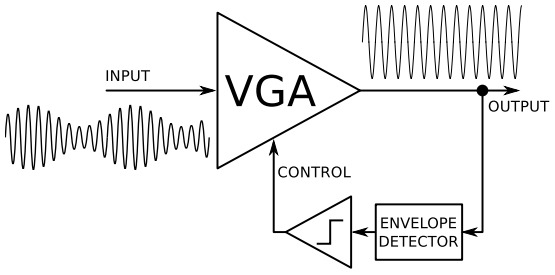

Fig. 1. Block diagram of the feedback AGC topology

output signal is sampled by the envelope detector and compared to the desired output voltage level. If the actual output amplitude is lesser than the required value, the VGA is set to the maximum gain. If the output voltage exceeds the set value, the gain is flipped into the minimum level. The main advantage of the feedback topology is in its simplicity. On the other hand, the feedback loop needs to be investigated because of delay and stability problems.

B. Feedforward topology

This kind of AGC represents rather interesting way of governing the output signal level. Fig. 2 depicts a block diagram of feedforward circuitry of AGC. The difference between feedforward and feedback topologies is apparent. The VGA is characterized by its

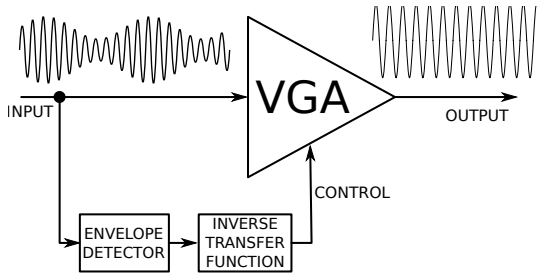

Fig. 2. Block diagram of the feedforward AGC topology

transfer function (gain vs. control voltage) that is the crucial parameter for this type of gain regulation. As one can observe, the input voltage is fed directly into the VGA as well as into the envelope detector, which creates a signal processed by the inverse transfer function generator. This block creates a controlling voltage defined by the desired output amplitude, a known transfer function of VGA and the actual input voltage. In this way, the gain of VGA is maintained simultaneously according to input amplitude changes. Furthermore, since this topology represents a direct opposite to feedback topology, there are no stability issues to tackle during the design period. On the other hand, the circuit complexity of inverse transfer function generator is quite high.

III. BULK-DRIVEN VARIABLE GAIN AMPLIFIER

As already stated, the proposed AGC circuit is based on bulk-driven VGA (BDVGA), which also represents the main block of whole circuitry. The AGC block has originally been designed for audio frequencies. The implementation of bulk-driven topology combined with an ultra low value of the supply voltage promise very low power dissipation and satisfactory gain, bandwidth as well as low distortion and noise parameters in audio spectrum.

The block diagram of the proposed BDVGA is shown in Fig. 3. Circuitry employs fully differential signal

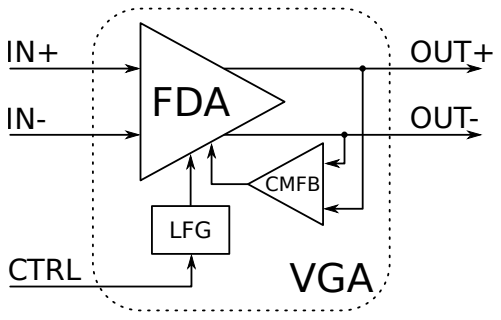

Fig. 3. Block diagram of the proposed bulk-driven VGA

processing due to severely limited voltage swing and required specifications. Mentioned methodology introduces increased circuit complexity but also greatly improves the dynamic range and noise properties of the whole system. The VGA consists of the fully-differential amplifier (FDA) with controllable gain, common-mode feedback (CMFB) circuit that is responsible for stabilizing and maintaining the operation point of the amplifier and finally, a circuit called LFG that defines the dependence of the whole VGA on the control voltage. In the following sessions, the main building blocks are described in details.

A. Fully Differential Amplifier (FDA)

The transistor level schematic diagram of the proposed bulk-driven FDA is depicted in Fig. 4. As already mentioned, the fabrication technology of interest is a general purpose twin-well 130 nm CMOS. Twin-well process enables using also NMOS transistors as bulk-driven devices, which is great advantage. The

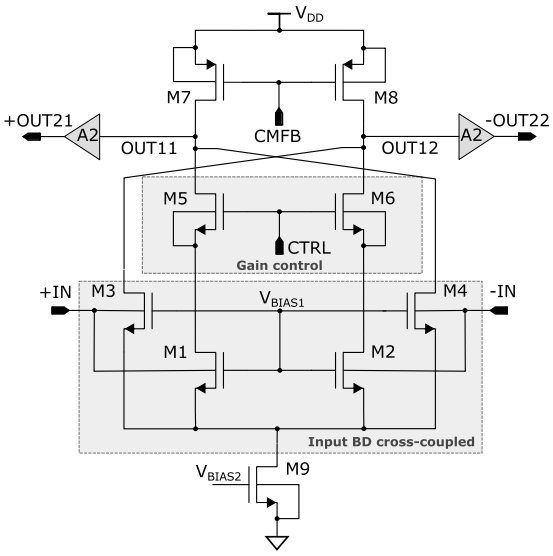

Fig. 4. Schematic diagram of the proposed bulk-driven VGA

power supply voltage is set to 0.6 V. Our research indicates that the whole system can reliably operate at this level of power supply. Devices M1 – M4 work as a bulk-driven cross-coupled differential structure. The presented cross-coupled connection introduces a high-gain capability for low-power and low-voltage amplifiers as well as rail-to-rail input signal range. All four devices have to be very precisely matched in layout representation.

Transistors M5 and M6 act as gate-driven current sources with the body-effect eliminated. This solution increases required silicon area since both transistors require their own deep N-well. However, the value of power supply voltage does not enable the use of conventional connection. Controlling voltage regulates the current flow into the differential pair M1 – M2, thus controlling its transconductance. MOS transistors M7 – M8 are implemented as a load structure for the differential part. So-called bulk-driven *negative resistance*

circuitry employed instead the proposed block would increase the overall gain. However, the sensitivity of this structure to PVT variations makes the presented solution more appropriate. The bias voltage for devices M7 and M8 is generated by the CMFB block.

The voltage gain of the differential circuit however, is not satisfactory, neither is its output voltage swing. Therefore, another amplifier stage has been introduced. Block A2 is a simple common-source amplifier circuit with its own CMFB signal, characterized by fixed gain and near rail-to-rail output voltage swing properties.

Common-mode feedback is widely used circuit in high-gain amplifier designs [6], [7]. Its main purpose is to prevent the common-mode output voltage from saturating to one of the supply rails, when input common-mode changes. However, the detailed explanation is not the scope of this paper. The designed CMFB blocks for the proposed VGA are presented in details in [8].

B. Linearity in dB scale

The dependence of the voltage gain of VGA on controlling voltage represents its transfer function. In our application, a linear dependence in dB scale is required. The research shows that decreasing gain with increasing controlling voltage is a more appropriate option. Accordingly to the mathematical definition, it represents an exponential dependence in linear scale.

The original transfer curve of the whole VGA has been used to create a desired linear-in-decibel dependence by means of automated spreadsheet. The required transfer function of the LFG block is depicted in Fig. 5. As one can observe, the transfer curve of the LFG is shaped as logarithmic function. Hence, the name of the block - Logarithmic Function Generator (LFG).

LFG output voltage can be generated by an analog circuit employing a single MOS transistor and converting its drain current into the voltage since the curve resembles the output characteristics of the transistor. This approach would require a stable biasing voltage, a precise I-V converter and nearly perfect fabrication process. Another feasible strategy is a usage of AD and DA converters and a simple combinational logic. In this way, the LFG promises less sensitivity to the PVT variations but on the other hand, the output voltage of the DA converter and hence, the whole LFG will be distorted. The amount of distortion is controllable by the number of bits the system works with. The optimum number of bits for our design is six, which gives resolution of 9.37 mV per bit that is roughly about 1.5% of V_{DD}.

The mentioned approach has been investigated further and has been described in VHDL and Verilog languages for simulation and synthesis purposes. The mixed-signal simulations with AD and DA converters modeled in Verilog-A and the respective synthesized combinational logic proved the feasibility and ability of the digital part to operate under mentioned power supply conditions. Our investigation also revealed that the used AD converter will have to be of so-called successive-approximation topology and the DA converter will be employing a popular M-2M ladder topology. The transistor level design of both blocks, however, is still in the development phase. The digitally generated LFG output voltage along with the ideal transfer curve and the actual linear-in-dB dependency are depicted in Fig. 5. One can notice logic hazards

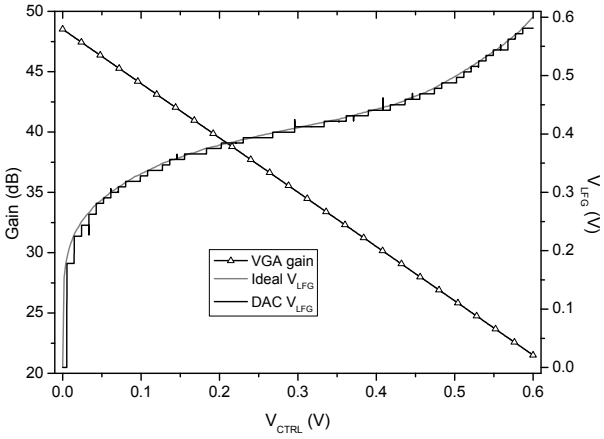

Fig. 5. The ideal and actual LFG transfer function along with the actual linear-in-dB dependence of VGA

present in the curve of the actual LFG transfer function as well as the fact that the VGA gain is almost ideally linear, which confirms the suitability of chosen circuitry. The tunable gain spans from 20.5 dB to 47 dB, which is satisfactory for a fully differential amplifier working with V_{DD} value of 0.6 V.

IV. TOPOLOGY COMPARISON

We have performed several simulation scenarios in order to verify the stability and functionality of the proposed AGC circuitry. Both AGC topologies were set up to maintain the output differential value of $\pm$ 150 mV, while the input differential voltage was represented by AM signal with the maximum possible modulation depth defined by the gain range of the VGA.

As mentioned above, the feedforward topology does not inherently introduce stability issues of the controlling part. However, various analyses endorsed it as inferior counterpart to the feedback approach. Even with idealized internal AGC blocks, the feedforward system exhibits worse parameters in terms of the output signal maintenance. The input and output differential waveforms of the feedback system along with the desired voltage value are depicted in Fig. 6. The output signal is successfully and quite precisely maintained around the desired value despite the fact that the input AM differential signal exhibits more than 90% modulation depth.

V. CONCLUSION

The paper presents an on-going development of the AGC loop designed in 130 nm CMOS technology employing a challenging bulk-driven operation of the VGA combined with ultra low-power supply voltage of 0.6 V. The design of VGA along with required CMFB circuit has proved to be very robust and stable even for

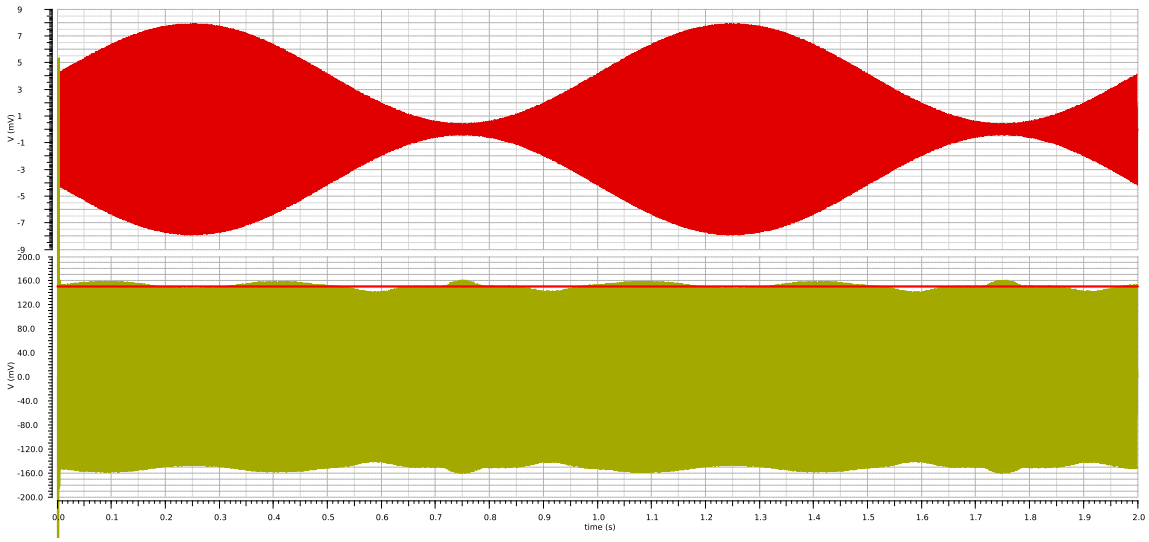

Fig. 6. Input differential AM stimulus along with desired level and actual differential output signal of the feedback AGC

constrained operating conditions. The worst-case (WC) power consumption of the whole VGA is P_{DISS} = 20.6 μW (typically P_{DISS} = 11.4 μW), the maximum spread of the gain due to PVT variations is Δa = 5.68 dB. The internal block responsible for shaping the dependence of VGA on the controlling voltage has been described in VHDL language, synthesized and incorporated into the design. The simulations have confirmed the overall stability and accuracy of the proposed LFG block.

The comparison of two different controlling approaches for achieving AGC functionality has been verified. The feedforward as well as the feedback topology have been modeled in Verilog-A language in order to enable further investigations and research directing in the future. The simulations have confirmed the minor stability issues in the feedback loop. However, the simplicity and accuracy in maintaining the desired voltage value (supported by the simulation results) makes it a better candidate for implementation into the whole AGC system.

ACKNOWLEDGEMENT

This work was supported by the Slovak Research and Development Agency under grant APVV-15-0254 and by the Ministry of Education, Science, Research and Sport of the Slovak Republic under grants VEGA 1/0823/13 and VEGA 1/0762/16.

REFERENCES

[1] Masuda, H. and Ohkawa, S. and Kurokawa, A. and Aoki, M., "Challenge: variability characterization and modeling for 65- to 90-nm processes," 2005, pp. 593 –599.

[2] Hasegawa, S. and et al, "A cost-conscious 32nm CMOS platform technology with advanced single exposure lithography and gate-first metal gate/high-k process," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, dec. 2008, pp. 1–3.

[3] K. K. Kim and Y. B. Kim and M. Choi and N. Park, "Leakage Minimization Technique for Nanoscale CMOS VLSI," *IEEE Design Test of Computers*, vol. 24, no. 4, pp. 322–330, July 2007.

[4] "0.4-V bulk-driven differential-difference amplifier," *Microelectronics Journal*, vol. 46, no. 5, pp. 362 – 369, 2015.

[5] G. Raikos, S. Vlassis, and C. Psychalinos, "0.5 V bulk-driven analog building blocks," *International Journal of Electronics and Communications*, vol. 66, no. 11, pp. 920 – 927, 2012.

[6] E. Kerherve and D. Belot, *Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers*, 2015.

[7] H. L. Chao, D. Ma, M. Koen, and P. Prazak, "Cmos low-power variable-gain cmfb-free current feedback amplifier for ultrasound diagnostic applications," in *Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian*, Nov 2006, pp. 427–430.

[8] Arbet, D. and Kovac, M. and Nagy, L. and Stopjakova, V. and Sovcik, M., "Variable-Gain Amplifier for Ultra-Low Voltage Applications in 130 nm CMOS Techniology," *International Convention on Information and Communication Technology, Electronics and Microelectronics*, 2016.