Readout Interface for Strip Detectors with Spectrometry Applications

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***Abstract* – In the present paper a preliminary design and implementation of a readout interface for strip detectors, using Applied Specific Integrated Circuits (ASICs) is discussed. Key issues are the parameters and features of the main constituent parts of the system: strip detectors, ASICs and driving electronics, as well as the preliminary test-results. The readout interface is intended to be used as a means to investigate the scope of strip detectors employed as spectroscopes in the area of experimental physics and their dynamic properties.**

Keywords-ionizing radiation; strip detector; front-end electronics; shaping time; spectroscopy; ASIC; FPGA; VHDL.

I. INTRODUCTION

Research on matter has been getting more and more attention in the last centuries. Important discoveries are challenging the scientific community to go deeper not only in the understanding of how matter is constituted but also in verification of many important theories which are pillars of the modern physics. Within the last few decades technological progress has made direct observation of subatomic particles a viable challenge. Thanks to major improvements in the semiconductor physics, nowadays we have several crucial tools for subatomic particle detection at our disposal, leading to several ground-breaking discoveries in major research institutions around the globe [1][2][3][4][5].

By now semiconductor detectors have become fundamental tools in applied physics. The *European Organization for Nuclear Research* (CERN) features semiconductor detectors (pixel and strip detectors) as the heart of detection within its accelerator [6][7]. The strip detectors, in general, have been an important part in experimental physics thanks to their versatility in terms of shape and size [7]; in addition strip detectors have an abundance of applications in physics, are low cost, and exhibit a good resolution and provide the possibility to keep the readout electronics away from the interaction region with its strong radioactive background.

Originally strip detectors were pure particle counting detectors however, using new generations of readout ASICs, today there are efforts to exploit spectroscopic features of these detectors as well in order to make them applicable to a wider range of tasks in applied physics.

In this paper a prototype of such a detector is presented. In the following we discuss the features of this device, give a description of the ASICs and strip detector, the driving electronics and PCB, and finally present some preliminary measurement results obtained by the device.

II. READOUT SYSTEM

Basically the system consists of one strip detector, 4 ASICs, one digitalization module for the analog signals produced by the ASICs, one control module for the bias voltage that depletes the sensor, an ALTERA FPGA development kit, one signal conditioning module, a module to interface the system with an external PC, and power supplies for all the components of the system.

A. Strip detector

The strip detector selected for the first stage of the project was a custom made silicon strip detector from the Norwegian company SINTEF produced in framework of the project AEGIS [8] (shown in figure 1). The detector contains 128 strips with a pitch of 80µm. It was fabricated in a 300µm thick wafer, with a total area of 14x14 mm^2 and an active area of 10x10 mm^2 connected to the PCB by wire-bonds[9].

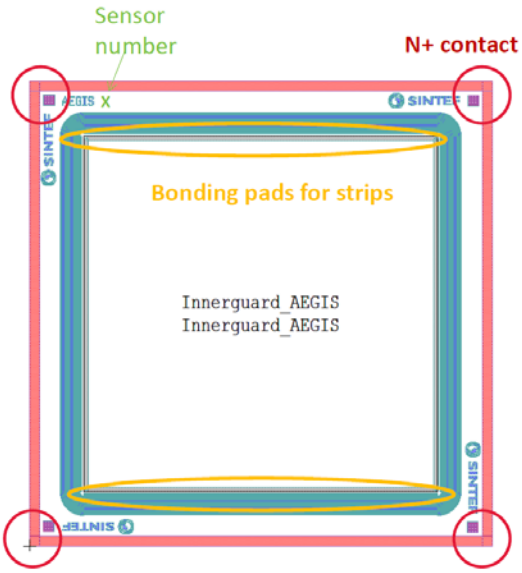

Figure 1. Strip sensor layout from SINTEF [9].

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B. *ASIC*

The ASICs chosen were designed by the Instrumentation Division Group of the Brookhaven National Laboratory (BNL) in New York, USA (shown in figure 2). Each ASIC contains 32 front-end channels and each channel contains a low noise charge preamplifier with fully compensated continuous reset, 5th order shaping amplifier with complex conjugate poles, a peak amplitude detector with analog memory, a band-gap referenced baseline stabilizer, a single threshold discriminator and a calibration capacitor [10].

The ASICs also contain a 10-bit register to coarsely control the threshold common to all the channels and a 4-bit register for individual fine equalization of each channel. The gain of the channels can be selected as: 14.25, 28.5, or 57 mV/fC. It covers an energy range up to 3.2 MeV. The shaping time can be set to 4 different values: 500ns, 1us, 2us, 4us. Additionally, the polarity to which the channels are sensitive to can be chosen (positive or negative) [10].

The ASICs used in this version of the PCB are packaged in an 80-pin QFP case by Metal Oxide Semiconductor Implementation Service (MOSIS). Unpackaged ASICs are planned to be used in further versions of the system. They have a size of only 5x5 mm^2 but must be wire-bonded for connecting to the PCB.

C. *PCB and Driving Electronics*

The driving electronics are placed on a 6-layers PCB. It contains single-ended, differential and analog signals. The system is based on an FPGA, working as the "brain" of the system, fully driving the ASICs, bias supply and other important fucntionalities, as well as supplying communication of the system with an external PC. The PCB uses a High Speed Mezanine Card (HSMC) connector and its cable to communicate with the Altera development kit. That is why the crucial part of the electronics can be placed well away from the sensor ad consequently away from harmful radiation fields.

The system works on an external 12V power supply, the supply voltages required by the different components of the PCB are provided by a number of voltage regulators. A picture of the PCB is shown in figure 3.

III. MEASUREMENTS

Figure 4 shows the complete system used during the test measurements. The measurements performed have been focused mainly on the analog performance of the ASICs. To accomplish this task the internal calibration capacitors implemented to each channel of the ASIC were employed.

As opposed of calibration with real signals obtained from the sensor this method allows to control the amount of charge injected to each channel of the ASIC individually which is a useful feature when debugging the readout system and provides the diagnostic of every channel.

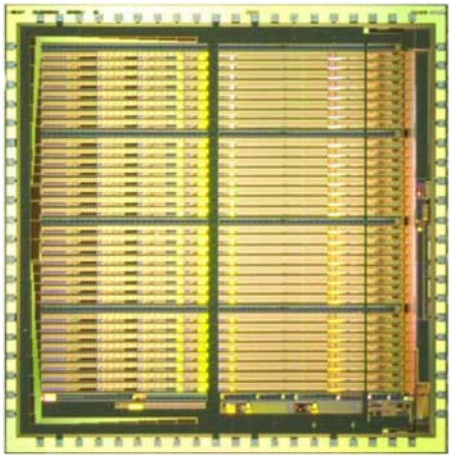
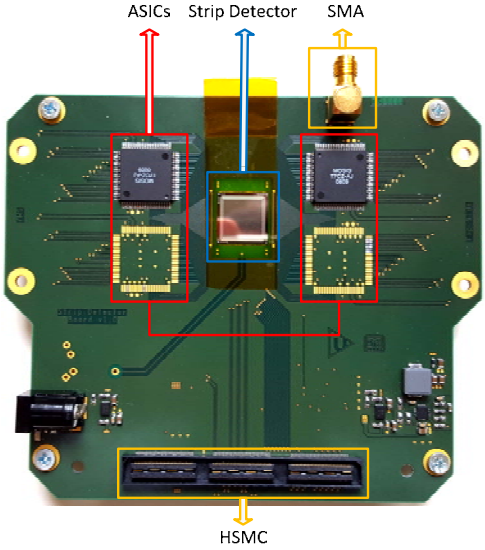
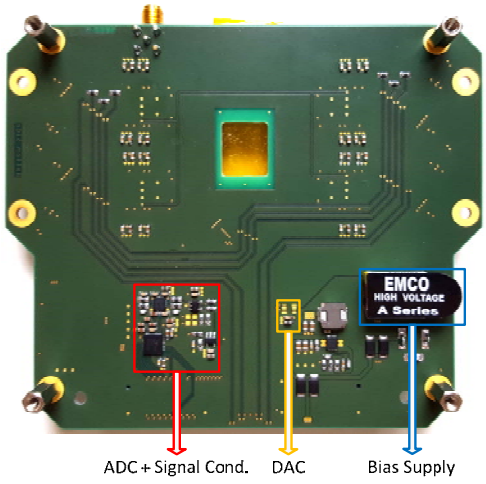


Figure 2. 5x5 mm unpackaged readout ASIC from BNL.



(a)



(b)

Figure 3. PCB sides: Top side (a), bottom side (b).

In order to test the stages of the front-end electronics available for each channel of the ASICs VHDL scripts capable to fully control the main three operational modes of the device, i.e. Acquisition, Configuration and Readout, were developed.

In a first test the linearity of the DACs controlling the charge injected to the channels was performed. The charge injections are produced by equivalent voltage pulses that feed the preamplifiers inputs, the output signal subsequently is processed by the shapers and peak detectors of each channel. The result of this test is shown in figure 4. In close agreement with the theoretical values a good linear behavior of the DAC register vs output voltage is observed.

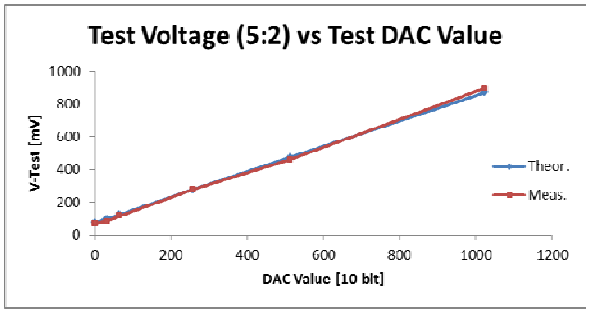


Figure 4. Amplitude of test voltage peak after 5:2 internal voltage divider vs DAC value. In blue the theoretical values and in red the measured values.

After demonstration of the linear response of the charge injection another test was performed to visualize the analog signal produced by the shapers. The shapers are an important part of the system since the peak of the produced signal provides an energy equivalent to the charge present at the input of the ASIC channels. This peak should be consistent with the voltage peak produced by the deposited energy in a particular strip of the detector. The corresponding value is then taken by the internal front-end electronics and saved in an analog memory for its external reading and digitalization.

Figure 5 shows the result of the test. The output of the shaper stage or peaking time is another important parameter since it directly affects the maximum readout speed of the system. On the other hand the contribution of noise also increases with decreasing peaking time [10]. Therefore it is necessary to find a compromise between the readout speed and the noise level of the system.

A range check of all channels of the ASIC also provides us with some interesting information. The result is shown in figure 6. In spite of applying the same amout of charge to all the channels, it is possible to see that they have slightly different performance. This is a common behavior in readout chips since the fabrication process is not absolutely perfect and the properties of the internal transistors are not exactly the same. The same effect can be observed in semiconductor detectors. No matter how precise the fabrication method is, every strip or pixel has a slightly different performance. After connecting the ASICs to the strip channels of the detector the channels will be shifted further. This however is not problematic since a homogenous response of the detector can be emulated by application of a common equalization to all channels.

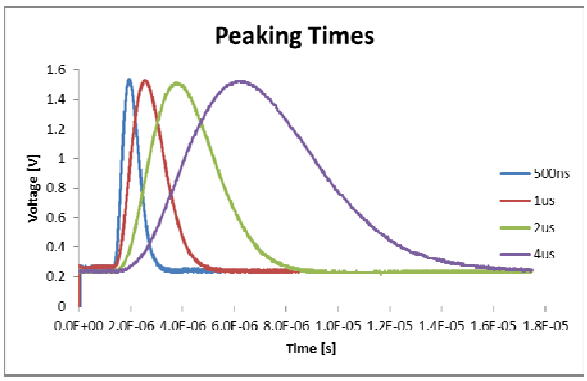


Figure 5. Peaking times of one ASIC channel for a negative charge of approx. 47.5 fC (gain = 28.5 mV/fC). Baseline (approx. 250 mV) is observed.

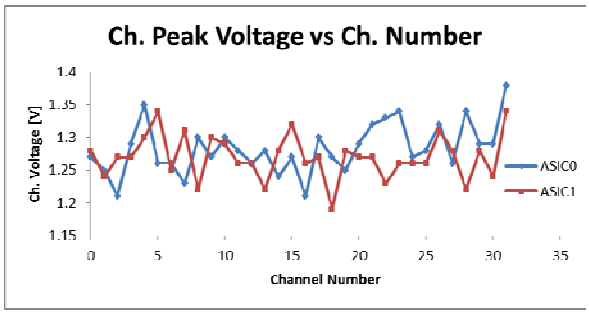


Figure 6. Peak voltage per channel for two ASICs, using a channel gain of 28.5 mV/fC and applying a negative charge of about 47.5 fC. The voltage does not include the baseline.

In a final step the analog values stored by the peak detectors were digitalized using the fast ADC module included on the PCB. Also in this case no unexpected behavior was observed.

IV. CONCLUSIONS

The present work investigated on the applicability of strip detectors in typical spectroscopic applications in the field of applied physics, e.g. single particle detection, particle tracking, dosimetry and X-ray imaging.

The measurement system basically consists of two key components: the ASICs and the strip detector.

Adequate choice of the ASIC employed is a crucial issue since it strongly determines the capabilities of the entire system. The limitations of this component in terms of ouput signal delays, maximum operational frequency and as well as some special features, e.g. output signal in sparsified mode, were evaluated in the present work.

A first version of the PCB was designed and fabricated successfully. The design took into account design rules for low noise operation when mixing analog, single ended and differential signals. Additionally, the power supplies layout was carefully

designed to reduce the noise according to the manufacturer's recommendations.

In a preliminary evaluation the test capacitors of the ASIC were successfully used to simulate the input signal coming from a strip detector. This way the functionality of the charge preamplifiers, shapers, peak detectors and other internal circuits available for each channel was verified.

There are two important advantages of the strip detectors when compared to pixel detectors: the first one is to have the readout electronics (ASICs) separated from the sensor, hence the particles penetrating the sensor don't have to interact with the front-end electronics. The second advantage is the price; strip detectors are much cheaper than pixel detectors. In applications where it is necessary to cover a large detection area, providing position information and energy if possible, it usually is more convenient to use strip detectors instead of pixel detectors.

Of course it is the long term goal of this project to employ the readout system shown here in real measurements using radioactive sources, however to this end it is necessary to complete the development of the communication protocol with the external PC, to develope a software capable to control and configure the ASICs, equalization of the system, and to visualize and save the aquired data.

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REFERENCES

[1] S. N. Ahmed, Physics and Engineering of Radiation Detection, 2nd ed., Oxford, UK: ELSEVIER, 2015.

[2] G. F. Knoll, Radiation Detection and Measurement, 4th ed., NY, USA: John Wiley & Sons, Inc., 2010.

[3] C. Grupen and B. Shwartz, Particle Detectors, 2nd ed., NY, USA: Cambridge University Press, 2014.

[4] G. Lutz, Semiconductor Radiation Detectors, 2nd ed., Heidelberg, Germany: Springer, 2007.

[5] H. Spieler, Semiconductor Detector Systems, 1st ed., NY, USA: Oxford University Press, 2005.

[6] G. Aad, et al., "The ATLAS Inner Detector commissioning and calibration," in The European Journal of Physics C, DOI 10.1140/epjc/s10052-010-1366-7, Springer, 2010.

[7] ATLAS Collaboration, "Operation and performance of the ATLAS semiconductor tracker," JINST ,2014.

[8] AEGIS Collaboration, "AEgIS experiment commissioning at CERN," in AIP Conf. Proc. 1521, 144, 2013.

[9] A. Kok. (2015, Apr. 13). AEGIS – Sample strip sensors [online]. Available e-mail: Angela.Kok@sintef.no.

[10] G. De Geronimo, et al., "Front-End ASIC for a Silicon Compton Telescope," in IEEE Transactions on Nuclear Science, Vol. 55, No 4, August 2008.