Description of the Functional Blocks for the Cross–Coupled Charge Pump Design Algorithm

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***Abstract*—This paper presents the circuit model that is used for the cross-coupled charge pump design algorithm. Symbolic description of the pump stage model as an analog functional block for high-voltage application is firstly discussed. Design process has been done by using simplified BSIM model equations assuming the long channel MOSFET. Characteristics have been verified by ELDO Spice and compared with the found relationships. Static and dynamic parameters of the subcircuit have been tested in two-stages structure by LT Spice simulator. Analysis results show the consistency between model and real circuits characteristics under given conditions. Complex model provides the reliable results for significantly smaller strange capacitances in comparision with the main pump capacitances. The model can be used for design and prediction of the pump parameters without long-time simulation process. The strong inversion region of MOSFET is expected, thus equations are correct for other MOSFET models that are used in chip design (PSP).**

Keywords - Cross-coupled charge pump, model, simulation, strong inversion, symbolic description.

I. INTRODUCTION

Cross-coupled charge pump is an advanced architecture of two-phase SC circuits designed for low-power applications on the chip. Circuit draft via the numerical analysis is unefficient from the view of the computional time. An important finding is to ensure a sufficiently

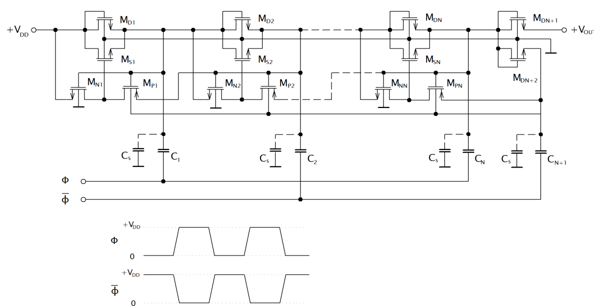

Fig. 1. Cross-coupled charge pump [5].

high voltage gain G_V at each stage, so that the pump function is correct. The basic condition $G_V > V_{TH}/2$ takes into account threshold voltage of switch transistor $V_{TH_{Msi}}$ but must also comply to treshold voltage voltage of the inverter transistors M_{Pi} and M_{Ni}, labeled $V_{TH_{MPi}}$ and $V_{TH_{MNi}}$. Threshold voltages are different in the same technology process due to body effect ([2], [4], [5]). Therefore, generalized condition for the charge pump, which will be considered, has the following form:

$$\frac{V_{TH_{Msi}}}{2} < G_V > \frac{|V_{TH_{MPi}}| + V_{TH_{MNi}}}{2}. \qquad (1)$$

The previous research has been focused on the on the theoretical and practical analysis of the cross-coupled charge pump [5], [6]. Analysis results show the charge pump description based on the equivalent digitals models does not comply with the simulation results of the real structure [5]. Corresponding waveforms were shown in [1], [5]. Thus, an alternative view on the issue has been offered. If condition (1) is not valid, this system may have a discontinuous character, as it was verified by simulation [5]. Maximal voltage gain is one of the main design criteria for pump transistors sizing [1]. For example, the CMOS inverter draft for voltage converters is different from the draft for digital applications. The minimal cross current condition means the asymmetry of the voltage transfer characteristic [1].

In this paper, the attention will be focused on the symbolic description of the pump functional blocks as an analog circuits. Simplified BSIM model equations for high-voltage applications ([1], [2], [4]) are used for this purpose (long channel transistors) . All equations were verified by simulation in ELDO Spice. The found analytical formulae of the subcircuit are tested in N-stage model by LT Spice in order to achieve the concurrence between model and real circuit characteristics. The main benefit is to find the design algorithm including the relationships for optimal transistors sizing and other pump parameters arising from the input application requirements. The strong inversion of the MOSFETs is expected, in which the behavior models is correct [3] compared with the real measured curves (BSIM, PSP) in the specified technology process.

II. ANALYTICAL MODEL OF THE PUMP STAGE

The cross-coupled charge pump stage contains the CMOS inverter, which is powered by internal voltages V_1 and V_2. DC voltage source V_{in} demonstrates the

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slow internal pump voltage change during the phase of the clock signal, i.e. charge/discharge of the main capacitor(s). The voltage on the main capacitor can theoretically achieve value V_2 in the passive interval and it will be doubled, i.e. $2V_2 \leq V_1$, in the active interval of the clock signal. Consequently, input voltage value may be continuously changed in the maximal range $V_{in} \in \langle 0, V_1 \rangle$. The input voltage V_{in} is setting

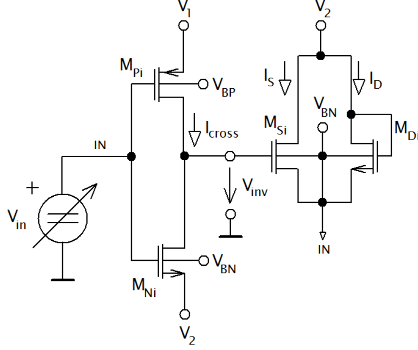

Fig. 2. Diagram of the cross-coupled charge pump stage

both the inverter cross current I_{cross} and switch current I_S through the inverter voltage transfer characteristic (VTC). Their influence on the pump properties is reported in [5]. Analytical expression of the inverter cross current characteristics (ICC) I_{cross} is determined by the drain current of the M_{Pi} or M_{Ni} transistor in saturation region, labeled $I_{DsatN(P)}$, and it is divided into three cases according to the input voltage [1]:

$$I_{cross} = \begin{cases} I_{DsatN}|V_{GS} = V_{in} - V_2, & \text{for C1} \\ I_{DsatP}|V_{SG} = V_1 - V_{in}, & \text{for C2} \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where C1 is: $V_2 + V_{THMN} \leq V_{in} \leq V_{SP}$ and C2 is: $V_{SP} \leq V_{in} \leq V_1 - |V_{THMP}|$. Calculation of the iverter switching point V_{SP} for *BSIM model* is specified in [1]. Derivation of the VTC is based on the fact, that the drain current of both the MOSFETs must be equal for each of the operating regions [4]. However, the complex expression is not necessary for practical results. Providing the long channel MOSFET, the VTC is linearized beween voltage levels V_{IL} and V_{IH}, where the valid logic levels are not defined. Then,

$$V_{out}(V_{in}) \approx \begin{cases} V_1, & \text{for } V_{in} \in I1 \\ \frac{V_1 - V_2}{V_{IL} - V_{IH}}(V_{IN} - V_{IL}) + V_1, & \text{for } V_{in} \in I2 \\ V_2, & \text{for } V_{in} \in I3, \end{cases} \quad (3)$$

where $I1 = \langle V_2, V_{IL} \rangle$, $I2 = \langle V_{IL}, V_{IH} \rangle$ and $I3 = \langle V_{IH}, V_1 \rangle$ Estimation of the parameters V_{IL} and V_{IH} is based on the condition $\tilde{I}_{cross} = 0$, where $\tilde{I}_{cross}$ specifies the relationship for the linearized ICC in both of the intervals [1] that are listed in Eq. 2.

Charge pump model application in simulator is additionaly completed by equations for other cases, when the basic condition (1) may not be satisfied. If the inverter is operating in subtreshold region, then its output voltage between input voltages V_{IH} and V_{IL} can be high enough so that, the gate-source voltage of the switch transistor will be grater than threshold voltage, i.e. $I_S > 0$. Extereme case also takes into account inverse operating mode of the inverter, when $V_1 < V_2$. These can occur, for example, during the rise time when the pump output voltage starts from 0 to the final value in steady state, for low power supply voltage, $V_{DD} \to V_{TH}$, overlap of the clock signals.... VTC of the CMOS inverter in subtreshold region (cross current is considered zero) is derived by using the subtreshold drain current equation of the MOSFET. It can be expressed as [2],

$$I_{D_s} = \underbrace{I_0 \cdot e^{\left(\frac{V_{GS_{\text{eff}}} - V_{TH} - V_{\text{off}}}{nV_t}\right)}}_{I_{S0}} \cdot \left[1 - e^{-\frac{V_{DS}}{V_t}}\right], \quad (4)$$

where n is subtreshold swing parameter, V_t is thermal voltage, $V_{GS_{eff}}$ is effective gate-source voltage, V_{off} is offset voltage, which determines channel current at $V_{GS} = 0$ and

$$I_0 = \mu \frac{W_{M_s}}{L_{M_s}} \sqrt{\frac{q\varepsilon_{Si}\text{NDEP}}{2\phi_s}} V_t^2, \quad (5)$$

where μ is mobility, q is electron charge, ε_{Si} is permittivity of silicon, NDEP is depletion doping concetration and ϕ_s is surface potential. Respecting Eq. 4 and $V_{gs_{eff}} = V_{GS}$[1], the VTC is given by

$$V_{inv}(V_{in}) = V_t \cdot \ln\left(-\frac{1}{2}\frac{I_{S0_N} - I_{S0_P} - \zeta}{I_{S0_P} e^{-\frac{V_1}{V_t}}}\right)|_{n=1}, \quad (6)$$

where

$$\zeta = \sqrt{4 I_{S0_P} I_{S0_N} e^{\frac{V_2 - V_1}{V_t}} + (I_{S0_N} - I_{S0_P})^2},$$

$I_{0_{N(P)}}$ is the drain current of the M_{N_i} (M_{P_i}) MOSFET for $V_{GS_N} = V_{in} - V_2$ and $V_{SG_P} = V_1 - V_{in}$.

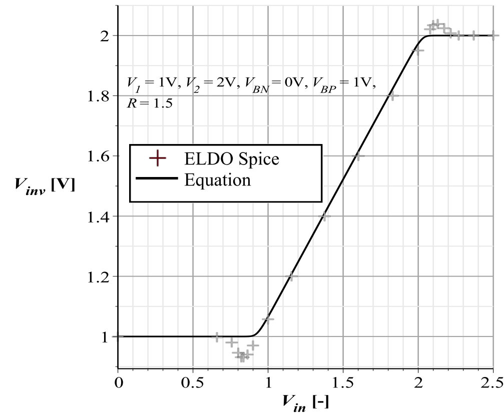

Fig. 3. Voltage transfer characteristics of the CMOS inverter for $V_1 < V_2$

Equation (6) is valid even if both the MOSFETs are OFF, therefore $V_{GS_N} \leq 0 \geq V_{SG_P}$. Then, the output voltage for case $V_1 < V_2$ is determined by the output

[1]Expression is not very accurate because the effective gate-source voltage is not considered. Drain current calculation error strongly depends on the specific vales of the bias voltages–error increses, when V_{GS} is near zero point.

resistance (drain-source) of each of the MOSFETs. This characteristic is shown in Fig. 3.

Now, the switch current I_S inclusive of its orientation will be analyzed. Thus, Drain and Source electrods of the M_{Si} transistor are not distinguished in the scheme. Under the basic condition (1), M_{Si} transistor is always ON in the interval $V_{in} \in \langle 0,V_2)$ because $v_{inv} \approx V_1$ and $V_{TH_{MSi}} < V_{TH_{MNi}}$ in the same technology process (Bulks of NMOSs are connected to the same potential). It means that main capacitor is charged during this phase and the current direction is *positive* $(I_S > 0)$ in conformity with the orientation of I_S matched in Fig.2. Moreover, the switch transistor is operating in *triode* region, labeled I_{DS0_F}, as it can be proved by using the saturation Drain-Source voltage equation [1], [2]. The current direction is reversed

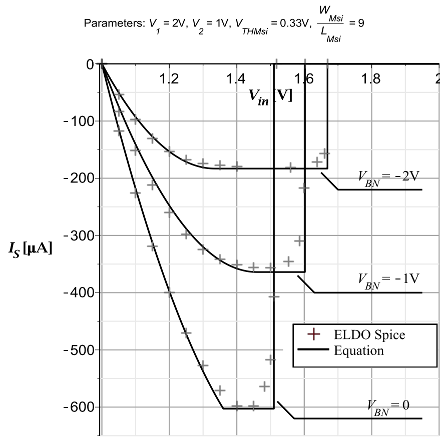

Fig. 4. Reverse current of the switch transistor vs. input voltage

$(I_S < 0)$, when the input voltage exceeds value V_2. Than drain current is controlled by the constant voltage $V_{GS} \approx V_1 - V_2$, while Drain-Source voltage is increasing (the primary function of the D and S electrods is exchanged). The switch transistor M_{Si} should be OFF in ideal case because the charge transport is realized to the next pump stage at this phase. However, reverse current I_{SR} increases until $V_{in} \leq V_{IL}$. Gate-source voltage decreases quickly in the interval $\langle V_{IL},V_{IH}\rangle$ and V_{DS} voltage change is neglibly small. Thus, the drain current achieves the maximal value at V_{IL} and it will be OFF at $V_{in} \approx V_{SP}$. The reverse current characteristic is shown in Fig.4. Total current I_S is given by the following formula:

$$I_S(V_{in}) \approx \begin{cases} I_{DS0_F}, & V_{in} \in \langle 0,V_2) \\ I_{S_R}, & V_{in} \in (V_2,V_{SP}\rangle \\ 0, & V_{in} \in (V_{SP},V_1\rangle \end{cases} \qquad (7)$$

Reverese current through the M_D transistor is zero, due to shorted electrods G and S for the negative orientation of I_D.

III. Simulation of the pump model properties

Pump model was created for the *test purposes* by LT Spice. Subcircuit of the i-pump stage X_S is shown in Fig. 5a. Internal structure includes two nonlinear dependent current sources controlled by the voltage at the output terminals also insluding Eq. (3,6). Feedback voltage V_{FB} terminal is used for connecting to the output terminal OUT of the next stage. It corresponds to the inverter supply voltage V_1 from Fig. 2. Current source BI$_1$ represents both the currents

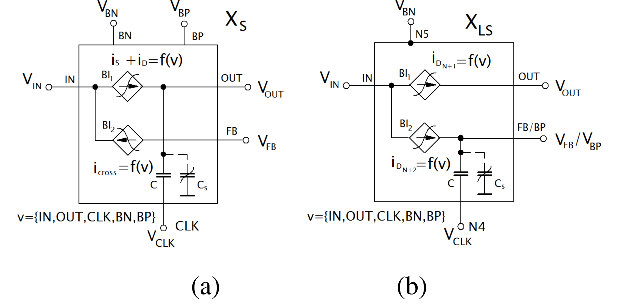

Fig. 5. Subcircuit of the i-pump stage (a) and the last stage (b)

through the diode, labeled I_D, and switch transistor (reverse+forward current), labeled I_S, and BI$_2$ models the inverter cross current, labeled I_{cross}. Subcircuit of the last stage X_{LS} (Fig. 5 b) is different from the other stages–two controlled sources only represent the drain currents through the diode transistors $M_{D_{N+1}}$ and $M_{D_{N+2}}$. Functional dependence between the currents and the control voltages $i = \mathrm{f}(v)$ follows from Equations (2-6). A Comparison of the parameters between the model and real circuit was tested in the two-stages charge pump, see Fig. 6. Some real charge

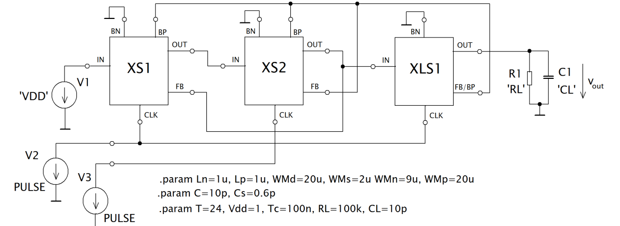

Fig. 6. Two-stages charge pump model

pump properties have been analyzed by the professional simulator ELDO Spice including real models of the components (library MGC Design Kit). Simulation parameters are given in Tab.I.

TABLE I
Simulation parameters

Parameter		Value
Temperature	ϑ	24 °C
Supply voltage	V_{DD}	1V
CLK frequency	f_c	10 MHz
Main capacitance	C	10 pF
Parasitic capacitance	C_s	0.6 pF
Load ressistance	R_L	100 k
Load capacitance	C_L	10 pF
Threshold voltage of	V_{TH0_N}	0.35 V
NMOS and PMOS at V=0	$\lvert V_{TH0_P}\rvert$	0.33 V
Channel length of N(P)MOS	L	$1\mu m$
W/L ratio of the M_{Si}	W_s/L_s	2
M_{Pi}	W_p/L_p	20
M_{Ni}	W_n/L_n	9
M_{Di}	W_d/L_d	20

Simulation results of the static and dynamic characteristics are shown in Fig. 7.

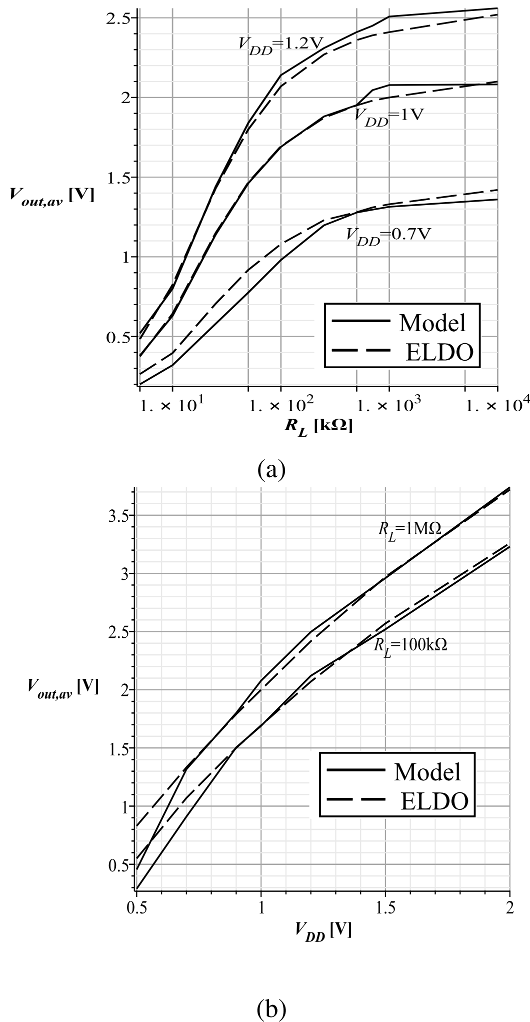

Fig. 7. Comparison static characteristics between the pump model and real circuit: Output voltage vs. load resistance (a) and supply voltage (b)

Model does not contain the dynamic part of the MOSFET model. If the the static characteristics of the model and BSIM equations are in accordance under given conditions, then pump losses caused by the parasitic capacitances can be estimated from the voltage drop of the real circuit in each of the nodes. Original MOSFET parasitic capacitances are only represented by the capacitance C_s in the pump model. Its approximate determination has not been known yet.

IV. Conclusion

Symbolic description of the functional blocks of the cross-coupled charge pump was discussed in this paper. Using BSIM model equations, the pump stage was described as simple analog macro-model circuit. Analytical relationships have been used for *optimal transistors sizing in N-stage charge pump*. All formulae were verified by simulation in the professional design software ELDO Spice, Design Architect-IC v2008.2_16.4 including the real component models in library MGC Design Kit. Long channel and strong inversion region of MOSFETs is expected, thus results are valid in the specified technology process, for example PSP models. The subcircuit of the pump stage was applied in N-stages pump for testing purposes by simulator LT Spice. Simulation results show conformity of the model and real circuits assuming defined conditions. Deviation of the output voltage increases, when the node voltage(s) drop(s) bellow a certain limit (due to low supply voltage, high load current,...) so that MOSFETs are operating in subtreshold region, see Fig. 7b. This state is not suitable in high voltage circuit. Dynamic part of model is omitted, it is provided $C \gg C_s$. Then, dynamic parameters can be estimated, as it is shown in Fig. 8. This part has been researched now. The main benefit of the model is the subsequent

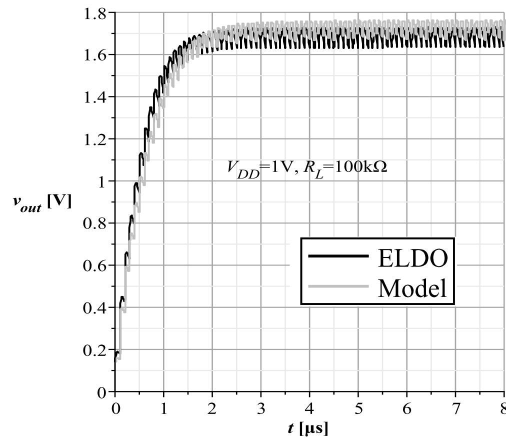

Fig. 8. Comparison dynamic characteristics (rise time) between the pump model and real circuit

creation of the design algorithm respecting both the input requirements (output voltage, load current, rise time, etc.) and real circuits properties as temperature effects, layout capacitances, etc.. The aim is to find the solution (for given circuit parameters) without long-time simulation process.

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