Practical Aspects of Realisation of Negative Charge Pumps

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Abstract – A charge pump is DC/DC converter that produces a higher output voltage than power supply or generates a negative output voltage. Some variants of charge pumps work as voltage regulator, too. A charge pump is realised by capacitors, transistors and/or diodes. Therefore, some charge pumps are integrated directly to the systems that use these charge pumps. E.g. Flash or EEPROM memories are supplied from standard voltage about 3 V, but write and erase processes use a greater voltage about 12 V. This paper is concentrated on comparison of standard variant of negative charge pump with a new design. Thus, the output voltage, rise time and other parameters of these negative charge pumps are compared by simulation executed by LTspice XVII. The simulated results are verified by practical realization of charge pumps in discrete form.

Keywords-negative charge pump; Dickson charge pump; Fibonacci charge pump; series output resistance.

I. STANDARD DICKSON CHARGE PUMP

Schematic diagram of standard Dickson charge pump (DCP) [1], [2], [3] for positive output voltage is shown in Fig. 1. This is the schematic diagram of the Nth order DCP. Therefore, DCP uses N capacitors for transfer charge (C_1 to C_N), one capacitor C_L at the output and N+1 diodes (D_1 to D_{N+1}).

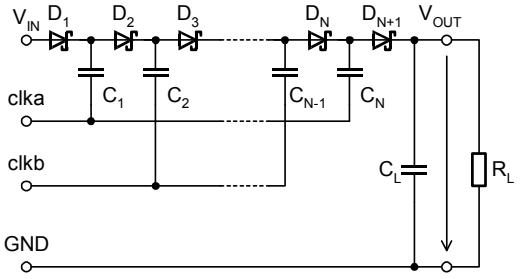

Figure 1. Schematic diagram of positive Dickson charge pump.

This variant of charge pump uses two-phase non-overlapped clock marked as clka and clkb. These clocks have swing in a range from GND to V_{IN}.

The maximal value of the voltages on diode cathodes are gradually increased to $2 \cdot V_{IN}$, $3 \cdot V_{IN}$,…, $N \cdot V_{IN}$ and $(N+1) \cdot V_{IN}$, ideally. The influence of the finite forward voltage drop V_D of used diodes leads to decreasing the output voltage about $(N+1) \cdot V_D$. Thus, the no-load output voltage V_O of positive Dickson charge pump of the Nth order applies according (1). We don't calculate the stray capacitance C_S [1] now because we assume a charge pump in discrete form and we use capacitors with relatively high capacitance ($C >> C_S$).

$$V_O = (V_{IN} - V_D) \cdot (N+1) \tag{1}$$

where V_{IN} is the input voltage, V_O is the no-load output voltage, V_D is the diode forward voltage drop, N is the number of stages.

The influence of resistive load R_L is described by the circuit accorded to Fig. 2. A charge pump is substituted as an ideal voltage source V_O with series resistance R_S.

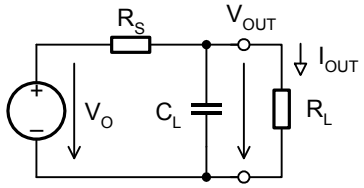

Figure 2. Equivalent circuit of DCP.

The output voltage of DCP at load is applied accorded to (2).

$$V_{OUT} = V_O - R_S \cdot I_{OUT} \tag{2}$$

where V_{OUT} is the output voltage at load, V_O is the no-load output voltage, R_S is the output series resistance, V_{OUT} is the load current.

References [1] and [2] define the output series resistance R_S as (3).

$$R_S = \frac{N}{f \cdot C} \tag{3}$$

where R_S is the output series resistance, N is the number of stages, f is the clocking frequency, C is the capacitance of transfer capacitors.

The validity of (3) is limited by a finite resistance of used diodes and finite output resistance of clock drivers for generating signals clka and clkb. Equation (3) assumes that influence of the resistance of diodes and clock drivers are sufficiently small to equivalent resistance of transfer capacitors. This condition is granted for a low capacitance of the transfer capacitors

The published research results were supported by the Internal Grant Agency of University of Pardubice, the project SGS_2017_030.

ISBN 978-80-261-0642-5,

usually. But for relatively high values of the transfer capacitance, (3) is invalid.

II. Negative Dickson Charge Pump

We can modify standard DCP to negative DCP by simply modification of the original circuit. The polarity of all diodes must be changed and the first diode D_1 must be connected to ground. Now, the minimal value of the voltages on diode anodes are gradually decreased to $-V_{IN}$, $-2 \cdot V_{IN}$,…, $-N \cdot V_{IN}$, ideally. After assuming the diode forward voltage drop, we get no-load output voltage (4).

$$V_O = -(V_{IN} - V_D) \cdot N + V_D \quad (4)$$

where V_{IN} is the input voltage, V_O is the no-load output voltage, V_D is the diode forward voltage drop, N is the number of stages.

Schematic diagram of proposed practical realisation of negative DCP is shown on Fig. 3. This solution uses two transistor inverters M_{1a}, M_{1b} and M_{2a}, M_{2b} as clocking buffers (transistors M_{3a}, M_{3b} invert input clocks only). Clocking signal clka, clkb is overlapped now. But generating non-overlapped clocking signal is circuity complicated.

The output series resistance R_S (3) must to be increased by output resistance of clocking buffers and resistance of diodes. Output resistance of clocking buffer is a finite resistance of a transistor channel in ON state.

We concentrate to the function of the first two stages now. In the first phase (clka = V_{IN} and clkb = GND), the capacitor C_1 is charged through diode D_1 and transistor M_{1b}. In the second phase (clka = GND and clkb = V_{IN}), the capacitor C_1 is grounded via transistor M_{1a} that charges the capacitor C_2 through diode D_2 and transistor M_{2b}. Described function can be generalized to all stages and then we get revised output series resistance R_{SR} (5). We assume nought ESR (equivalent series resistance) of used capacitors, thus the transfer capacitors are ideal.

$$R_{SR} = \frac{N}{f \cdot C} + N \cdot (R_{DSNMOS} + R_{DSPMOS} + R_D) + R_D \quad (5)$$

where R_{SR} is the revised output series resistance, N is the number of stages, f is the clocking frequency, C is the capacitance of transfer capacitors, R_{DSNMOS}, R_{DSPMOS}, R_D are the resistances of transistor channel or diode in ON state.

Values R_{DSNMOS}, R_{DSPMOS}, R_D are a strongly depended on applied voltage because transistors and diodes have nonlinear I-V characteristics. Right values of these resistances must be determined from I-V characteristics for actual voltages or currents values.

Proposed solution was verified by simulations by LTspice XVII. We used transistors 2N7002 (NMOS) and BSS84 (PMOS), Schottky diodes PMEG4010BEA and capacitors C = 2.2µF. Other parameters were: power supply voltage V_{IN} = 3 V, clocking frequency f = 33 kHz (amplitude 3 V, D.C. 50 %), number of stages N = 7.

Parameters for (5) are determined from I-V characteristics. Diode forward voltage drop is V_D = 0.1 V, diode resistance is R_D = 150 Ω for current 1 mA. Resistance of N-channel is R_{DSNMOS} = 4 Ω, for I_D = 1 mA at U_{GS} = 3 V. Resistance of P-MOS channel is R_{DSPMOS} = 10 Ω, for I_D = -1 mA at U_{GS} = -3 V. Thus, the revised series output resistance is R_{SR} = 1394 Ω. Table I summarizes calculated and simulated values $V_{OUTCALC}$ and V_{OUTSIM} of the output voltage for selected values of the output current I_{OUT}. $V_{OUTCALC}$ value was calculated by (2), (4) and (5).

TABLE I. Calculated and Simulated Output Voltages for Negative DCP of the 7th Order

I_{OUT} (mA)	$V_{OUTCALC}$ (V)	V_{OUTSIM} (V)
-0.0404	**-20.148**	**-20.216**
-0.1002	**-20.067**	**-20.044**
-0.1985	**-19.942**	**-19.849**
-0.3915	**-19.692**	**-19.577**
-0.9498	**-18.967**	**-18.996**
-1.8217	-17.835	-18.217
-3.3739	-15.821	-16.870
-6.7495	-11.439	-13.499
-8.0120	-9.8005	-8.012
-8.8667	-8.6910	-4.433

Table I documents that calculated and simulated results are very similar (the relative difference is a lower the 0.6%) up to the output current I_{OUT} = -1 mA. Results for other values of the output current are more different, because values of resistances R_{DSNMOS}, R_{DSPMOS}, R_D are invalid for a higher current. These resistances were calculated for current 1 mA.

Simulated results were verified by measurement. Presented negative DCP of the 7th order was realized on PCB by discrete devices listed above. These results are described in chapter IV.

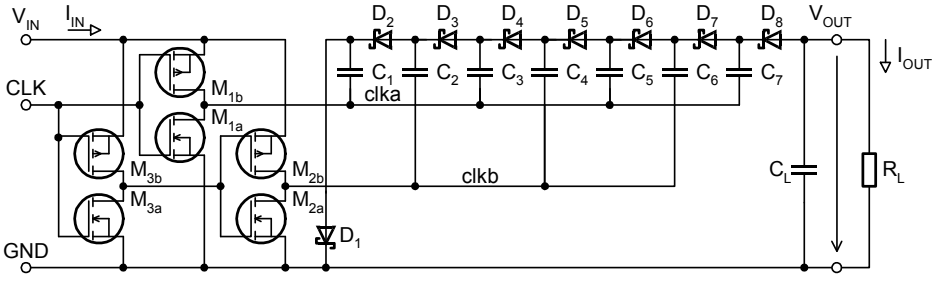

Figure 3. Practical realization of negative Dickson charge pump of the 7th order.

III. Negative Fibonacci Charge Pump

References [4] and [5] describe positive Fibonacci charge pump (FCP) as a charge pump with a higher output voltage than DCP. The voltage in each stage is increased by Fibonacci number multipliers (1, 1, 2, 3, 5, 8, …). Original positive FCP [5] can be modified to negative FCP (see Fig. 4).

Figure 4 represents negative Fibonacci charge pump of the 4th order. The switches are driven by two-phase clocks. Figure 4 is accorded to the odd phase. For the even phase, the role of switches is inverted. The transfer capacitors C_1 to C_4 are charged to voltages $-V_{IN}$, $-V_{IN}$, $-2 \cdot V_{IN}$ and $-3 \cdot V_{IN}$, ideally. Thus, ideal no-load output voltage is $-7 \cdot V_{IN}$. Thus, we get the same output voltage as for negative DCP of the 7th order.

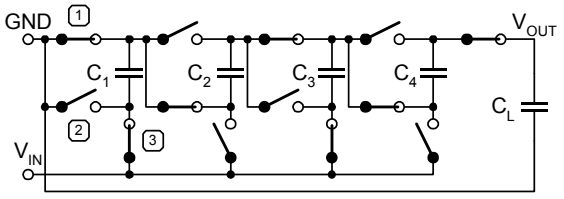

Figure 4. Principle schematic diagram of the negative Fibonacci charge pump of the 4th order (switches are drawn for the odd phase).

Proposed realization of negative FCP is shown in Fig. 5. The first switch (see Fig. 4 to the first stage) is realized by diode D_x (x is number of the stage). The second switch is realized by transistor M_{xa} and the third switch is realized by transistor M_{xb}. Other two transistors M_{xc} and M_{xd} forms inverter that drives the next stage (x+1). This inverter is a necessary for generating the opposite clock phase and for a level shifting [7], but the presence of this inverter complicates construction and evokes a leakage current.

The calculation of the FCP series output resistance is very complicated. The capacitors are charged to various voltages (DCP capacitors increase their voltage about V_{IN} for one stage) and currents of switches have various values too (DCP switches have a similar average value of a current). The I-V characteristic of a diode is defined by Shockley equation (6) [6], thus the static diode resistance is decreased with increased current. Similarly, the I-V characteristic of a MOSFET in the linear region is defined by (7) [6], thus the static channel resistance is strongly depended on the gate voltage and channel voltage (the gate voltage is gradually increased in each FCP stage). Certainly, the series output resistance of FCP has a lower value than DCP.

$$I_D = I_0 \cdot \left[\exp\left(\frac{V_D}{V_T} \right) - 1 \right] \tag{6}$$

where I_D, V_D are the diode current and voltage, I_S is the reverse-bias saturation current, V_T is the thermal voltage.

$$I_D = K \cdot \left[2 \cdot \left(V_{GS} - V_{GS(th)} \right) \cdot V_{DS} - V_{DS}^2 \right] \tag{7}$$

where K is the conduction parameter, I_D, V_{DS} are the channel current and voltage, V_{GS} is the gate voltage, $V_{GS(th)}$ is the threshold gate voltage.

Proposed solution was verified by simulations by LTspice XVII. We used transistors 2N7002 (NMOS) and BSS84 (PMOS), Schottky diodes PMEG4010BEA and capacitors C = 2.2 µF. Other parameters were: power supply V_{IN} = 3 V, clocking frequency f = 33 kHz (amplitude 3 V, D.C. 50%), number of stages N = 4.

Simulated results were verified by measurement. Presented negative FCP of the 4th order was realized on PCB by discrete devices listed above. These results are described in chapter IV.

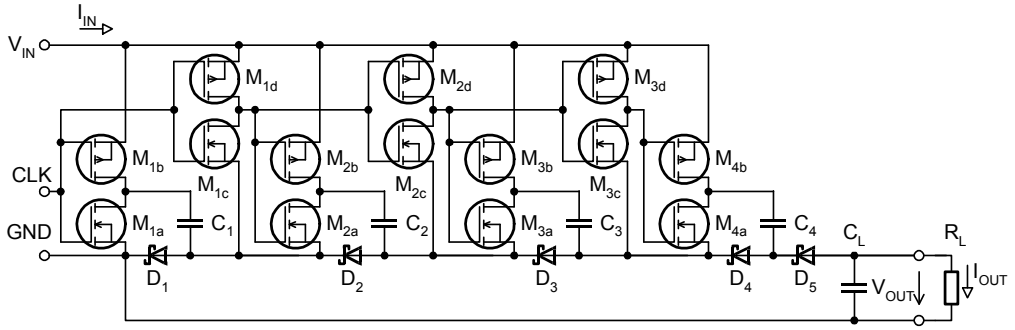

Figure 5. Practical realisation of the negative Fibonacci charge pump of 4th order.

IV. Verification

The function of the presented charge pumps was verified by measurement of their key parameters. The photography of realized charge pumps shows Fig. 6.

Firstly, we measured the dependencies of the output voltage and efficiency on the output current. Schematic diagram of the circuit is shown in Fig. 7.

In the time of the measurement, the constant value of then input voltage V_{IN} = 3V was regulated for compensation of a voltage drop of the ammeter A_1. The efficiency was calculated from standard definition as a ratio between output power and consumed input power (8).

$$\zeta = \frac{P_{OUT}}{P_{IN}} \cdot 100\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\% \tag{8}$$

where ζ is the efficiency, P_{IN}, P_{OUT} are the consumed input power and output power, V_{IN}, I_{IN}, V_{OUT}, I_{OUT} are the input or output voltages and currents.

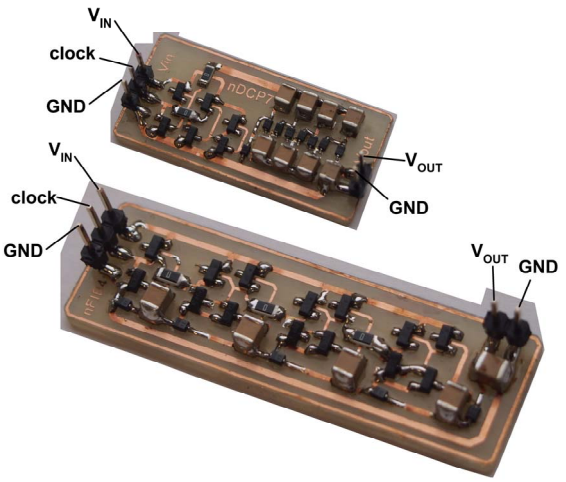

Figure 6. Photography of samples of realized charge pumps.

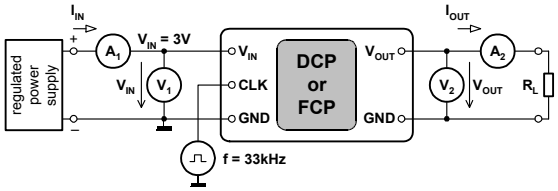

Figure 7. Schematic diagram of the measurement circuit.

The measured results are compared with simulated results by graphs that show Fig. 8 and Fig. 9.

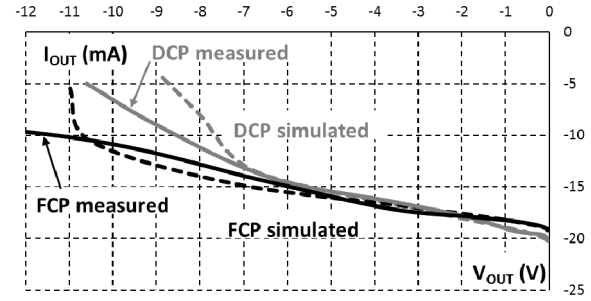

Figure 8. Graph of the output voltage as a function of the output current.

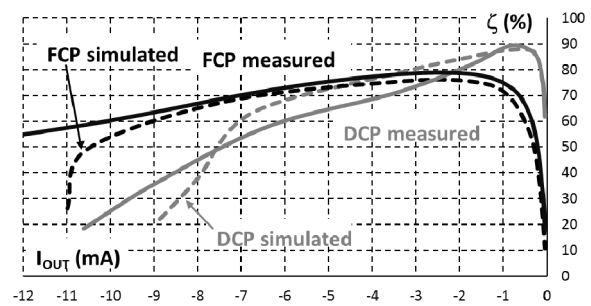

Figure 9. Graph of the efficiency as a function of the output current.

Secondly, the rise time of the output voltage at the output current I_{OUT} = -1 mA was measured. The DCP had the rise time t_{RDCP} = 64.6 ms and the FCP had the rise time t_{RFCP} = 11.8 ms. These values are related to the output series resistance, thus FCP with a lower output series resistance has a lower rise time.

Thirdly, the output ripple peak-to-peak voltage for output current I_{OUT} = -1 mA was measured. The DCP had the ripple voltage V_{Rp-p} = 10 mV and the FCP had the ripple voltage V_{Rp-p} = 10 mV, too. These values are related to the output current, clocking frequency and capacitive load. But these parameters are the same for DCP and FCP.

V. Conclusion

The principle of Dickson charge pump and Fibonacci charge pump for generating a negative voltage was presented. We generated the output voltage V_{OUT} = -18.5 V (from power supply 3 V) approximately at the output current I_{OUT} = -1 mA.

The results from simulations in LTspice XVII was verified by measurement of the discrete realization of the presented charge pumps. Presented differences between simulation and measurement are caused e.g. by a diversity of a threshold voltage of used transistors.

A Fibonacci charge pump uses a lower number of stages, has a lower series output resistance and a lower rise time. This pump is suitable for a higher output current, especially. A Dickson charge pump has a more primitive structure but uses a higher number of capacitors. The proposed Dickson charge pump uses 8 capacitors, but Fibonacci charge pump uses 5 capacitors only.

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