Accuracy Analysis of a New Reference-free Digital Temperature Sensor in CMOS

Sami Ur Rehman
Department of Electrical Engineering and Computer Sciences
Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
srehman@masdar.ac.ae

Abstract— **A CMOS digital temperature measurement technique is reported, which doesn't require an explicit reference voltage during temperature to digital conversion. Instead, one of the inputs from the sensor core serves as the reference. After eliminating the need to use an external reference, we observe at least twofold increase in temperature estimation accuracy compared to the reference based traditional approach. Designed in 65nm CMOS, the digital sensor consume a total power of 220µV and an area of 0.25mm^2, and achieves a ±3σ accuracy of 1ºC after curvature correction and room temperature trim.**

Keywords- reference-free, analog to digital conversion, thermal sensor core, accuracy.

I. INTRODUCTION

Reference circuits are considered an essential part of any digital sensor front-end circuit. Since the reference is a value against which the input is compared, the digitization of a time-varying input in a sensor readout system typically requires a PVT immune and stable reference. A Bandgap Reference (BGR) circuit introduced first in [1] is still a popular choice of implementation for many applications. The idea is based on adding a quantity complementary to temperature (CTAT) like V_{BE} or V_{GS} to a quantity proportional to temperature (PTAT) like ΔV_{BE} or ΔV_{GS} such that their temperature-dependent slopes cancel out, resulting in a temperature independent BGR ($V_{BGR}=V_{BE}+\alpha\Delta V_{BE}$, where α is a design dependent multiplication factor). Looking closely, we observe that a BGR circuit is achieved through a combination of three arithmetic operations .i.e. subtraction, multiplication, and addition. Analog implementation of these operations introduces non-linearity and error in the reference voltage, making it a sensitive circuit. Some of the common error sources which can potentially corrupt the output of BJT based BGR are 1) *Op-amp Offset*: PTAT current generation circuit requires an op-amp to generate difference of the emitter base voltage. Offset associated with this op-amp could be as large as ±10mV and can contribute largest error to BGR circuit , 2) *Process Variations in V_{BE}:* Since $V_{BE}=kT/q\times\ln(I_C/I_S)$, process variations can result from the variations in saturation current(I_S) or collector current (I_C).Spread in I_S could be due to variations in base doping and transistor dimensions. I_S can change by as much as 40% of its nominal value in even a mature CMOS node [2], 3) *Process Variations in ΔV_{BE}:* ΔV_{BE} is generated by forcing currents with different current densities in the BJTs. Temperature drift in the ratio of these currents can impact the accuracy of the BGR. 4) *Process Spread and Mismatch in Bias Resistor:* Process spread and mismatch in the bias resistors used to generate the PTAT current can result in a PTAT error, 4) *Emitter-Base Series Resistance:* Typical values of emitter-base series resistance in parasitic vertical *pnp* could be as much as 250 ohms. Voltage drop across this resistance adds error to V_{EB}, 5) *BGR Curvature:* In reality, V_{BE} does not strictly posses first order temperature coefficient and is actually slightly non-linear over a wide temperature range. This curvature of V_{EB} is carried forward to the BGR, and limits its precision.

However, since [1], many variants of BGR have been reported, some with military-grade precision. But, such accuracy can only be achieved through precision-enhancement and linearity-compensation techniques. Mixed-signal implementation of such error correction circuits in scaled CMOS nodes is challenging due to presence of various short channel effects. Also, a penalty in terms of power and area consumption has to be paid. Therefore, current trend is to push these error correction circuits into digital domain or, even better, to resort to techniques capable of moving the arithmetic operations of BGR itself into the digital world.

In the realm of temperature sensor design, one such technique was pioneered by Makinwa in his numerous publications .e.g. [3]. In [3], we observe that two of the three arithmetic operations were implicitly implemented in the digital domain; however, the difference operation is still being performed in analog domain through a difference amplifier. Now, we present a smart sensor with all arithmetics of BGR pushed into the digital backend. The theoretical concept of the reference-free scheme was first proposed in our prior publication [4]; however, this paper provides in detail the accuracy analysis of measured results.

II. THEORETICAL BACKGROUND

When two BJT devices are operated at different current densities, the difference of their base-emitter voltages is directly proportional to absolute temperature ($\Delta V_{BE}=V_{BE2}-V_{BE1}=kT/q\times\ln(n)$) [1], where

ISBN 978-80-261-0642-5,

n represents difference of current densities, as can be seen in Fig 1. This relationship has been exploited to design precise thermal sensors in silicon. It is also clear from [1] that the outputs of the thermal sensor, V_{BE1} and V_{BE2}, can be utilized to implement the BGR circuit. This BGR reference, along with an Analog-to-Digital Converter (ADC), digitizes one of the two outputs of the thermal sensor or their difference. The resulting ADC ratio of input over reference can be interpreted in a way such that one of the inputs from the sensor core serves as the reference. In other words, since a BGR is an arithmetic combination of outputs from the sensor core, we can use one input as a reference to the ADC and can implement the remaining arithmetic operations needed for a BGR after the ADC in the digital backend. To theoretically manifest this qualitative interpretation of reference-free digital temperature sensor we note that the output of any ADC is the ratio of input to the reference. This means the ADC output, μ, for the thermal sensor can be written as:

$$\mu = \frac{V_{IN}}{V_{REF}} = \frac{\alpha \times \Delta V_{BE}}{V_{BE} + (\alpha \times \Delta V_{BE})} \quad (1a)$$

$$\mu = \frac{V_{IN}}{V_{REF}} = \frac{1}{1 + \frac{V_{BE}}{\alpha \Delta V_{BE}}} \quad (1b)$$

$$\mu = \frac{V_{IN}}{V_{REF}} = \frac{1}{1 + \frac{1}{\alpha(V_{BE2}/V_{BE1} - 1)}} \quad (1c)$$

Eq (1) shows theoretically similar but practically different digitization schemes for the traditional, Makinwa [3], and the proposed method in Eq 1a, 1b and 1c respectively. Traditional scheme uses external voltage reference while implementing all three arithmetic operations of BGR in analog domain as shown in Fig 1a, [3] uses ΔV_{BE} as reference and V_{BE} as input (ADC output is $X=V_{BE}/\Delta V_{BE}$), pushing two of the three arithmetic operations into digital backend. The proposed scheme uses lower of the two V_{BE} voltages as input while other as reference (ADC output is $X=V_{BE1}/V_{BE2}$) as can be seen in Fig 1b. In [4], we proposed theoretical background of two reference-free successive approximation (SAR) ADC based smart thermal sensors. However, only the ratio-metric approach, discussed above, has been implemented in silicon and its measured accuracy results are presented here.

III. Circuit Implementation

A. Sensor Core

The sensor core consists of two parasitic *vpnps* biased with PTAT currents of different current densities (Since *vpnps* are diodes biased through emitters, we will refer to V_{BE} as V_{EB}). Vertical parasitic *vpnps* available in CMOS have to be biased through emitter.

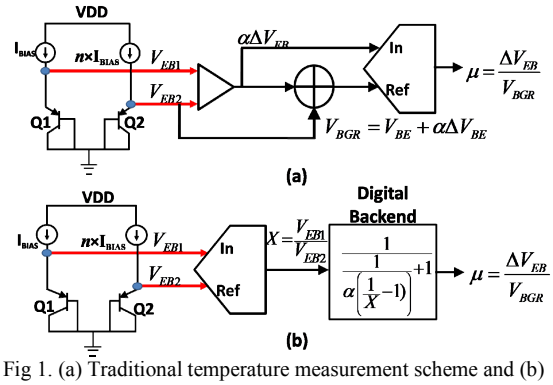

Fig 1. (a) Traditional temperature measurement scheme and (b) the proposed scheme.

This results in Vbe being dependent on the common emitter current gain, β. Variations in β result in variations in Vbe and hence affects the accuracy of the sensor. The nominal value of β is around 1 in 65nm CMOS process as can be seen in Fig 2a.

To eliminate the dependency of β, Q1 and Q2 have to be biased with PTAT current. The circuit on the left side of Fig 2b generates PTAT current by forcing the nodes X and Y to have similar voltage using the positive feedback, and copies the generated PTAT current into temperature sensing BJTs, Q1 and Q2, using MOS current mirrors, M4 and M5. Dynamic element matching was implemented in the current mirrors; however, it is not shown in the Fig 2b for simplicity. In another variant the positive feedback was replaced with an op-amp. Further details of this circuit could be found in [4].

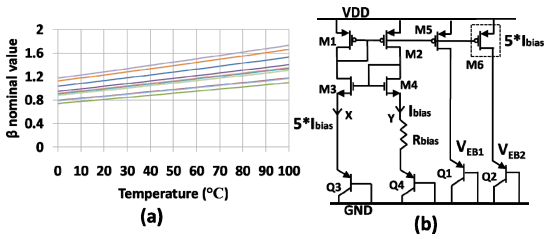

Fig 2. (a) Statistical nominal simulated values of β in 65nm CMOS, (b) Designed sensor core circuit with PTAT current generator

B. 12-bit SAR ADC

In the following stage, the implemented 12-bit data converter is split capacitor array fully differential Successive Approximation Register (SAR) ADC with unit capacitor of 20fF. The ADC, shown in Fig. 3, is monotonically switched and follows set and up SAR scheme (after sampling input, all bottom plates are grounded and then connected to V_{REF}, or remain grounded, as determined by SAR logic). V_{EB2} is first sampled on the top capacitor plate of both Digital-to-Analog (DAC) capacitive arrays. Meanwhile, the bottom plate of the DAC array is connected to V_{EB1} and the bottom plate of bottom DAC array is connected to V_{EB2}. Next the bottom plates of both DAC arrays are grounded. Afterwards regular SAR scheme is initiated and bottom plates of DAC arrays are set/reset depending on the output of the comparator. The comparator is composed of a 3-stage amplifier followed by a dynamic latch and consumes

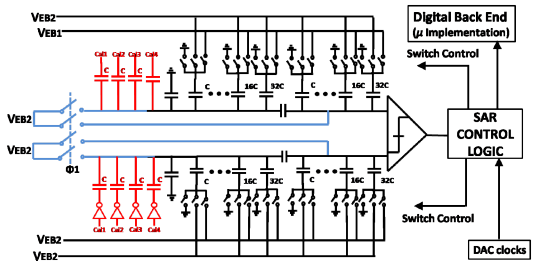

Fig 3. Designed 12-bit split capacitor SAR ADC with 4-bit calibration DAC and digital backend

30μA of current. The SAR ADC yields $X=V_{EB1}/V_{EB2}$and the digital backend was implemented as a software estimation routine.

Redundancy provides tolerance to comparator decision errors and eliminates wide codes. We employ 4-bit DAC array to provide redundancy which can tolerate up to 4 LSBs of comparator error. In SAR ADCs calibration is a process that measures and corrects for capacitor mismatch errors. Although we implemented calibration for errors in the largest 4 capacitors in our SAR architecture, the range of code values exercised by X is designed so the 3 MSB capacitor mismatch contribution becomes a simple offset. This is due to the value of X being in between the major code transitions contributed by the 3 MSBs. Since the nonlinearity due to these capacitor errors becomes effectively an offset, it is eliminated using a simple room temperature trim. The fact that the 3 MSBs do not change over the temperature range of interest can be used to eliminate the first three SAR algorithm steps to save power and conversion time, but this was not implemented in this prototype. The calibration scheme sets the 4-bit calibration DAC dynamically during SAR operation.

IV. Measurement Results and Comparison

Micrograph of the designed 65nm CMOS microchip and the measurement setup can be seen in Fig 4. The measurement setup included a thermal chamber, data acquisition IO card, reference RTD Pt-100 thermister and measurement software. The designed thermal sensor was placed inside the chamber along with reference thermister. The DUT PCB was connected to the software through the IO card. For temperature accuracy measurements the chamber temperature was

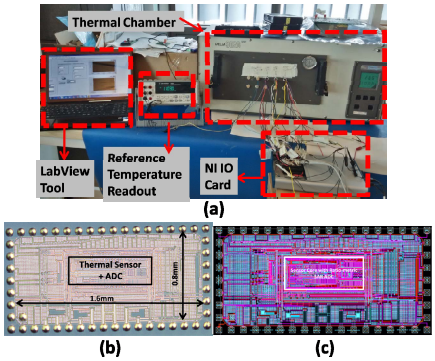

Fig 4. (a) Temperature measurement setup, (b) chip micrograph, and (c) chip layout

swept from 25ºC up to 100ºC.

To provide a comparison of the temperature estimates based on the ratio and difference of V_{EB}, we collected data for V_{EB} versus temperature from 12 chips using a 16-bit acquisition card. To eliminate the contribution of random errors during measurements, for each chip at every temperature, 20000 samples were taken and its average value was used to report the error at that temperature.

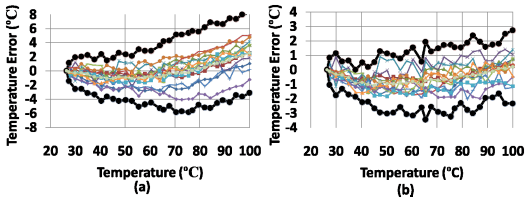

Fig 5. (a) Raw temperature estimation error from the sensor core using reference based approach and (b) reference-free approach with ±3σ limits and room temperature trim for 12 chip samples.

Fig 5 provides the statistical comparison of raw temperature sensor core error between the proposed and traditional temperature estimation schemes (BGR was estimated from the measured values of V_{EB1} and V_{EB2}). Thick black lines in the figures represent ±3σ values of errors over a temperature ranging from 25ºC to 100ºC for 12 chip samples. Fig 5 clearly suggests using the proposed scheme results in two times better accuracy compared to traditional implementation.

Process alterations in parameters like saturation current, collector current, bias resistors, base-emitter resistance etc can result in base-emitter voltage changing the polarity of its TC over temperature; usually called BJT curvature. This curvature is visibly seen in Fig 5. We computed curvature correction equations using technique presented in [5] for all chip samples over the given temperature range. For the proposed scheme we achieved correction coefficients

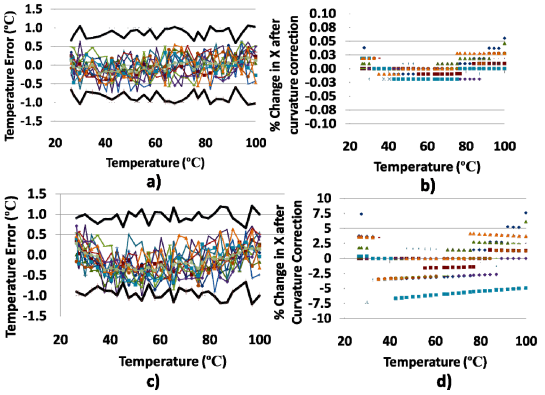

Fig 6. (a) Curvature corrected temperature error for proposed approach with ±3σ limits and (b) the corresponding % change in the value of V_{EB1}/V_{EB2}. (c) Curvature corrected temperature error for the traditional approach with ±3σ limits and (d) the corresponding % change in the value of X ($\Delta V_{EB}/V_{REF}$).

which changed the value of V_{EB1}/V_{EB2} by a maximum of ±0.05% from its nominal value across the entire temperature range as can be seen in Fig 6(a&b). Curvature correction resulted in ±3σ accuracy of within 1ºC. To achieve the same accuracy in traditional approach we had to adjust curvature

coefficients in correction equations which changed the value of $\Delta V_{EB}/V_{REF}$ by as much as ±7.5% of its nominal value compared to mere ±0.05% in proposed scheme, shown in Fig 6(c&d). Bringing ±7.5% change, compared to ±0.05%, requires considerably higher power and area overhead when these equations are implemented in hardware.

The outputs of the sensor core, V_{EB1} and V_{EB2}, were directly applied to the input and reference terminals of the on-chip 12-bit SAR ADC. Fig 7a shows the error resulting at the output of the ADC for 6 chip samples. Fig 7b shows the Differential Non-linearity (DNL) plot of the SAR ADC. A fine ramp signal was applied at the input terminal of the ADC and varied from 0.5V to 1.1V. This input was generated using the IO board with 16-bit voltage step resolution. To avoid the noise issues on the internal V_{BE2} reference to the ADC, an external1.1V was applied to the reference input.

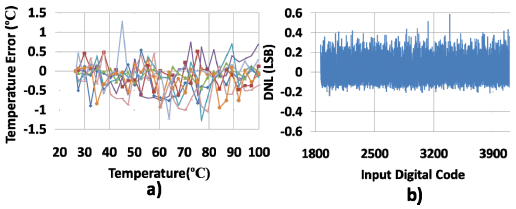

Fig 7. (a) Raw temperature error at the output of the ADC with room temperature trim for 6 chip samples. (b) DNL of the designed 12-bit SAR ADC

Fig 8 (a&b) shows error estimated following the traditional approach of using a BGR circuit as reference and ΔV_{EB} as input with a room temperature trim and two point trim respectively. Fig 8 (c&d) shows error results of sensor core from our proposed temperature estimation methodology with V_{EB1} as input and V_{EB2} as reference. Fig 8 (e&f) presents error result after curvature correction and Fig 8 (g&f) shows the estimated error at the output of the ADC.

Table I compares the specifications of the designed sensor with state of the art thermal sensors in submicron CMOS nodes which utilize similar sensing mechanism as ours mechanism as ours.

TABLE I
COMPARISON OF DESIGNED SENSOR WITH STATE OF THE ART

Sensor	Sense Mech.	Inaccuracy (±°C)	Process Node (nm)	Temp Range (°C)	Trim Points
[6]	V_{BE}/V_{REF}	1.5	14	0 to 100	2
[7]	I_{GS1}/I_{GS2}	1.6	65	0 to 100	2
[8]	V_{BE}/V_{REF}	1.5	22	-10 to 110	2
This Work	V_{EB1}/V_{EB2}	1	65	25 to 100	1

CONCLUSION

A new reference-free digital temperature estimation scheme is presented which provides ±1°C 3σ error inaccuracy with only room temperature trim in 65nm CMOS. Comparison to state of the art proves the proposed scheme provides accuracy advantage over the existing designs without employing any error compensation and linearity correction circuits.

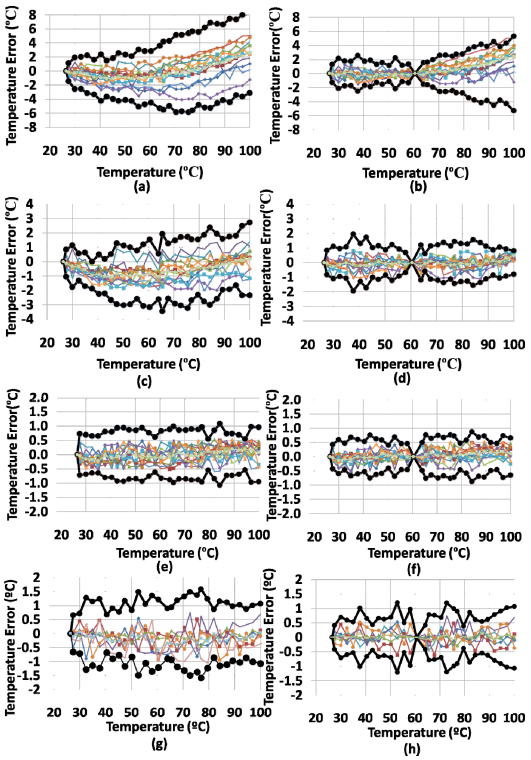

Fig 8. Statistical measured temperature error plots with ±3σ limits. (a&b) Sensor core temperature error for traditional approach, (c&d) proposed approach, (e&f) proposed approach with curvature correction from 12 chip samples.(g&h) Sensor core with SAR ADC temperature error for the proposed approach from 6 chip samples.

REFERENCES

[1] D. F. Hilbiber, "A new semiconductor voltage standard," *IEEE ISSCC Dig. Tech. Papers*, pp. 32–33, 1964.

[2] V. G. Ceekala *et al.*, "A method for reducing the effects of randommismatches in CMOS bandgap references," *IEEE ISSCC Dig. Tech. Papers*, pp. 318–319, 2002.

[3] K. Souri, Y. Chae, K.A.A Makinwa, "A CMOS temperature sensor with voltage-calibrated inaccuracy of ±0.5°C (3σ) from 55°C to 125°C", *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292-301, Jan. 2013.

[4] S. U. Rehman; A. Shabra, "A Temperature Estimation Method Using the Ratio of Emitter-to-Base Voltages," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* , vol.PP, no.99, pp.1-9.

[5] B.-S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. of Solid-State Circuits*, vol. SC-18, no. 6, pp. 634–643, Dec. 1983.

[6] T.Oshita, J. Shor, D.E. Duarte, A. Kornfeld, D. Zilberman, "Compact BJT-Based Thermal Sensor for Processor Applications in a 14 nm tri-Gate CMOS Process," *IEEE J. Solid- State Circuits* , vol.50, no.3, pp.799-807, 2015.

[7] Wenfeng Zhao; Rui Pan; Yajun Ha; Zhi Yang, "A 0.4V 280-nW frequency reference-less nearly all-digital hybrid domain temperature sensor," *IEEE Asian Solid State Circuits Conference*, pp.301-304, 10-12 Nov. 2014.

[8] J. Shor, K. Luria, D. Zilberman, "Ratiometric BJT-based thermal sensor in 32nm and 22nm technologies," *IEEE ISSCC Dig. Tech. Papers* pp.210-212, 2012