Non-isolated AC/DC Energy Converter for Smart Grid Sensor Nodes

Juraj Brenkuš, Viera Stopjaková, Jakub Chovanec and Ján Lachkovič
Institute of Electronics and Photonics
Slovak University of Technology
Ilkovičova 3, 812 19 Bratislava, Slovakia
Email: juraj.brenkus@stuba.sk

Abstract—This paper present an AC/DC converter topology for sub 0.5 W applications. The presented results are based on preliminary transistor level simulations of the circuit topology in Cadence® Virtuoso® Analog Design Environment. The technology used was a 50 V CMOS process, while the HV devices (400 V) were considered as external components and modelled accordingly. 3 HV MOS devices and 4 external passive components are required by this topology. The simulation results show efficiency more than 70% for two stage configuration, when the rectifier and buck converter is used, and more than 60% for three stage configuration, when the additional low dropout regulator is also used. Moreover, the topology shows a no-load consumption less than 15 mW for both of the configurations.

Index Terms—Power conversion, Low power, Buck converter

I. Introduction

With the emerge of Smart Grids, there is a strong need for applications that could provide data on energy consumption along the grid itself. Such applications could also include metering devices deployed on wall outlet level in households or office buildings. Such devices communicate are equipped with wireless communication interfaces to exchange information with a back-end installation (e.g. server or cloud). These devices are usually required to be compact, so they can be integrated directly to the wall outlet and always on, since they have to monitor the power drawn from the wall outlet by the appliance connected. These requirements create such criterion on the power supply of these metering devices, that the most reasonable solution is AC/DC energy conversion directly from the mains. However, as shown below the solutions available on the market have certain drawbacks that created the motivation for our work. In this paper we propose a solution to a non-isolated AC/DC converter solution suitable for such metering modules. The rest of paper is organized as follows. Section 2 gives a brief overview of existing solutions and our motivation. Section 3 describes in details the proposed AC/DC converter solution. Section 4 is addressing the efficiency evaluation of the proposed solution and section 5 compares the proposed solution with existing solutions. In section 6, conclusions are drawn.

II. Overview of available solutions

Transformer based solution with high frequency switching on the primary side, the so called flyback converter [4], [5], [6], is the most common solution available on the market. It is a widely used isolated solution for output powers from 1 W higher. Due to the usage of transformer, this topology is not easily scalable to smaller output powers. Therefore, the application of such solutions is limited to systems that can cope with a supply module that is at least $9\ cm^3$ in volume. A traditional solution to a non-isolated AC/DC converter for small output powers is a capacitive supply. This is a simple, cheap and compact solution that, however, has poor power factor due to the series capacitance [7]. Anyhow, this solution is still widely used in consumer products. Transformer-less buck converter solutions typically integrate an off-line high voltage converter circuit, e.g. [1], [2], [3]. A transformer-less AC/DC power converter based on such a circuit typically has an conversion efficiency more than 60% for output power more than 100 mW, but usually exhibits a no-load power consumption more than 30 mW. Since these days there is a lot of new emerging applications, especially in the area of Smart Grid sensor nodes, with average power consumption in the range of 10 - 200 mW (always on sensor nodes) that can't be powered from a battery (dimensions, lifetime), a solution to compact and efficient AC/DC power supply is needed. In the next chapters, we are describing such a solution, that is suitable for nodes that don't require an isolated power supply.

III. Proposed energy conversion solution

The proposed AC/DC converter solution is based on three main stages:

- Rectifier and mid-voltage converter
- Synchronous buck converter
- Linear regulator

The general electrical requirements on the design are summarized in Table I. Moreover, the design should use only minimum number of external components in order to minimize the overal converter dimensions.

The first two of these stages are vital for the functionality, the third one is optional and provides better stability and improved spectral purity of the output voltage. The proposed topology, depending on the requirements of the target application, can work in two or three stage conversion mode. Fig. 1 shows the block diagram of the proposed converter. Beside the three main stages, a protection and filtering stage is also present at the input of the converter. This stage
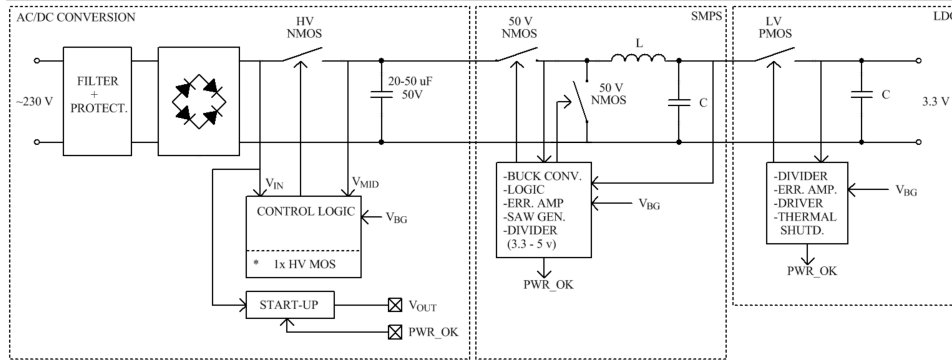
Fig. 1. Block diagram of the proposed AC/DC converter.

Parameter	Value
Input AC voltage range	80-265 V
Input voltage frequency	50-60 Hz
No load consumption	less than 15 mW
Output DC voltage	3.3 V
Output power	less than 0.5 W
Conversion efficiency	more than 60%

contains a low pass filter, an overvoltage protection and a fuse. After this stage, the rectifier stage converts the AC voltage to a lower value DC voltage and stores the converted energy in the output capacitor. The energy from this capacitor is used to feed the synchronous buck converter that converts this voltage to the 3.3 V output voltage of the AC/DC converter. If the converter is working in three stage configuration, utilizing also the linear regulator, the output voltage of the buck converter is set to 3.7 V, while the linear regulator produces 3.3 V at its output. The selection between the two modes of operation (two or three stage) is governed by an external logic signal. The building blocks of the converter are further described in more details.

A. Rectifier and voltage converter

This is the first stage of the converter and is connected to the output of the protection and filtering stage. There are two main functionalities covered by this stage:

- Input AC voltage rectification
- Level control of the rectified voltage

After the input AC voltage is rectified by the full wave bridge rectifier, the HV NMOS transistor is taking care of this stage's output capacitor charging process. This process is governed by the control logic, where the input and the output voltage of the stage is monitored. The voltage on the capacitor is controlled to be in the range of 25-50 V. Furthermore, to avoid excessive losses due to transient peaks during the charging process, the charging transistor is turned on only when the V_{DS} voltage difference on the switch is
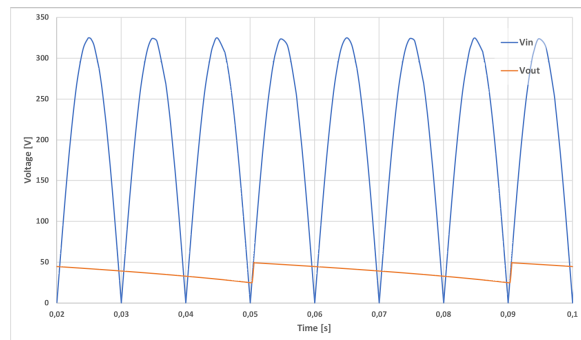

Fig. 2. Block diagram of the first stage's control logic.

Fig. 3. Input and output voltage on the rectifier switch.

close to zero, otherwise an extra serial inductor as a current peak supressor would be required. Simplified diagram of the control logic is depicted in Fig. 2.

Figure 3 shows the input and output voltage behavior of the voltage converter switch for full output load of 500 mW. Output capacitance of 22 μF is assumed.

As already mentioned, the voltage on the capacitor is controlled to be within a predefined range. The upper limit of this range is set to be 50 V. The higher this value, the better the conversion efficiency of this stage. Moreover, as stated by the equation $Q = C \times V$, the higher the voltage, the more charge can be stored in a capacitor of a given capacitance. This is vital for the timing of the first stage, since the more charge is stored in the output capacitor, the less often it has to be recharged, thus the first stage can work in a low-power (stand-by) mode. During this mode, the output capacitor voltage is monitored only and the HV input part is turned off to save power. The limitation for
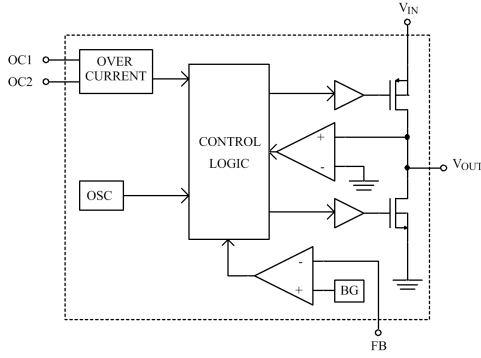
Fig. 4. Block diagram of the buck converter.

Fig. 5. Statistical distribution of R_{ON} of the pass device.

Parameter	Value
Input DC voltage range	20-50 V
Switching frequency	1 MHz
Output DC voltage	3.3/3.7 V
Output voltage ripple	less than 25 mV
Output current ripple	less than 30 mA

Fig. 6. Spectral components of the buck converter's output voltage.

maximum of 50 V for this design was given by two facts:

- Voltage levels of available HV transistors in the targeted technology
- Input voltage range limitation of the synchronous buck converter

The targeted 0.35 μm CMOS technology offers transistors with the maximum V_{DS} of 20, 50 and 120 V. From the first stage's conversion efficiency point of view the 120 V transistor would be the best choice. The second limiting factor, however, is creating an opposite requirement, since the broader the input voltage range of the buck converter ($V_{in,max}/V_{in,min}$), the bigger the voltage difference on the pass device becomes (V_{in}-V_{out}), and the bigger the output current peaks can become, thus requiring a higher inductance value in the output LC tank. Therefore, taking these requirements into account, 50 V has been selected as the mid-voltage level, providing an acceptable input voltage range for the buck converter, while also giving a decent discharge time before the capacitor needs to be recharged again.

This stage of the converter also contains the start-up circuit. This circuit takes care of the internal low voltage supply domain during the power up phase of the converter. After the output voltage regulation has been properly set up, the low voltage domain is switched to and supplied from the output of the converter and the start-up circuit is disabled.

B. Synchronous buck converter

The output of the mid-voltage capacitor is connected to the DC/DC voltage converter, more specifically to a synchronous buck converter. Block diagram of this converter is depicted in Fig. 4.

The power path consists of the NMOS pass device, the LC tank and the flyback device. In synchronous buck converter topologies, the flyback device is realized by an actively controlled MOS transistor. This transistor is switched on when the voltage at the output node of the buck converter (across the flyback device) goes below 0 V. In such case, the flyback device creates a low impedance path to the ground node and compensates the charge at the output node. The aim is to protect the pass device by keeping its V_{DS} within acceptable values. The simulates statistical distribution of the R_{ON} resistance of the pass device is showed in 5.
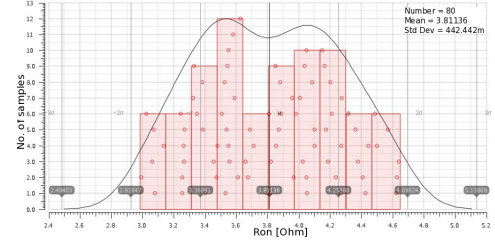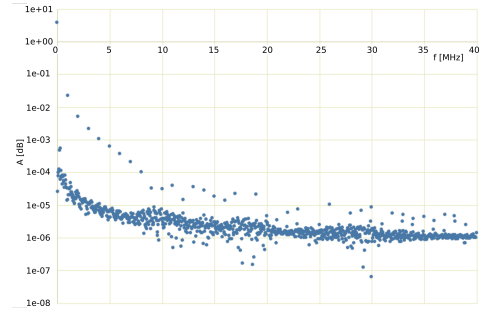
Since there are two active power devices, one creating path from the input to the output node (the pass device) and the second one creating path from the output to the ground node (the flyback device), due care has to be taken of the proper switching control of these devices, since if both device would become active in the same time, a low impedance path would be created from the input to the ground node of the buck converter. Such situation would lead to excessive current flow from the input to the ground node and, consequently, to converter malfunction. To properly address this issue, a non-overlaping clock generator was included in the control logic. The electrical specifications of the proposed buck converter are summarized in Table II The values of the output inductance and capacitance were calculated based on the equations 1 and 2, assuming the parameters from Table II.

$$L = \frac{(V_{IN} - V_{OUT}) \times D/f}{I_{RIPPLE}} \tag{1}$$

$$C = \frac{I_{RIPPLE} \times D/f}{\Delta V - I_{RIPPLE} \times ESR} \tag{2}$$

For the given parameters, the values of the inductance and capacitance were calculated to L=114 μH, C=92 nF. Figure 6 shows the spectral components of the buck converter's output voltage.

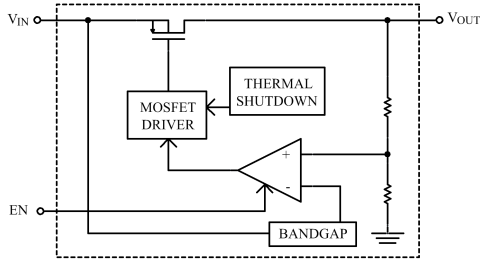Fig. 7. Block diagram of the linear regulator.

TABLE III
BRIEF SPECIFICATIONS OF THE LDO REGULATOR.

Parameter	Value
Output voltage	3.3 V
Dropout voltage	less than 350 mV
Output current	less than 200 mA
Quiescent current	less than 100 μA

C. Low dropout regulator

As the last stage of the AC/DC converter, a low-dropout (LDO) linear regulator is introduced. This stage is not necessarilly required for the proper function of the AC/DC converter, but if used, a higher quality output voltage is provided to the load. It is essential for circuits that are sensitive to spectral purity of the supplied voltage. The basic topology of the linear regulator used in this solution is depicted in Fig. 7, while Table III shows the brief electrical specifications of the proposed LDO regulator. The worst case dropout voltage obrained from the Corner analysis of the design is 345 mV with the dimensions of the PMOS device W/L=7000/0.5 μm.

IV. EFFICIENCY EVALUATION

Besides the overall dimensions of the converter, the conversion efficiency is also an important parameter of the system. Special interest is payed to the no-load state, since the converter is permanently connected to the mains, thus consuming energy. In this section we show the efficiencies of the system and the singular stages under different load conditions. These results were obtained from transistor level simulations of the circuit in Cadence® Virtuoso® Analog Design Environment. Two and three stage operation was considered, while output loads in the range from 10 mW to 500 mW, input AC voltage of 230 V (effective) and frequency of 50 Hz were taken into account. The no-load power (less than 1 mW output power) consumption of the AC/DC converter is less than 15 mW in both two and three stage configuration.

V. COMPARISON WITH EXISTING SOLUTIONS

As can be seen from the simulation results, the proposed topology shows a conversion efficiency comparable with the solutions available on the market. However, the proposed solution has a no-load consumption less than 15 mW. Such result, when compared to existing solutions, is an improvement of at

TABLE IV
EFFICIENCY EVALUATION FOR DIFFERENT LOAD CONDITIONS.

Load [mW]	Efficiency [%]				
	Rectifier	Buck converter	LDO	2-stage mode	3-stage mode
10	77.27	70.59	83.33	54.55	45.45
100	85.54	85.92	81.97	73.49	60.24
200	82.25	87.77	81.97	72.19	59.17
500	85.21	88.24	83.33	75.19	62.66

least 50%. This is a remarkable improvement since such an AC/DC converter is permanently connected to the mains. Moreover, since the proposed solution needs only a few external components, resulting in a compact design, the converter is suitable for applications with stringent criteria on dimensions.

VI. CONCLUSIONS

A solution to AC/DC power conversion for highly integrated sensor nodes was presented in this paper. This solution is intended for maximum output power 0.5 W. The solution can work in two configurations: one with a rectifier, mid-voltage converter and a DC/DC buck converter and the other one when an additional low dropout stage is added to the conversion chain. Such configuration provides improved spectral purity of the output regulated voltage. The proposed solution shows a conversion efficiency of more than 70% in the configuration without the LDO and 60% when the LDO is also deployed. Moreover, the no-load consumption of the proposed solution is below 15 mW, that is an important achievement tkaing into account that the converter is permanently connected to the mains.

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