

FPGA based modulator for five level flying capacitor inverter

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Abstract – This paper concerns a modular pulse width modulation (PWM) modulator that is suitable for polyphase multilevel inverters. The modulator is implemented in a field programmable gate array (FPGA) with a softcore microprocessor controlling it. Further it presents experiments with a five level flying capacitor multilevel inverter and the proposed modulator.

Keywords-modulator; FPGA; multilevel inverter

I. INTRODUCTION

Broad usage of the electrical energy in various fields of everyday life needs to transform parameters of the electrical energy for the particular application. Power electronic converters are capable of changing voltage, frequency and even number of phases of the electricity, so they are nowadays a key element that can be found almost in every path of the electricity before its final usage.

Basic element of a power electronic converter is a valve that is nowadays represented by a power transistor in most of cases. Properties of power semiconductor devices (not only transistors, but let's assume to use power transistors, such as IGBTs – Insulated Gate Bipolar Transistor) are being constantly improved to achieve higher switching frequency, higher current, lower losses or to withstand higher voltage. However, they are still limited in applications where high voltage is used. This limitation can be overcome by a suitable topology, where more transistors are connected in series. Switching more transistors in a series as if it would a single device is problematic, mainly due to deviations of the properties of the devices from the manufacturing process. For this reason the topologies of converters for high voltage applications are seeking for multilevel voltage solutions where each transistor can be switched separately. Various multilevel topologies are currently being studied, developed and used all over the world such as modular multilevel converter (M2C), diode clamped multilevel converter, cascaded H-bridge multilevel converter or flying capacitor multilevel inverter (FCMI). The last of them is in focus of this paper (see Fig. 5).

Every power electronic converter needs a proper control of its switching devices to perform its function.

In case of an inverter, this element is called a modulator. Waveform that should be produced on the output of the inverter is an input of the modulator. The output of the modulator can be understood as a vector of switching states of the switching devices of the inverter or more simply – modulator generates switching pulses for the transistors.

A. Realization of modulators

As mentioned before among other improvements, the switching devices can operate at higher and higher frequencies. Therefore the demands for the controllers are also rising to be fast enough to carry out the suitable switching commands. The control strategies themselves are also getting more and more complex using rising computational power of the controllers. The demands on communication properties of the controllers are also rising. While couple of years ago the serial lines such as RS-485 were sufficient, current applications in industrial field use buses such as industrial ethernet. This increases the pressure to the computational power of the controllers even more.

Producers of the microcontrollers used to offer microcontrollers with modulators. However with the market innovation cycle shortening and focus on consumer electronic, offer of such devices is slowly getting narrower. The other thing is that the producers are not giving any warranty how long a particular device will be produced. Moreover it is not viable to meet all possible applications with a series production.

These facts are driving more and more developers to use FPGAs for their application specific controller peripherals and to use microprocessors only for computation and connectivity tasks [5]. This trend has been caught also by the producers of the FPGAs who developed so-called softcore microprocessors (or soft processors) that could be implemented in their FPGAs and more recently also devices that combines so called FPGA fabric with hardware processor cores (most often ARM cores). Nowadays there are also other companies than FPGA producers that develop and offer softcore microprocessors which indicate that this market is increasing. To mention some names we can speak about Microblaze [8] and Picoblaze softcore microprocessors or Zynq and Arria devices that combine FPGA with hardware processor or even more

hardware peripherals to become a true system on chip (SoC).

B. Subharmonic PWM

Switching devices of the inverter have two principal states of operation: fully opened and fully closed. To achieve a desired waveform a pulse width modulation (PWM) is a very suitable technique, because it uses just right two states – low and high. By duration of the pulses it changes the mean value on the output.

One of the most common manner of creating the PWM is so called subharmonic PWM (some authors may use different terminology) which principle lies in continuous comparing of a carrier and a reference waveform. Imagine a phase leg of an H-bridge of a three phase two level inverter which we want to have a particular sinusoid on its output. If the carrier amplitude is smaller than the amplitude of the reference waveform, the upper valve opens; otherwise the lower valve (transistor) is opened [6] (see Fig. 1).

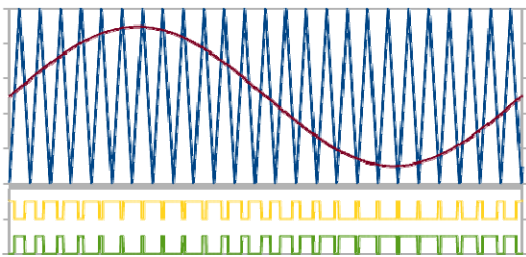


Fig. 1 Principle of the subharmonic PWM with a triangle carrier and sine reference.

The above described principle implies what kind of components a modulator must have. Solution presented in Fig. 1 can be realised by blocks shown in Fig. 3.

For an N-level inverter N-1 carrier signals are needed [1]. These can have different relations such as that they can have smaller amplitudes than the reference signal(s) and can be placed in belts each above other. Common solution is also to have the carrier signals regularly phase shifted in time [2], such as in Fig. 2. For five level inverter we need then 4 carriers.

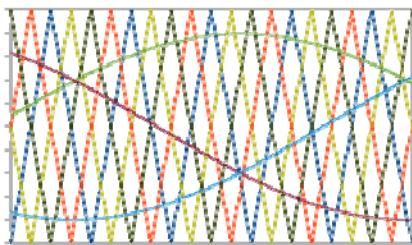


Fig. 2 Detail of possible carrier and reference signal relation for five level three phase inverter

II. BLOCKS OF THE MODULATOR

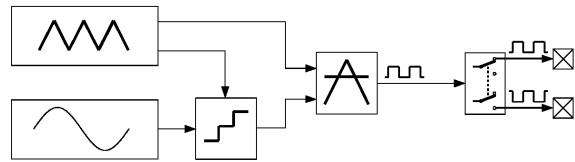


Fig. 3 Block schematic of one phase leg of a two level modulator

Blocks of carrier and reference signals are located on the left. Reference sinusoid is stored in a block random access memory (BRAM) of the FPGA in a form of a quarter of a period with suitable mathematical operations to create a reference waveform of desired amplitude and frequency to follow principles of numerically controlled oscillator [3]. Arbitrary number of samples per reference quarter-period can be used with respect to easily produce the full period without bumps and with the respect to the size of BRAM [4].

Carrier is normally implemented by a free running counter. Triangle or chainsaw waveforms can be used which have influence on harmonic composition of the inverter output waveform. Signals between the depicted blocks are numbers in essence.

The module designated with stairs is called a sampler in this paper. It should prevent creation of false switching pulses [1],[7] as presented in Fig. 4.

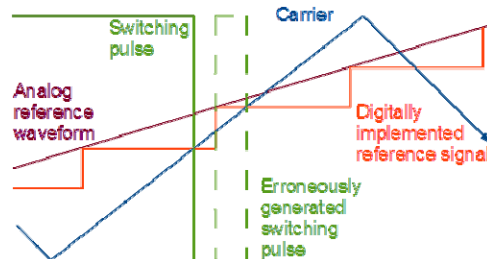


Fig. 4 Creating of a false switching pulse within

This block transfers the value of the reference to its output only in time instants when carrier signal reaches some of its peaks. This assures that the value of the reference used in comparator will not change during the period or half-period of the carrier. In case of triangle carrier waveform, sampling of the reference can be performed in upper or lower maximum or in both [4]. Output of the comparator is a binary signal for upper transistor of the complementary switching pair.

Comparator block basically realize the principle described in chapter I-B. The last block is so called dead-time generator and it should assure that the second transistor in switching pair is switched off with a time reserve before the other one is switched on.

III. EXPERIMENTAL RESULTS

A modulator for a five level flying capacitor multilevel inverter (FCMI) based on above described blocks has been implemented in a Xilinx Spartan 3AN FPGA on a Starter Kit development board [9]. VHDL language was used for the description of the

modulator. Microblaze softcore microprocessor component was used for control and communication with other peripherals. Its program is written in C language. The communication with the modulator is carried out by a set of registers. The adjustable parameters of the modulator are following: type of modulation, reference signal frequency, modulation index (the ratio between carrier and reference waveform amplitudes), carrier signal frequency and dead time.

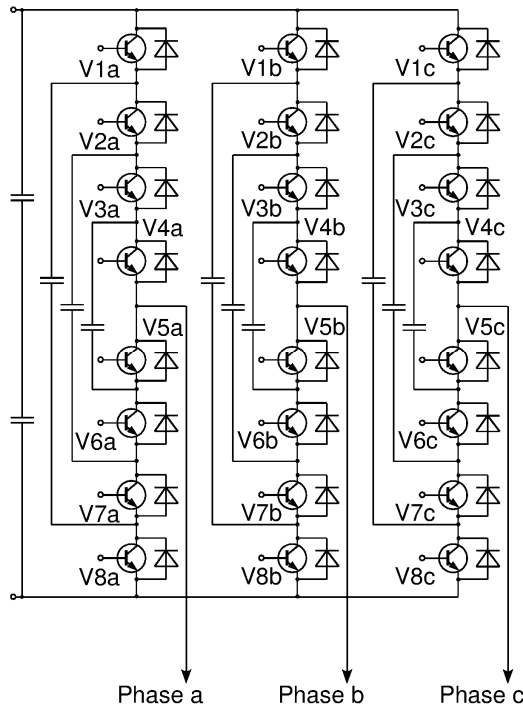


Fig. 5 Schematic of the 5 level flying capacitor multilevel inverter

Block scheme of the implemented modulator is presented in Fig. 7.

Presented test waveforms were recorded with following settings: 504 samples per sine wave period, frequency of the reference: 50,0032 Hz; modulation index: 0,8; dead time: 3 ms; carrier frequency: 1250 Hz; leading-edge regularly sampled PWM [1].

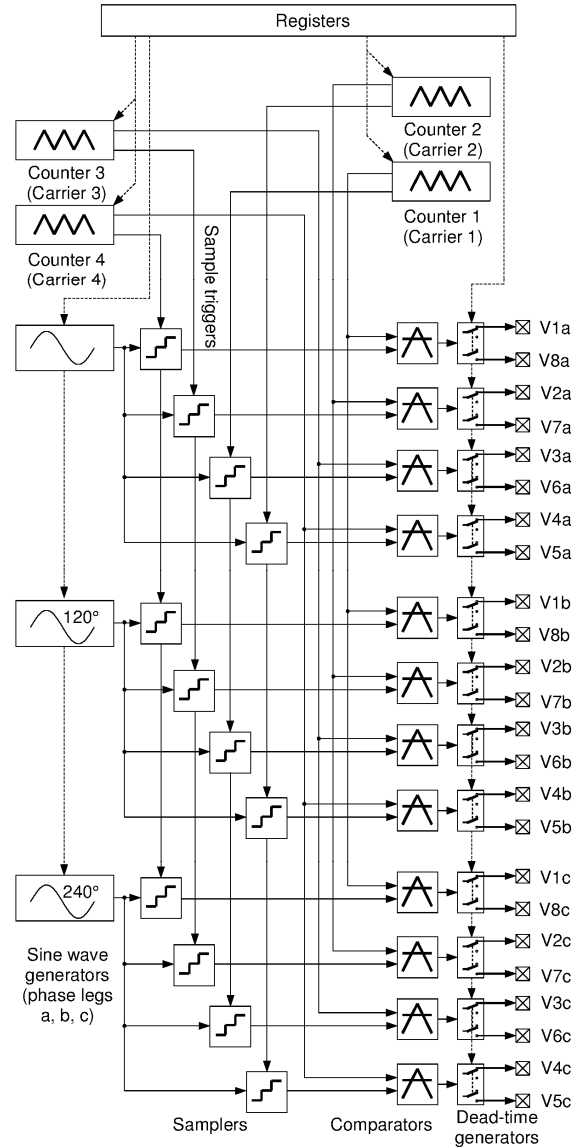


Fig. 7 Block scheme of the implemented modulator for five level inverter

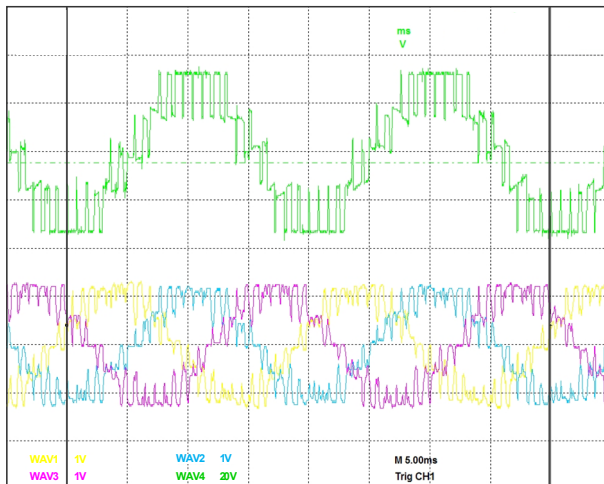


Fig. 6 Phase voltage and phase currents with pure resistive load on the output of the inverter

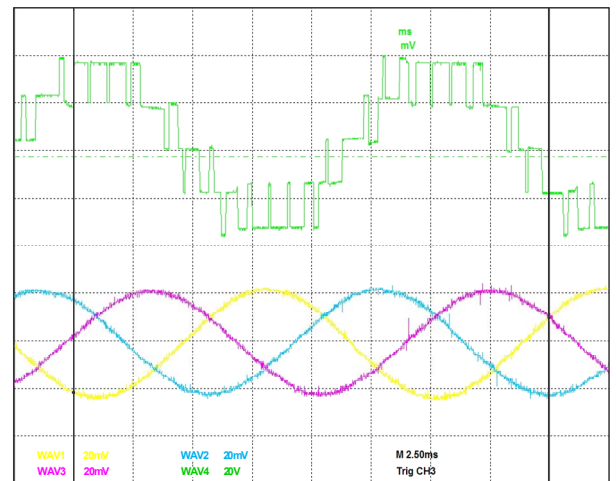


Fig. 8 Phase voltage and phase currents with RL load on the output of the inverter

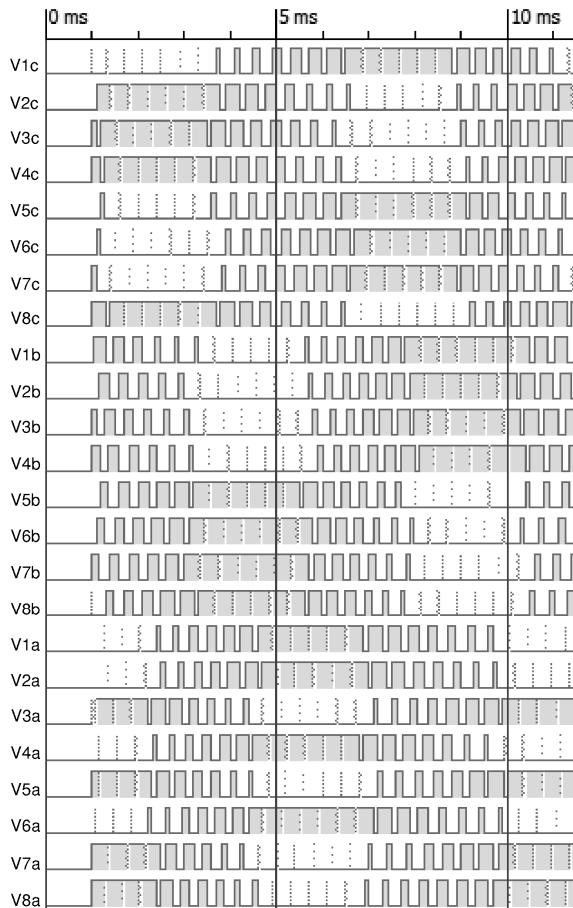


Fig. 9 Modulator pulses for all valves of the 5 level flying capacitor multilevel inverter

IV. CONCLUSION

This paper concerns implementation of a PWM modulator for a three phase five level flying capacitor inverter. It describes particular blocks of the modulator and their function. General structure of the proposed modulator is shown and experimental waveforms for resistive and RL loads are presented.

Flying Capacitor Multilevel Inverter is one of promising topologies of multilevel inverters that can be used for high voltage application such as high power electric drives or electricity transmission and

distribution system. Modulator for such a complex inverter can be advantageously implemented in FPGA which offers possibility of easy changing various types of modulations.

Tested implementation has been carried out on a Spartan 3 FPGA on a development board with Microblaze softcore microprocessor controlling the modulator values. Laboratory five level FCMI with power rating up to 1 kW was used for tests with passive loads. The recorded waveforms are promising with the voltage levels in acceptable tolerance. Tests with active loads need some more work but they are the aim of future work on this topic.

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