Digital Calibration of Operational Amplifiers and Influence of Calibration Circuitry

Michal Šovčík, Viera Stopjaková, Daniel Arbet, Lukáš Nagy and Martin Kováč

Institute of Electronics and Photonics
Faculty of Electrical Engineering and Information Technology
Slovak University of Technology
Bratislava, Slovakia
michal.sovcik@stuba.sk

***Abstract*—This paper presents the implementation of a digital calibration method for a variable-gain amplifier (VGA), where the amplifier input offset voltage is the calibration target. The whole system is implemented in $130\ nm$ CMOS technology using the supply voltage of $600\ mV$. Firstly, fundamentals of calibration circuitry operation are described, followed by detailed explanation of the proposed implementation. Then, investigation of possible undesired effects of calibration circuitry on the amplifier characteristics is performed. The whole calibration system was verified through simulation for various temperatures using Cadence environment and BSIM3v3 transistor model version. The VGA was calibrated within the temperature range from $-20°C$ to $60°C$, in which standard deviation of the input offset voltage reaches less than $802\ \mu V$ and mean value is at most $450\ \mu V$. Using the calibration, the standard deviation is reduced to 35% compared to the VGA without the calibration, while the change of mean value is rather negligible.**

***Keywords*—process-voltage-temperature variations; digital calibration; variable-gain amplifier; input offset voltage**

I. Introduction and motivation

The most well-known trends in development of semiconductor process technologies include mainly the shrinkage of integrated circuits (IC) die area and power consumption reduction. According to [1], it was fabricated a chip in $10\ nm$ CMOS process node in 2017 packing 100 million of transistors in $1\ mm^2$. Such development in IC design and fabrication brought the wide spread of electronics as we know it today. On the other hand, advanced technologies brought also drawbacks, which play a significant role in the overall trade-offs of IC design. Designers have to cope with rapidly increasing random fluctuation of process parameters, voltage and temperature sensitivity (PVT) along elements in the same die.

Therefore, along the technology downscale the fabrication can not ensure the designed process parameters, such as geometric dimensions, doping profile or dielectric layer thickness. These physical deviations consequently reflect themselves on electrical parameters of ICs. The standard deviation of the transistor threshold voltage (V_{TH}) in $45\ nm$ CMOS process node reaches approximately 16% of the mean value [2]. Other affected electrical parameters include parasitics of the chip interconnects, namely parasitic impedance and parasitic capacitance [3].

The semiconductor devices' characteristic parameters alter also with time. IC electrical parameters are therefore, affected by ageing, which creates their long-term drift causing a systematic error.

Additionally, ICs need to be obviously robust against environmental changes during the operation. This can include the temperature variation range from -20 to $85°C$. In such a wide temperature range, the electric characteristics of semiconductor devices significantly change, resulting in additional systematic error in the operation of ICs.

Another significant IC production trend, the low-power consumption arises from the need of battery operated devices or energy-autonomous systems on chip. This trend further imposes new challenges within IC design as the circuits need to maintain their functionality with substantially reduced value of supply voltage. As the V_{TH} does not scale proportionally to V_{DD}, the ratio V_{DD}/V_{TH} has decreased from approximately 3 in 800 nm process node to the level of 2 in 45 nm process node [4]. This tendency worsens even more, when combined with the temperature change and technology downscale. Thus, such challenges require important sophistication of circuit topologies and design approaches to preserve the operation parameters.

The operation of a precise analog circuit greatly depends on the matching of differential paths. Here, for example, the input offset voltage (V_{IN_OFF}) of an operational amplifier (OA) originates. This undesired parameter is tightly related to the degradation of other AC or DC amplifier parameters. Systematic or random deviations described above may actually cause the mismatch and it consequentially decreases IC reliability and production yield.

Therefore, there has arisen the effort to develop techniques for compensation of degraded parameters through the circuit calibration. The methods of digital calibration of analog ICs are developing as a counterpart to former analog methods as Autozero or Chopper stabilization. The following section will cover the general fundamentals of the calibration subcircuit (CS) proposed for analog ICs. In Section III, the implementation of the digital calibration for a variable gain amplifier (VGA) in 130 nm CMOS process is described. Section IV explain possible adverse effects of calibration circuitry on the VGA performance. Sec-

ISBN 978-80-261-0722-4,

tion V, simulation results of the implemented calibration method are presented.

II. Fundamentals of digital calibration

The general block diagram of a calibration system for analog ICs is showed in Fig.1. It is composed of the CS that is connected to the calibrated device (CD) through the sense and compensation ports P_S and P_C, respectively. As the names suggest, the CS consists of additional blocks that sense the degraded parameter and compensate it proportionally in response.

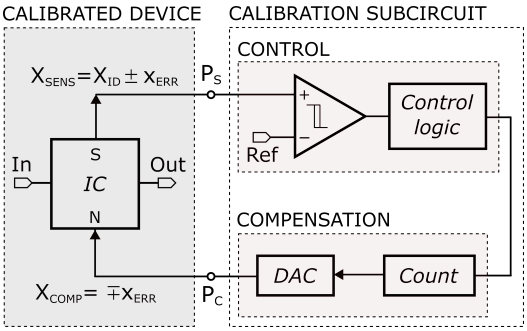

Fig. 1. Block diagram of an IC with the calibration subcircuit.

At first, an electric parameter of the calibrated device, which is impaired by PVT variations and needs to be compensated, is chosen. This parameter is then sensed with the control block through dedicated sensing port of the IC (port S in Fig.1). The sensed parameter can be generally expressed as

$$X_{SENS} = X_{ID} \pm x_{ERR}, \tag{1}$$

where X_{ID} is the ideal value of the sensed parameter X_{SENS} according to specifications, and x_{ERR} is the actual deviation of X_{SENS} from X_{ID}.

The X_{SENS} is then compared to the reference signal through a comparator based on the operational amplifier. Until X_{SENS} exceeds specified limit, the compensation block is triggered through the control logic. The compensation block consists of a digital-to-analog converter (DAC), which is controlled by a counter. While the counter is triggered, it generates gradually increasing digital code for the DAC connected to the CD through its nulling port N. The connection needs to be established in the way that the increasing DAC output value (X_{COMP}) decreases the X_{SENS}. Actually, the X_{COMP} is following the trend of x_{ERR} with inverse polarity, so the DAC feeds the inverted value of actual deviation of $X_{SENS} - \mp x_{ERR}$ to N port of the IC. Fully calibrated value of the selected circuit parameter can be defined as follows:

$$X_{COMP\_FIN} = X_{ID} \pm x_{MIN}, \tag{2}$$

where x_{MIN} is the minimal deviation that can be achieved with respect to the accuracy of the whole CS. This accuracy depends especially on the comparison precision and DAC imperfections. When the equivalence $x_{ERR} = x_{MIN}$ is achieved, the control block terminates the calibration cycle and DAC will continuously feed the X_{COMP_FIN} to the CD. The duration of a particular calibration cycle depends on the magnitude of x_{ERR} and also on the DAC switching frequency.

The proposed method of calibration is dynamic, while it reacts to the actual deviation of the sensed parameter. In this way, also temperature and ageing drifts of the IC parameters can be eliminated. Therefore, the frequency of the calibration process will depend on the continual change of factors influencing variations of IC characteristics. If the variation due to ageing is considered, a single calibration iteration at the device initiation would be sufficient. If the IC parameters vary with temperature, the calibration can be performed with low frequency (in order of Hz). In the case of the rapid change of parameters (e.g. due to flicker noise), the calibration process needs to be performed with higher frequency [5].

The CD nodes, represented by ports S and N, need to be chosen in accordance to nature of the sensed parameter and also specific IC topology. This is more deeply described in our work [6]. Further, the design of whole system needs to consider the backward effect of additional calibration circuitry on the VGA. This connection at P_S and P_C ports introduces extra parasitics, which can possibly impair the VGA characteristics. This analysis is actually the object of our further investigations.

The main advantage of proposed approach compared with other techniques of offset cancellation (as chopper stabilization and autozero) is minor impact on original characteristics of calibrated device. On the other hand, the satisfying precision of calibration raise the chip area overhead. Also the current configuration of proposed technique doesn't allow the use in continuous time signal processing.

III. Proposed Calibration System

A. Calibration objectives

As a calibrated device it was used the VGA, which was previously fabricated in 130 nm CMOS process, so the whole system could be fully integrated. The VGA is realized as a fully differential amplifier, which works with the ultra-low supply voltage of 600 mV. Its maximum gain reaches approx. 33 dB, and bandwidth of 20 kHz (for load capacitance of 10 pF) can achieved. The amplifier's V_{IN_OFF} is a main target of calibration. In order to enhance the CS performance, it was essential to optimally adjust its properties with respect to the actual V_{IN_OFF} distribution over significant number of uncalibrated VGA prototype samples. The residual offset after calibration (corresponding to the x_{MIN} in Section II) is directly proportional to the maximum V_{IN_OFF}, which this method is able to compensate. To be more specific, this property is represented by the relationship between the DAC's specifications, the resolution and the full scale. For this purpose, it was carried out the measurement of VGA V_{IN_OFF} over 60 samples of unpackaged dies. The statistical results of measurement are depicted by histogram in Fig.7. The distribution reaches the

standard deviation of 3.45 mV and the mean value of 1.01 mV. The 3σ range of V_{IN_OFF} extends to the value of 10.35 mV. Such an offset is consequently amplified by the VGA overall voltage gain, as it is actually the differential voltage. Therefore, the output voltage offset increases to 474 mV, which is quite near the supply voltage range. Eventually, this results in the substantial reduction of the VGA output dynamic range and its other critical parameters [7].

The purpose of the calibration is improvement of V_{IN_OFF} statistical distribution markers. Fig. 2 generally depicts this aim at exemplary offset distribution before and after calibration. The values in this plot represent trend line of histogram. As one can observe, the ultimate purpose of the calibration is to shift more VGA samples into range of the specification tolerance limits. Otherwise, the samples exceeding these limits need to be retested or discarded. The test expenses in some integrated systems reach 40-50% of the total cost [2]. It is important to note that increasing the integration may also this way increase the overall production costs. Consequently, this could be overcome using a successful calibration.

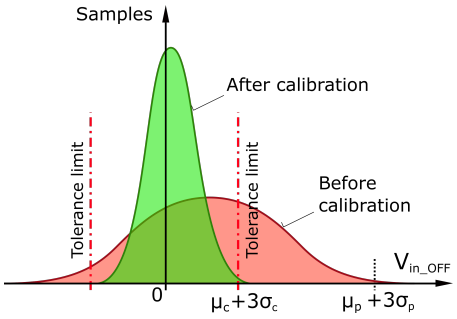

Fig. 2. The enhancement of V_{IN_OFF} distribution markers using calibration.

B. Calibration system architecture

In this section, we propose the details on implementation of whole calibration system. This was fabricated in 130 nm CMOS process together with VGA and the measurement verification is to be performed soon.

Besides the supply voltage, the proposed CS requires for now the clock signal and reference voltage drawn from an external source. The designs of an on-chip ring oscillator and bandgap reference are scheduled in the framework of future design runs so that the whole system could be fully integrated. Fig.3 depicts the block diagram of the proposed calibration systems.

Here, the main blocks correspond to the general calibration system blocks depicted in Fig.1. Therefore, the CS can be similarly divided to compensation circuitry (CPC) and control circuitry (CLC). The main difference is formed by the system terminal ports ($P_{S1,2}$ and $P_{C1,2}$) as these are realized in pairs instead of singles. This is given by the differential topology of both VGA and DAC circuits.

1) Compensation circuitry: The core of the CPC is represented by an 8-bit DAC. The converter output is differentially connected to the VGA so that

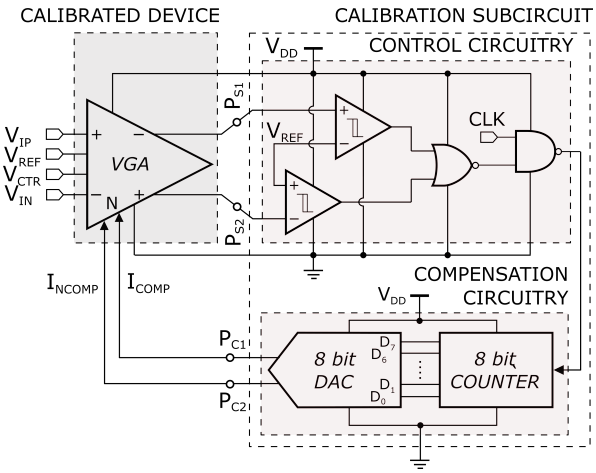

Fig. 3. The block diagram of the calibration system implemented in a VGA.

it can modify the current-voltage conditions in both branches of the amplifier differential structure. The DACs input code is set by an counter. Initially, the DAC input code is 0, and the corresponding outputs are at level of 0 and FS, respectively. The output offset voltage of VGA (V_{OUT_OFF}) is, in this case, near the supply voltage value, as the amplifier is unbalanced. Consequently, the counter increases the input code for the DAC and its outputs are responsively changing in opposite directions. The VGAs current-voltage conditions are adjusted according to the actual DAC outputs. These are gradually changing their values until they eventually swap their initial states. This process is continuously monitored by the CLC block, which terminates it immediately after V_{OUT_OFF} reaches the lowest possible value. After that, the DAC continually supplies its last set output values and calibrated VGA can emerge its normal operation.

2) Control circuitry: The main purpose of the CLC block is to terminate the calibration cycle when V_{IN_OFF} reaches the lowest possible value. This remains then as the residual input offset voltage and it is approximately equal to the DAC resolution (in the ideal case). The CLC use the V_{OUT_OFF} as a detection signal, since it is directly proportional to the V_{IN_OFF} according to following formula:

$$V_{OUT\_OFF} = A_{CLG}.V_{IN\_OFF}, \tag{3}$$

where A_{CLG} is a closed loop gain of the VGA. The main CLC parts are two voltage comparators with hysteresis. The need of two comparators instead of the only one results from the VGA differential topology. Each VGA output is connected to the first input of comparators. The second input of both comparators is fed with the reference voltage (V_{REF}), which represents the ideal VGA output common mode. As it was previously explained, the DACs outputs start to change as the counter begins to increase its output code. One of them is stepping down from FS while the other is stepping up from 0. The detection configuration of the CLC and VGA circuits is formed so that both com-

parators are initially in low output state. The following NOR gate output is kept in high state. In this way, one of the subsequent NAND inputs is in high logic state, allowing the logic gate to be transparent for the other input. This is formed by the clock signal (CLK), which is then fed to the counter. In this manner, the DAC conversion proceeds and the V_{IN_OFF} is reduced through the appropriate compensation configuration of DAC and VGA.

When one of the VGA outputs crosses the V_{REF} level, the corresponding comparator flips its output to high level and the NOR gate flips its output to low level. Since CLK signal for the CPC is stopped in this way, the counter as well as DAC maintain their last set output values. After the calibration is terminated, the CLC continues to sense the VGA output and it starts the whole cycle again when V_{IN_OFF} rises above the determined level. Therefore, this method is able to eliminate also the temperature and ageing invoked drifts of offset.

C. Layout

The layout of the whole calibration system is depicted in Fig. 4. The main parts of the system are highlighted and their dimensions are presented (in μm).

IV. Analysis of calibration circuit's adverse effects on VGA

In Fig. 5, it is depicted the circuit-level interconnection of the DAC output with the VGA, forming the compensation configuration. As it can be observed, the DAC output currents I_{COMP} and I_{NCOMP} are mirrored to the VGA circuit through bulk-driven current mirrors M_{P1}-M_{Z5} and M_{P2}-M_{Z6}, respectively.

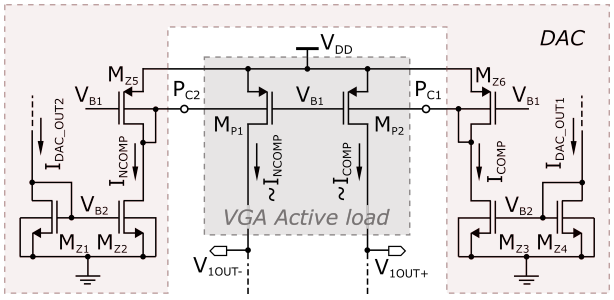

Fig. 5. The compensation configuration of DAC output and VGA.

Bulk electrodes of the VGA active load transistors M_{P1} and M_{P2} were originally connected to the source electrodes. Therefore, in the compensation configuration rises a potential of the calibration circuit's negative impact on the VGA performance. Firstly, extra transistors cause additional capacitances, arising from their semiconductor structures. Moreover, additional parasitics of chip interconnects occur as well. This will reflect mainly in the frequency characteristics, as increased capacitances alternate the location of poles and zeroes in the transfer function of the VGA.

Fig. 6 depicts the small-signal model of M_{P1} in the compensation configuration with M_{Z5} (the analysis considers only one channel of the VGA differential topology, since the same principles hold also for the other one) [8], [9]. As it can be observed, the number of elements which determine the output node pole location has doubled with M_{Z5} connected to VGA (in comparison to the case, when only M_{P1} is used).

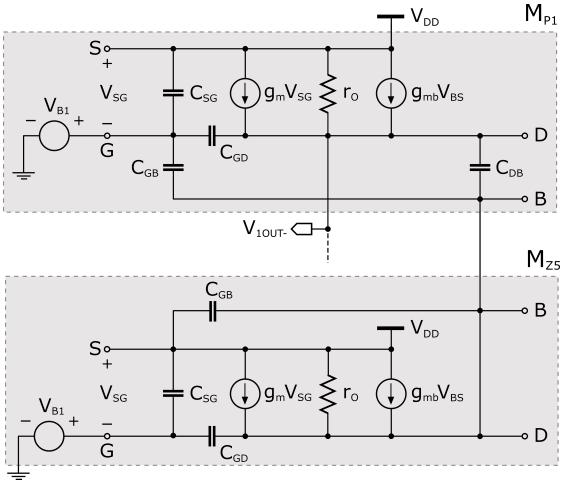

Fig. 6. Small-signal model of the compensation configuration.

V. Verification

A. Calibration system operation

The proposed digital calibration approach was verified through Monte Carlo analysis using 150 samples. The obtained distribution of V_{IN_OFF} after the calibration is compared to measurement results of non-calibrated VGA in Fig. 7, both at temperature of $27°C$. Since both distributions consist of a different number of samples, their plots are normalized. One can observe that standard deviation (σ) is reduced from $3.45\ mV$ to $0.42\ mV$ and mean value (μ) decreases from $-1.1\ mV$ to $-273\ mV$. These result prove the general aim of the calibration (Fig. 2).

The calibration process was analysed also for various temperatures. In Fig. 8, the V_{IN_OFF} distributions for $-20°C$, $27°C$ and $60°C$ temperatures are depicted. The common plots overlay shows roughly similar attributes of distributions at marginal temperatures and at $27°C$. At the moment, the calibration system suffers from unidentified issue at temperatures above $60°C$, when VGA offset is no more reduced. This remains as the further aim of our research.

The plots in Fig. 9 more precisely characterize the offset distribution. Here, the achieved reduction of σ and μ after the calibration (related to temperature) is displayed. The σ exhibits a significant drop, while it ranges from $13.5\ \%$ to $35\ \%$. The value of μ varies from $10\ \%$ to $158\ \%$, however, its magnitude remains in hundreds of μV.

B. Adverse effects of calibration circuits on VGA

To verify the hypotheses on possible adverse effects of the calibration circuits on the VGA performance, the simulation analysis of the main VGA parameters,

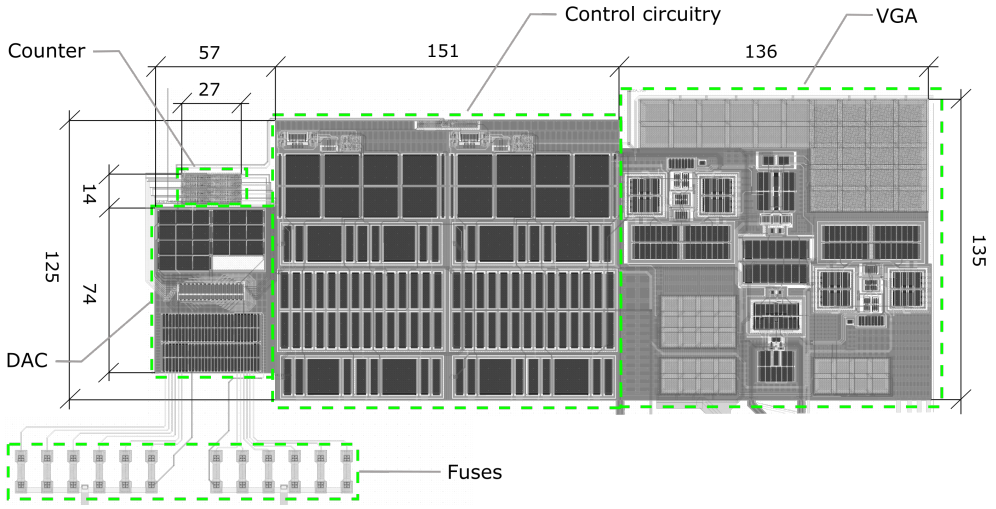

Fig. 4. The layout of whole calibration system (dimensions are in μm).

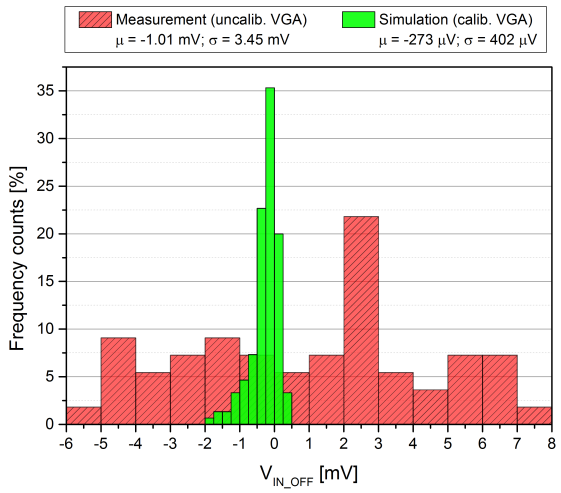

Fig. 7. Simulation results of the calibrated VGA input offset in comparison to measurement results of non-calibrated VGA (at temperature of $27°C$).

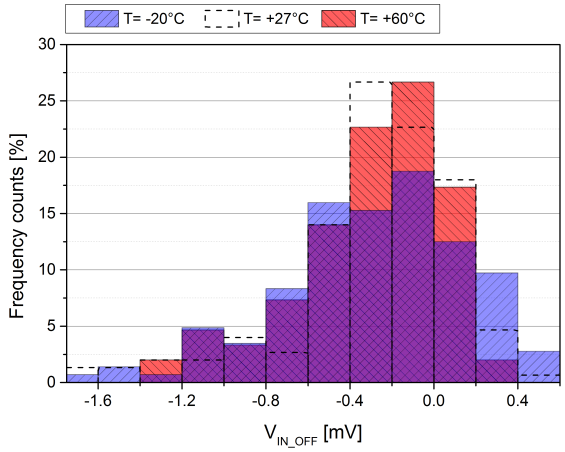

Fig. 8. Simulation results of the calibrated VGA input offset for different temperatures.

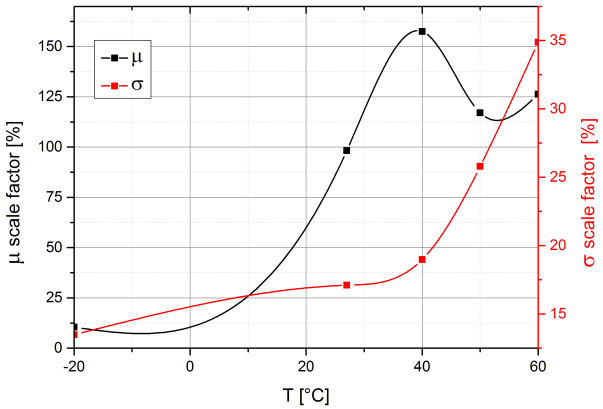

Fig. 9. Scale factor of μ and σ parameters (of the input offset) after the calibration vs. temperature.

e.i. frequency, voltage gain, bandwidth (BW) and gain-bandwidth (GBW), was performed. In these simulations, the parameters of the VGA with and without the calibration were investigated and compared, for the control voltage values in the range from $0\ V$ to $0.6\ V$.

In Fig. 10, the VGA voltage gain for different control voltages (V_{CTR}) under nominal conditions is depicted. It is obvious that the gain magnitude degradation is almost negligible.

For detailed verification of expected output node pole shift, hence BW and GBW degradation, the VGA parameters in relation to V_{CTR} (achieved results are depicted in Fig. 11). It can be observed that the BW is reduced in the compensation configuration approx. from 1.5 to $2.25\ kHz$, while the GBW does not exhibit significant change after the calibration circuit is connected.

To present the exact rate of BW and GBW degradation, the plots in Fig. 12 display the ratio of the individual parameters with and without the calibration circuit connected. In this analysis, also the process corners and temperature change were considered. In the worst-case scenarios, the BW varies between 88% and 109%, and it only slightly depends on V_{CTR}.

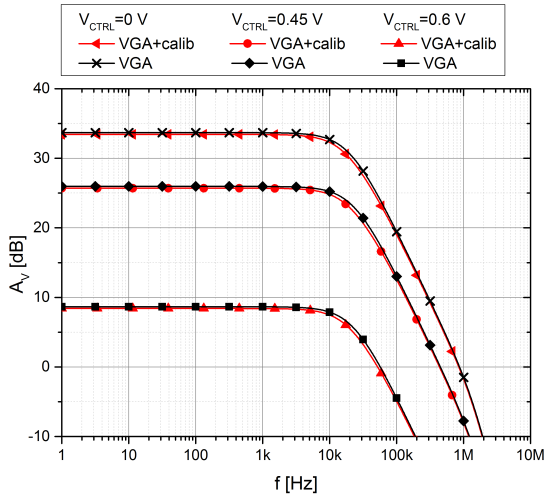

Fig. 10. VGA gain versus frequency: with and without the calibration circuit.

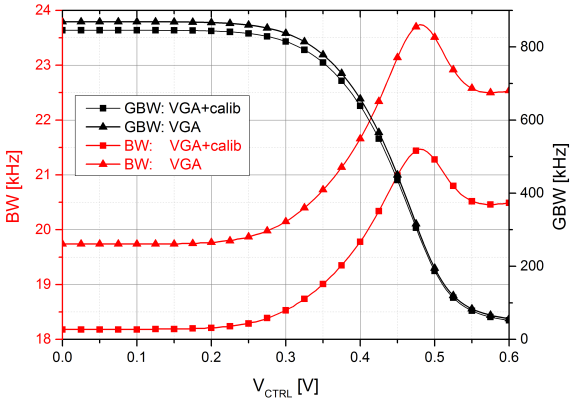

Fig. 11. The VGA bandwidth and gain-bandwidth: with and without the calibration circuit.

However, GBW exhibits greater deviations verified for the V_{CTR} range from 0.45 to 0.6 V. In the worst-case, GBW is reduced to 75%, however the mentioned V_{CTR} range corresponds to rather low values of gain. The calibrated VGA is quite robust in higher gain range.

VI. Conclusion

In this paper, fundamentals of a digital calibration system for analog integrated circuits (e.g. operational amplifiers) were presented. Implementation of the digital calibration for VGA, aimed at input offset voltage, is proposed. The whole system was fabricated in 130 nm CMOS process. The operation of the calibration system was verified through Monte-Carlo simulations, considering also temperature changes. The achieved results reveal that standard deviation of offset is reduced using the calibration to less than 35% (802 μV) in the temperature range from $-20°C$ to $60°C$. The offset mean value suffers from greater variations but it remains under 450 μV. Therefore, the proposed method appears to be promising in eliminating the amplifier input offset voltage. The further research will be aimed at the measurement evaluation to validate the simulation results. We will also focus

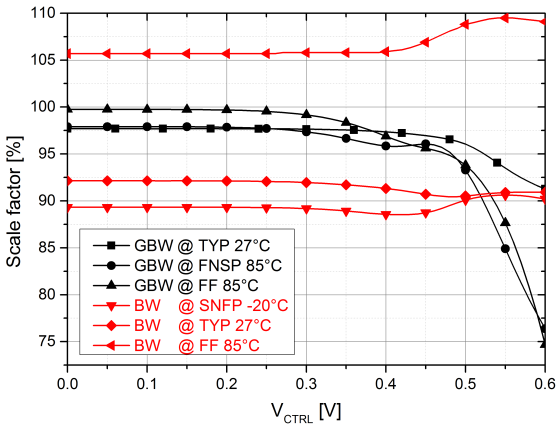

Fig. 12. The scale factor of the bandwidth and gain-bandwidth reduction: with and without the calibration circuit (process and temperature variations considered).

on expanding the temperature range of the system operability between $60°C$ and $85°C$. Further design runs will preferably include the implementation of a ring oscillator and a band-gap reference, so that the whole system could be fully integrated.

Acknowledgements

This work was supported in part by the Slovak Research and Development Agency under grant APVV-15-0254 and the Slovak Republic under grant VEGA 1/0905/17.

References

[1] R. Courtland, "Intel now packs 100 million transistors in each square millimeter," https://spectrum.ieee.org/nanoclast/semiconductors/processors/intel-now-packs-100-million-transistors-in-each-square-millimeter, 2017, [Online; accessed 13-December-2017].

[2] M. Onabajo and J. Silva-Martinez, *Analog circuit design for process variation-resilient systems-on-a-chip*. Springer Science & Business Media, 2012.

[3] J. Chang, Y. Chen, and W. C. et. al., "A 7nm 256mb sram in high-k metal-gate finfet technology with write-assist circuitry for low-vmin applications," in *IEEE International Solid-State Circuits Conference*, Feb 2017, pp. 206–208.

[4] R. Kumar and V. Kursun, "Voltage optimization for temperature variation insensitive cmos circuits," in *48th Midwest Symposium on Circuits and Systems, 2005.*, Aug 2005, pp. 476–479 Vol. 1.

[5] M. Pastre and M. Kayal, *Methodology for the digital calibration of analog circuits and systems*. Springer, 2006.

[6] M. Šovčík, V. Stopjaková, D. Arbet, M. Kováč, and M. Potočný, "Digital methods of calibration for analog integrated circuits in nanotechnologies," in *2017 15th International Conference on Emerging eLearning Technologies and Applications (ICETA)*, Oct 2017, pp. 1–6.

[7] R. Palmer, "Dc parameters: Input offset voltage," Texas Instruments, Tech. Rep. SLOA059, March 2001.

[8] B. a. Razavi, *Design of analog CMOS integrated circuits*. McGraw-Hill, 2001.

[9] R. J. Baker, *CMOS: circuit design, layout, and simulation*. John Wiley & Sons, 2008, vol. 1.