# Tracking Deadtime Algorithm for GaN DC/DC Converter

Pavel Skarolek, Jiří Lettl
Czech Technical University in Prague
Faculty of Electrical Engineering
Department of Electrical Drives and Traction,
Technicka 2, 166 27 Prague 6, Czech Republic
skaropav@fel.cvut.cz, lettl@fel.cvut.cz

*Abstract* – **The presented method automatically adjusts the deadtime of gallium nitride (GaN) transistors in half-bridge to increase the efficiency. This removes the need of manual measuring and setting the deadtime of the finished converter. The developed algorithm was tested and compared with the fixed deadtime case. The obtained results show that the developed algorithm is achieving higher and more stable efficiency compared to selected fixed deadtime.**

***Keywords - GaN transistor; deadtime; tracking algorithm; DC/DC converter***

## I. INTRODUCTION

Gallium nitride (GaN) normally-off transistors are available for power electronics [1]. Typical applications that become useful are DC/DC converters or power factor correctors (PFC) [2]. In such an application, a high frequency hard switched half-bridge is usually employed.

The absence of freewheeling diode in GaN transistor brings the benefit of zero reverse recovery current [2]. However, in half-bridge converter, the reverse conduction of the transistor is needed [3].

The reverse conduction characteristic of GaN transistor [4] is such that the gate voltage has to be applied for the transistor to achieve a low voltage drop in the reverse conduction region.

The same phenomenon occurs in all metal oxide field effect (MOSFET) transistors. However, the body diode that is present in silicon and also in silicon carbide (SiC) structure has much lower voltage drop. This leads to the decrease in efficiency in particular when increasing deadtime is not significant for MOSFETs except GaN. It is because the body diode conducts the reverse current however, GaN transistors do not have the body diode in its structure [5].

The deadtime must be carefully adjusted for the converter equipped with GaN transistors to keep the high efficiency in a wide range of power [6].

The proposed algorithm is developed for typical buck or boost DC/DC converter employing half-bridge of GaN transistors and working inductor coil as in Fig. 1.

One option is to measure the efficiency depending on the converter power and create a look-up map that determines the optimum deadtime for the control circuit [7].

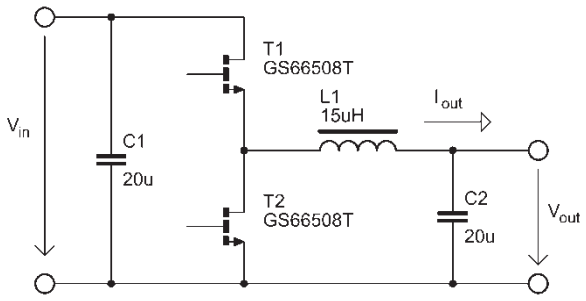


Figure 1. DC/DC converter topology

The other option is to add a specific analogue circuit which measures the voltage drop at reverse conduction as a feedback for the control circuit adjusting the deadtime [8].

This technique needs more time to be spent when putting the converter into operation because of the necessity of measuring the deadtime look-up map or adding a new circuit.

The proposed tracking algorithm works only with regularly measured values such as output voltage and current to find the optimum deadtime. The tracking algorithm for example [9] keeps adjusting the deadtime online when the converter is running.

## II. TRACKING ALGORITHM

When the added deadtime is longer than needed it forces the GaN transistor to operate in reverse conduction region with no gate voltage applied. It results to higher voltage drop and lowers the converter efficiency.

To operate the tracking algorithm, it is necessary to find a value that should be measured in the circuit and that depends on the converter efficiency.

For the converter we can write the following equation (1). The output voltage $V_{out}$ depends on the input voltage $V_{in}$, the converter duty cycle $d$, and a voltage drop that represents also the voltage loss $V_{loss}$ caused by the deadtime.

$$V_{out} = V_{in} \cdot d - V_{loss} \quad (1)$$

If we neglect the loss in the inductor coil, as we study only the half-bridge, we can write that the loss voltage depends on the deadtime $t_{dt}$, switching period $T$, on-state resistance $R_{DSon}$, off-state resistance in reverse conduction region $R_{SDoff}$, and output current $I_{out}$ according to (2).

ISBN 978-80-261-0812-2, 

$$V_{loss} = \left(R_{DSon} \cdot \frac{T - t_{dt}}{T} + R_{SDoff} \cdot \frac{t_{dt}}{T}\right) \cdot I_{out} \quad (2)$$

Because the off-state reverse resistance is much higher than the on-state resistance the loss voltage depends mostly on the deadtime.

$$R_{SDoff} \gg R_{DSon} \quad (3)$$

$$V_{loss} \sim t_{dt} \quad (4)$$

It leads to the option that we can measure the output voltage for constant converter duty cycle while adjusting the deadtime and find an output voltage maximum.

The maximum exists because decreasing the deadtime behind certain value forces transistors to operate short circuited. It means that further decreasing the deadtime decreases the output voltage according to Fig. 2.

The main benefit of the algorithm is that we don't have to calculate driver delays and transistion times to estimate properly the minimum safe deadtime. The algorithm is able to find it only by measuring the output voltage in case of constant duty cycle and input voltage.

## III. Duty Cycle Correction

Changing the deadtime changes the duty cycle, too. For the tracking algorithm correct operation we have to correct the duty cycle when changing deadtime.

We have to separate two different modes of operation depending on continuous or discontinuous inductor current. In each of them the duty cycle correction is different.

### A. Continuous Current Mode

In continuous current mode the current flows through the inductor in one direction only. It means that in the half-bridge one transistor acts as a freewheeling diode and conducts the reverse current when the other one is turned off.

The voltage drop on transistors operating in reverse conduction region appears only on one of the two possible voltage levels according to Fig. 3 depending on the direction of the inductor current.

As shown in Fig. 3, the deadtime changes the resulted converter duty cycle. When we define the controller duty cycle $d_{MCU}$ (5) as the transistor T1 on-time $T1_{on}$, we can calculate the converter duty cycle according to (6).

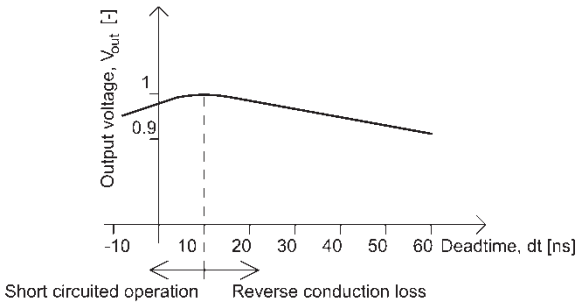


Figure 2. Output voltage dependency on deadtime

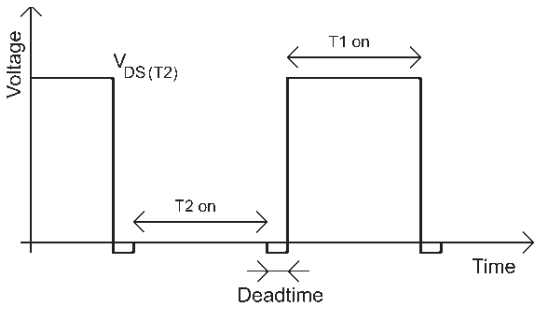


Figure 3. Continuous current mode

$$d_{MCU} = \frac{T1_{on}}{T} \quad (5)$$

$$d = d_{MCU} - \frac{t_{dt}}{T} \quad (6)$$

It means, we have to adjust the $d_{MCU}$ together when changing the $t_{dt}$.

### B. Discontinuous Current Mode

In discontinuous current mode of operation the inductor current changes its polarity during each switching period. This happens when the average current is smaller than half of the peak-to-peak current ripple. Every time one transistor is turned off, the other conducts the reverse current.

According to Fig. 4 the reverse voltage drop caused by the deadtime appears always after both rising and falling transitions. Because of that in discontinuous current mode the deadtime does not affect the converter duty cycle (7).

$$d = d_{MCU} \quad (7)$$

## IV. Measured Results

The tracking algorithm was tested on a GaN DC/DC converter prototype shown in Fig. 5. The board consists of the half-bridge made of two GS66508B GaN based transistors with high speed drivers derived from [10] and of the microcontroller STM32F334 to generate gate signals.

The controller is ARM Cortex M4 equipped with high resolution timer that enables the deadtime and also the duty cycle resolution to be down to 217 ps [11].

The deadtime setting affects the efficiency significantly. So the measurement was performed for two cases, in the first case with fixed deadtime setting and in the second one with the proposed tracking algorithm. The efficiency was measured in multiple points while changing the transferred power of the DC/DC converter.

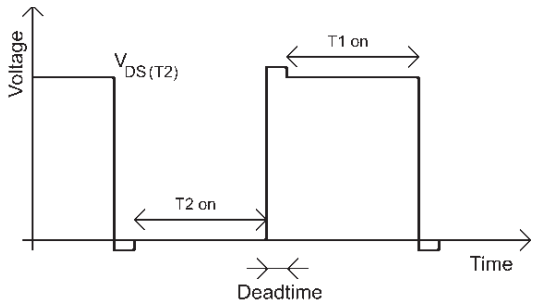


Figure 4. Discontinuous current mode

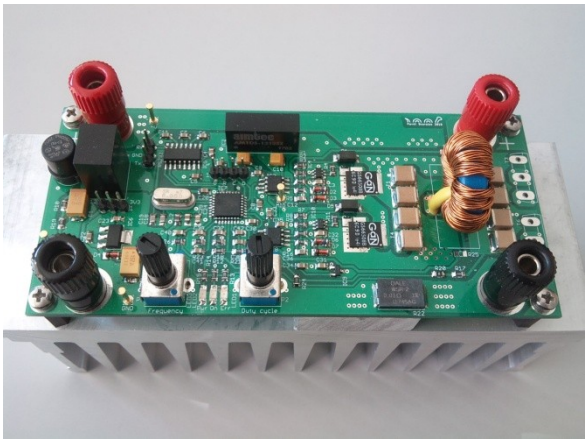

Figure 5. GaN DC/DC converter prototype

### A. Output Voltage Waveform

Depending on the load, two different output voltage waveforms were observed, depending on the continuous and discontinuous current modes.

In Fig. 6, the output voltage waveform in continuous current mode is shown. For the comparison with Fig. 7, in the discontinuous current mode the duty cycle is not compensated. We can see that without the compensation the continuous current mode results in lower duty cycle. The deadtime is here clearly represented by the times when the voltage is negative.

For both figures the set parameters are: the duty cycle $d_{MCU}$ = 0.5, the deadtime $t_{dt}$ = 100 ns, and the switching period $T$ = 2 500 ns.

For the continuous current mode in Fig. 6, the duty cycle is decreased to $d$ = 0.46 because of the deadtime.

In Fig. 7, the duty cycle remains the set $d$ = 0.5.

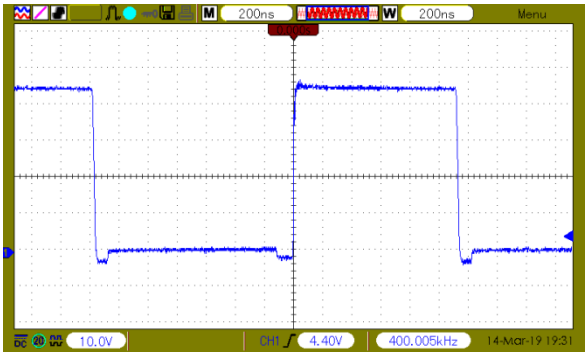


Figure 6. Voltage waveform in continuous current mode

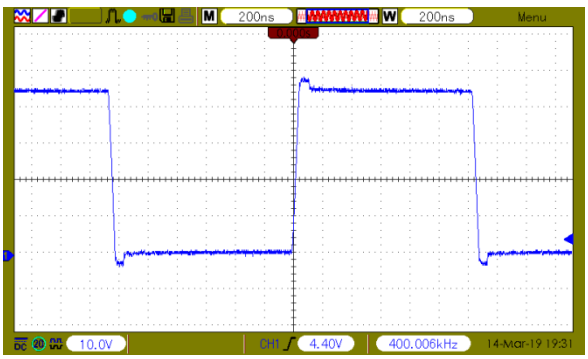


Figure 7. Voltage waveform in discontinuous current mode

It is because in discontinuous current mode the inductor current is always flowing through the opposite transistor when the other one is turned off. This symmetrical operation makes no change in converter duty cycle unlike the case of continuous current mode.

### B. Output Voltage on Deadtime Dependency

In Fig. 8, the dependency of output voltage on the deadtime was measured to make sure that the maximum exists.

It was measured with decreased input voltage of 40 V and 0.5 duty cycle to be safer to use also into the negative deadtime.

In the negative deadtime, the transistors are in short circuit operation across the half-bridge for the time $-t_{dt}$ resulting in dramatic heat dissipation increase. The short circuit current in this case is limited by the parasitic inductances in the half-bridge supply.

The voltage drop is steep so it was measured only to $t_{dt}$ = -10 ns where the voltage dropped to similar value as for $t_{dt}$ = 100 ns.

The deadtime is plotted with respect to the gate signals, so partly short circuited operation is appearing also when the deadtime is lower than switching delays of the transistors [4].

When the deadtime decreases from higher values the output voltage increases. This happens because the reverse conduction region voltage loss is getting lower.

The output voltage is rising until this voltage loss is minimized and no delay is between one transistor has finished turning off and the other has started turning on. The deadtime is adjusted so that it matches the turn-on and turn-off delays including actual rise and fall times for the given converter voltage and current conditions.

When we further decrease the deadtime transistors are starting to operate short circuited which results in steep decrease of the output voltage.

### C. Efficiency Measurement

In Fig. 9, the efficiency was measured at stable input voltage value and 0.5 duty cycle while changing the load current.

Two options were measured, first one with fixed deadtime roughly set to 40 ns to be bigger than estimated maximum delays in driving circuits and transistors. The second was measured with tracking deadtime algorithm running and constantly searching for the output voltage maximum at given load.

It can be seen that the tracking algorithm achieved higher efficiency in the measured converter power range.

In this particular case at 175 W, the efficiency values for both fixed and tracked deadtime are close which means the set fixed deadtime was optimal only for just this load power.

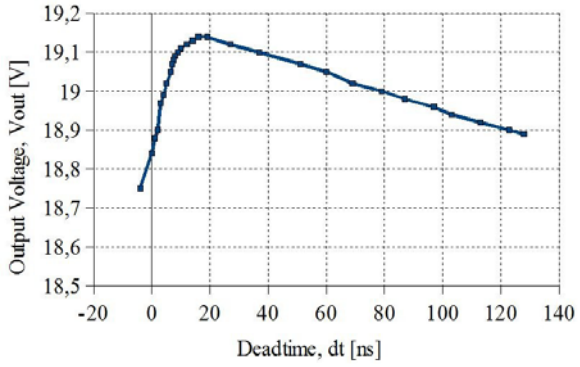


Figure 8. Output voltage on deadtime dependency

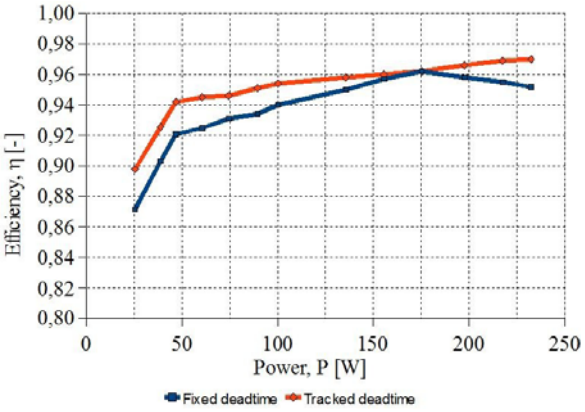


Figure 9. Comparison of efficiency depending on power for fixed and tracked deadtime

For lower and higher load the set deadtime is too short or too long increasing the losses in transistors while the tracking algorithm is still able to find the optimal deadtime again to keep the efficiency higher.

At low power the efficiency is decreasing because of the power consumption of the control circuit and drivers.

## V. Conclusion

The converter topology was tested to prove the existence of the output voltage maximum when changing the deadtime in case of constant and corrected duty cycle. It means the tracking algorithm is able to successfully find the maximum which is the optimum deadtime setting.

The tracking algorithm was tested and compared with the fixed deadtime setting. For the case of tracked deadtime the efficiency is higher over the whole range of varying converter output power compared to a fixed deadtime setting.

Adding the tracking algorithm to existing converter removes the need of measuring and precise setting the deadtime before new converter is put into operation.

The advantage of the proposed solution lies in that the only measuring of common values such as converter output voltage and current is enough to determine the mode of operation to correct the duty cycle and to implement the tracking deadtime algorithm.

## Acknowledgment

This work is supported by the Technology Agency of the Czech Republic under the grant for Competence Centre Programme, project No. TE02000103 and by the Czech Technical University in Prague under the the Student Grant Competition, grant No. SGS17/180/OHK3/3T/13.

## References

[1] K. J. Chen et al., "GaN-on-Si Power Technology: Devices and Applications," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 779-795, March 2017.

[2] G. Deboy, M. Treu, O. Haeberlen and D. Neumayr, "Si, SiC and GaN power devices: An unbiased view on key performance indicators," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2016, pp. 20.2.1-20.2.4.

[3] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 707-719, Sept. 2016.

[4] GaN Systems, "Bottom-side cooled 650 V E-mode GaN transistor," GS66508B Premiliary Datasheet, 2016.

[5] Y. Uemoto et al., "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," in IEEE Transactions on Electron Devices, vol. 54, no. 12, pp. 3393-3399, Dec. 2007.

[6] P. Williford *et al.*, "Optimal Dead-time Setting and Loss Analysis for GaN-based Voltage Source Converter," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 898-905.

[7] D. M. Joo, J. E. Byun, B. K. Lee and J. S. Kim, "Adaptive delay control for synchronous rectification phase-shifted full bridge converter with GaN HEMT," in *Electronics Letters*, vol. 53, no. 23, pp. 1541-1542, 9 11 2017.

[8] L. Schirone, M. Macellari and F. Pellitteri, "Predictive dead time controller for GaN-based boost converters," in *IET Power Electronics*, vol. 10, no. 4, pp. 421-428, 31 3 2017. doi: 10.1049/iet-pel.2015.0551

[9] N. Bizon, M. Raducu, M. Oproescu and L. M. Constantinescu, "Energy efficiency of the PV panels using a MPPT controller with improved search speed: Part I: Modeling of the PV power system under extremum seeking control," *2014 International Conference on Applied Electronics*, Pilsen, 2014, pp. 45-50.

[10] Skarolek, P.; Lettl, J. Current Limiting Driver for GaN Half-Bridge In: 22nd 2017 International Conference on Applied Electronics. Pilsen: University of West Bohemia, 2017. pp. 227-230.

[11] ST Microelectronics, STM32F334 Reference Manual, 2016.