Diagnostic Device for Photomultiplier Tubes at ARP ToF Detector

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***Abstract* - Long-term usage of photomultiplier tubes (PMTs) led to the discovery of aging effects especially in harsh environment as a radiation is. Aging decreases the efficiency of the PMTs. This means PMTs need to the recalibration after some time. Because CERN´s Large Hadron Collider (LHC) runs for few years, the diagnostics of the PMTs is necessary. Eventual recalibration without removing the PMT is possible to accomplish by integrating the light source nearby PMT´s chassis. The light source should by as precise as possible. The used LED source needs a driver. The driver consists of controllable power source and timing controller. The perfect timing of the pulses is controlled by FPGA. An attention to the radiation hardened parts was needed because of the device proximity to the radiation source. The development and testing of the PMT diagnostic device (PDD) are described in this paper.**

Keywords – FPGA; high energy physics; PMT; photomultiplier; LED driver; physical instrumentation; PWM; rad-hard

I. Introduction

The CERN is the place where particle detectors of different types are frequently used. Some of them use for the particle energy detection conversion to light. The PMTs of different constructions are the integral part of the signal chain. The light detected by the PMT is fed to an amplification chain. When in operation we do not have any information about the whole chain and its changes.

The time-of-flight (ToF) detector for forward physics based on the Cherenkov radiation used at the ATLAS ARP Experiment is one we deal with [1]. Its main purpose is to measure the particle momentum and reduce the background during the multiple p-p collisions. The ToF detector uses the microchannel plate (MCP) PMT [2]. After some time of continuous run, PMT shows signs of aging in a radiation environment. With help of the PDD we can take into account the corrections applied on the measured data.

Two phases were considered for diagnostics of the signal processing chain. The first was the diagnostics during the installation process to assure the proper chain function. The second one is the continuous diagnostics during the whole run of the detector.

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II. Device Architecture

The PDD is designed for last Roman Pot flange design where the MCP PMT is placed out of vacuum in the special tube. The MCP PMT and detector material, where Cherenkov light has an origin, is separated by the transparent window. The light from the diagnostic source is fed by four optical guides to the window and reflected to MCP PMT photocathode. The PDD should supply four optical guides with light signal.

Design should satisfy these specifications:

- Settable pulse energy
- Controllable pulse width and rate
- Minimal time resolution of 2.5 ns
- Able to run on external or USB power
- Communication by UART and I^2C

The PDD architecture is shown in Fig. 1. USB and I^2C buses are used for the PDD control via PC (installation process) or time-to-digital converter (TDC) module (ToF run). The communication interface is composed of UART/USB converter, signal filters and IO protection circuits.

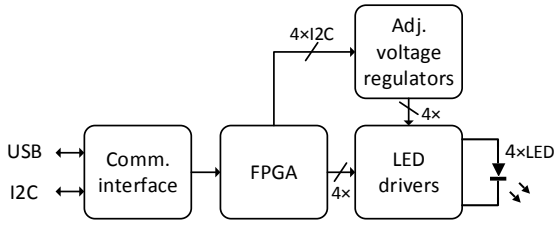

Figure 1. PDD block diagram

The FPGA, which acts as a main controller, receives and process the control commands and transmits data back to the master device. After the data processing the FPGA adjusts the voltage regulator output level for powering of the LED drivers. This adjustment affects the LED forward current. There is also a possibility to change the parameters (pulse width and switching frequency) of the PWM control signals for LED drivers.

Four UV LEDs are then used to produce the light pulses at the same wavelength as the Cherenkov detector and fed to the fiber-optic cables. The PDD

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itself is mounted approx. 2 m far from the Roman Pot near to the NIM crate with other modules for signal processing of ToF detector.

III. Hardware Desciption

Radiation hardened FPGA IGLOO 2 was chosen due to its ability to withstand the radiation dose of several hundred krad [3, 4].

Fig. 2 shows the IGLOO2 devkit designed and used during the PDD development process [5]. Beside of the FPGA itself the kit also implements the USB/UART converter, 4 LEDs, 3 push-buttons and two long pin headers with resistor network allowing many different signal standards (LVCMOS, LVTTL, LVDS, CML, LVPECL etc.).

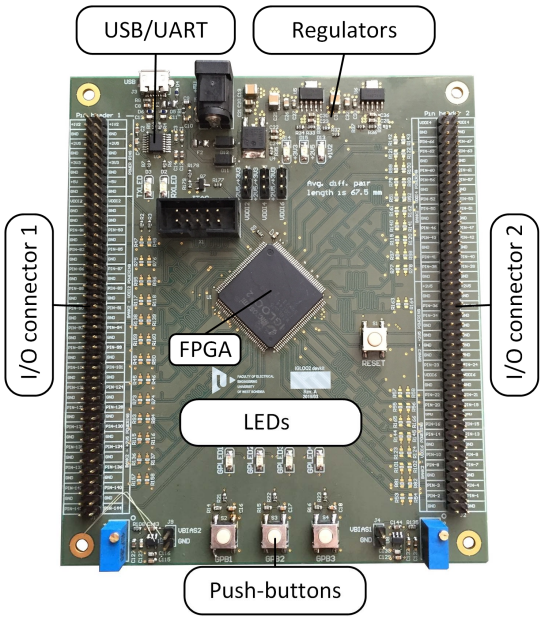

Figure 2. IGLOO2 development kit

The timing requirements for the LED pulse width and rate are following:

- 7 kHz to 100 kHz switching frequency
- 2.5 ns to 640 ns pulse width

Due to these challenging timing requirements (fine granularity and low minimal pulse width) the fast LED driver had to be developed.

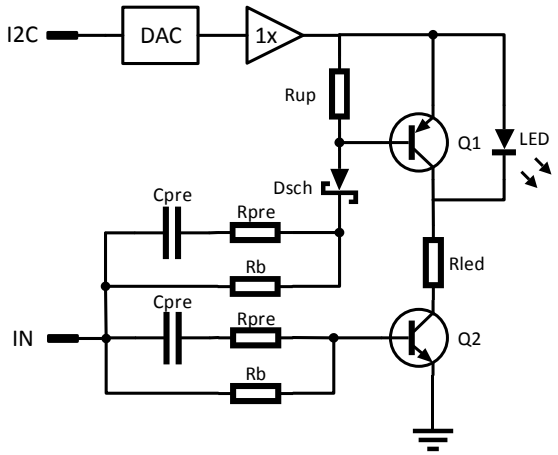

Figure 3. LED driver circuitry

Fig. 3 shows the LED driver circuit diagram. The push-pull driver is composed of high speed NPN and PNP transistors with f_T up to 7 GHz. The transistor switching is accelerated by the pre-emphasis circuits in which the R_b resistors set the continuous base current. The C_{pre} and R_{pre} affect the slope of the rising and falling edges of the control signal. R_{up} resistor contributes to fast turn off of the PNP transistor. As the IN signal level corresponds to LVCMOS3V3, and the push-pull driver power voltage level is ranging from the 3.5 V to 5 V, four serially connected Schottky diodes are used to shift the control signal voltage level of the PNP transistor. The power voltage level of the driver is set via I2C-controlled DAC and unity gain buffer because of the DAC limited output power. The LEDs should emulate the wavelengths of the original source in range from 200 nm to 400 nm (near UV) [6].

After the successful test of the PDD prototype a new PCB integrating the FPGA and LED drivers can be designed with respecting the required form factor.

IV. FPGA Firmware

The PDD Firmware was developed according to the previously mentioned requirements. Whole project was developed using IDE Libero SoC v12.3 from Microsemi.[7]. It was chosen due to the used FPGA IGLOO2. Source code is fully written in VHDL language. For interconnection of VHDL entities (as a top-level entity) Libero Smart Design was used.

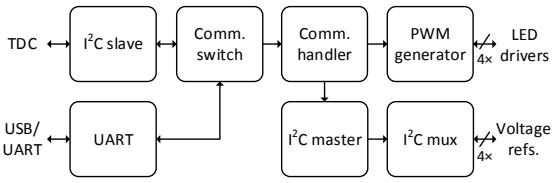

Figure 4 Block diagram of firmware

The diagram depicted in Fig. 4 consists of seven blocks described in the following sections.

A. I2C slave

The PDD works as a slave and responds to the commands sent by TDC (ToF run mode) or by Raspberry Pi during the test and debugging phase.

B. UART

This entity is to be used only during the ToF installation process. In this situation the PDD will be controlled manually by PC.

C. Communication switch

As mentioned above the device can communicate via UART or I2C. Without user input from UART interface the PDD works as I2C slave. During manual control through UART, the parent device (master), which controls the pulser by I2C, is physically disconnected. That makes impossible to receive data through I2C and UART at the same time and therefore the priority logic is not required.

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D. Communication handler

This entity decodes incoming data and consequently controls the other entities. Another function of the communication handler is to send requested data back to the master device.

The PDD is controlled by writing data into eight control registers by PC or other devices on I2C bus. These registers include control registers for PWM and four 8-bit DACs. One of these registers is status register.

Data written into the device are then read back by the parent device to make sure that correct data were received.

E. PWM generator

In the PWM entity there are 2 main registers used to set the pulse width and rate of the control signals. The first one is the 16-bit wide reload register. This register controls the rate of the control signals. The internal counter is reset when its value is equal to the reload register. A new PWM cycle is then started.

Pulse width is controlled by second register called compare register. When the internal counter reaches the value, which is stored in this register, the output value is toggled. For safety reasons (limiting of the maximum pulse width) this register is only 8-bit wide.

One of the most important features was implementation of the buffer (shadow) registers which are the same size as the main control registers. Values are firstly written into buffer registers, where they are stored until the end of the PWM cycle. When a new PWM cycle starts, these values are then transferred from buffer registers to the main control registers. This insures glitch less run.

Resolution of 2.5 ns is achieved by feeding the PWM entity with 400 MHz clock.

For a safety reason of the tested PMT and testing LEDs the maximal pulse rate is limited to 100 kHz. This limitation is done in multiple places within the FPGA design in order to avoid the error probability. This function is achieved by reading the received value at several points and by having a minimal value which can be written into reload register.

F. I2C master

Because of the external DACs, which are controlled by I2C, the PDD must also be able to work as I2C master.

DACs incorporated in this device use the simplest communication possible. During communication, 8-bit DAC expects to receive only one byte of data on the bus, which uses as value for the setting of the output voltage level.

G. I2C mux

Internally I2C master block is routed into multiplexer, which is then routed into four different pairs of FPGA pins. Multiplexer is needed because all of the four DACs have the same address and has to be on separate bus. This means that addressing is done by switching internal multiplexer and transmitting on different pins.

V. Added Safety Measures

In the remote-control mode is important to have all of the relevant information about the PDD status. This monitoring is done by the master device by reading the status register. This register indicates any error in the communication with DACs. This information can be used for diagnostic purposes if error occurs.

Another function of the status register is to indicate if I2C bus is busy and cannot send next command to DACs.

During the LHC testing period it is impossible to access the device for prolonged time. For this reason, many safety measures were implemented. One of these measures is automatic I2C timeout. After receiving the first byte of the command, the timeout counter is started. If the second byte is not received within defined time period, the whole entity is reset. This increases the reliability and decreases the chance for the communication to enter “dead lock” states due to the single-event effect or other unexpected reasons.

VI. Tests and Measurement

Raspberry Pi was used to test the I^2C slave block of the PDD firmware. By using of the Python script, whole test procedure could have been fully automated. This automatic test procedure assures the reliability of the I2C communication by repeatedly writing to and reading from the PDD control registers.

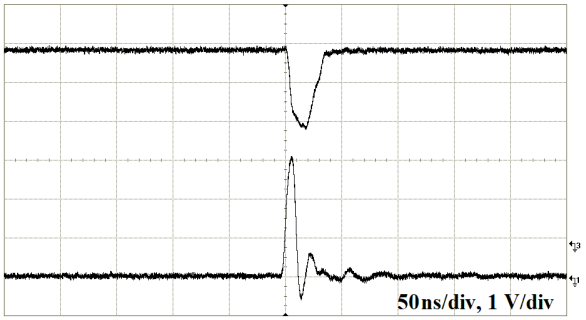

Figure 5. LED anode voltage (top) and driver control signal (bottom)

The oscillogram in Fig. 5 shows the waveforms. The lower one represents the control PWM signal which is common for PNP and NPN transistors. In this case the control signal pulse width is set to 10 ns. The upper waveform is the LED cathode voltage. It is obvious that the LED pulse width is significantly longer (approx. 25 ns). This 15 ns time difference is caused by the deep saturation (base/collector current ratio) of the NPN transistor. In order to achieve the same pulse width of the control signal and cathode voltage the driver voltage has to be reduced or the R_b increased. This means that the LED forward voltage (current respectively) has to be tuned in a relatively narrow range as the collector current is changing accordingly and the base current remains at the same level. The further improvement of pulse shape could be done by separate timing of NPN and PNP transistors.

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VII. Conclusion

During the test procedures the communication and data transfer via I^2C and UART buses were tested sufficiently. The tests of the relation between the control and LED cathode pulse widths emphasized the influence of the NPN transistor saturation depth. This phenomenon has to be taken into account during the change of the voltage level for powering of the LED driver. As the prototype version of the PDD was tested successfully a new fully integrated version of the PDD will be designed and then tested in the full ToF chain. This new PDD will be tested at synchrotron in DESY (Hamburg) and also in CERN before the installation at LHC accelerator.

Acknowledgment

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