Using an ANN Approach to Estimate Output Power and PAE of A Modified Class-F Power Amplifier

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Abstract – **In this paper, an efficient Class-F power amplifier (PA) is designed, simulated and modeled. This type of amplifier has nonlinear behaviors and uses tuning and controlling harmonics as the most important mechanism to increase efficiency. Feedforward artificial neural network (ANN) model is proposed to predict and estimate the nonlinear output of the power amplifier. The designed amplifier operates at 900 MHz, with 18 dB gain and 70 %Power-Added Efficiency (PAE). In the design process, the artificial neural network model is used to predict PAE and output power parameters as a function of input power, drain voltage and gate voltage of the applied transistor (DC Biasing voltages). The obtained mean relative errors (MREs) are less than 0.03% and 0.09% for the predicted output power and PAE parameters.**

Keywords-component; Artificial neural network; Class-F power amplifier; Power added efficiency (PAE)

I. INTRODUCTION

PAs are high power-consuming elements in communications. Therefore, efficiency is an important factor in amplifier design [1-4]. Switching power amplifiers are good choices for high-efficiency applications. Also, Class-F is a good choice of switching amplifier, because of its high efficiency. Class-F amplifier is the harmonic controlled type of amplifiers [5-7]. In another word, the switch voltage and current are formed using different harmonics in Class-F amplifier. The switch voltage is squared waveform, while the switch current is a half-sinusoidal waveform in the Class-F amplifier.

Usually analyzing of switching amplifiers leads to complex equations. In most cases, there is not any closed-form solution and the equations should be solved numerically. Therefore, designing of the switching amplifiers is a time-consuming procedure,

especially when the parasitic transistor elements are considered[2].

The Class-F amplifier is a circuit with output harmonic control circuit. This harmonic control circuit adjusts the harmonics in the transistor voltage and current waveforms to shape the transistor waveforms. The transistor squared voltage and half-sinusoidal current waveforms are shaped in the such way that they are not overlapped in the time domain, therefore, the efficiency of the amplifier will be increased. This advantage causes Class-F amplifier to be desirable choice in the high efficiency applications [8-10].

Artificial intelligence is an excellent solution to ease the design procedure and modeling in several engineering problems [11-15]. Also, ANNs have been used to model the power amplifiers [16-19]. There are several conventional ANN networks which are used in electronics filed, such as MLP (multilayer perceptron) [16] and spiking neural networks [20].

II. AMPLIFIER DESIGN

The block diagram of the Class-F PA is shown in Fig. 1(a). As seen, the PA has two matching networks, which transfer input and output impedances (50 ohms) to the desired values at the gate and drain of the applied transistor. These desired values obtained from source-pull and load-pull analysis. The output matching networks, not only transfer output impedance to the desired value but also control the harmonics in the circuit. The harmonics control circuit (HCC) is the important part in the Class-F PA. HCC passes even voltage harmonics and suppresses odd harmonics, so the voltage and current waveforms will be shaped as shown in Fig. 1(b). The drain voltage and drain current of a typical Class-F amplifier can be written as follows [21]:

$$V_D(\theta) = V_{DD} + V_m \sin(\theta) + V_{3m} \sin(3\theta) + V_{5m} \sin(5\theta)... \quad (1)$$

$$i_D(\theta) = I_D - I_m \sin(\theta) - I_{2m} \sin(2\theta) - I_{4m} \sin(4\theta)... \quad (2)$$

In equations (1) and (2), V_D and I_D stand for DC drain voltage and current, respectively. Also, V_{im} and i_{im} are the i_{th} harmonics drain voltage and current amplitude, respectively. Moreover, $\theta = \omega t$ and ω is the fundamental angular frequency.

The proposed amplifier is shown in Fig. 2. In the designed amplifier microstrip transmission lines (TLs), pHEMT transistor and capacitors are used. Transmission Lines TL1–TL3 is used as an input matching network and TL8–TL10 are used as output matching network, which works as harmonics control circuit (HCC) simultaneously. Transmission Lines TL4–TL5 are used as DC drain bias line. In this design 5 V, DC voltage is used for drain and -0.75 V, DC voltage is used for gate voltage. Transmission Lines TL6–TL7 are used as DC gate bias line.

Figure 1.   (a) Block diagram and (b) drain waveforms of typical Class-F PA
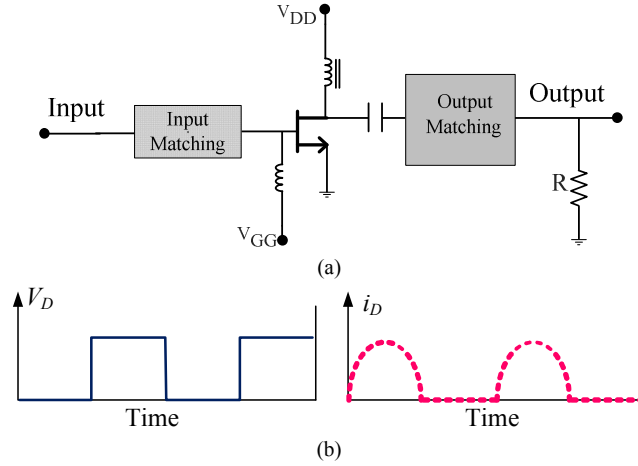

(a)

(b)

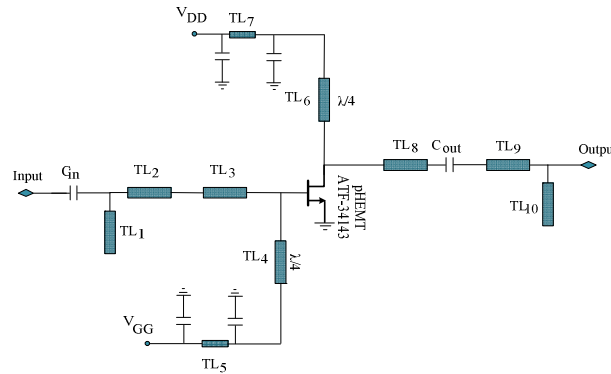Figure 2.   The schematic structure of the designed Class-F amplifier.

TABLE I.   DESCRIPTION OF THE APPLIED PARAMETERS

Parameter	Discription
V_{DD}	DC voltage for the drain of the amplifier
V_{GG}	DC gate voltage for the gate of amplifier
V_D	Drain voltage of the transistor
i_D	Drain Current of the transistor
V_{im}	Magnitude of the ith voltage harmonic
V_{im}	Magnitude of the ith current harmonic
C_{in}	Capacitance at the input of the amplifier
C_{out}	Capacitance at the output of the amplifier
Tl_i	Index for the ith transmission line

Description of the applied parameters in the paper is listed in Table I. According to the circuit of the proposed amplifier, the LC equivalent circuit (LCEC) of the amplifier is extracted, which is shown in Fig. 3. In the presented LCEC, the inductors and capacitors

are named corresponding to the transmission lines TL1–TL10. The amplifier layout, based on the circuit schematic diagram, is shown in Fig. 4. The scattering parameter (S21) of the designed Class-F amplifier is shown in Fig. 5. The scattering parameters for a device describe the electrical behaviour of a linear device, which can be defined by a matrix. For a two port amplifier scattering parameters can be written in a 2×2 matrix. In the small signal condition, the amplifier can be assumed as a linear device, so the S21 parameter shows the small signal gain of the amplifier. The achieved small signal gain shows good performance of the proposed amplifier at 900 MHz frequency. The value of small-signal gain, at the main frequency, is about 18 dB. The gain and PAE parameters are shown in Fig. 6. As seen, the large signal gain of the proposed

PA is about 17.7 dB, which confirmed the small-signal gain value. The PAE of the designed amplifier is about 70 % for 15 dBm input power at 900 MHz frequency. The amplifier output power at main frequency is depicted in Fig. 7. As seen in this figure, the 1-dB point of the designed PA is about 30 dBm, which shows an acceptable linear operating range. Fig. 8 shows the drain waveforms of the amplifier. As seen the drain voltage and current are approximately square and half-sinusoidal waveforms.

III. NEURAL NETWORK MODELING

As mentioned, the artificial neural network is the proper technique to model electrical devices such as microwave devices and power amplifiers. The parameters which are considered for the input of the neural network are 1- input power Pin(dBm), 2- DC gate bias voltage Vg (V) and DC drain bias Vd (V). Also, the parameters which are considered for output of the neural network are 1- output power Pout(dBm) and 2- power-added efficiency (%). The considered neural network for modeling of the amplifier is shown in Fig. 9.

The multi-layer perceptron (MLP) neural network is considered in this paper to model the power amplifier. The presented MLP in this paper consists of two hidden layers with five and six neurons in the first and second hidden layers, respectively. Fig. 10 shows the architecture of the proposed MLP network. The proposed ANN ran more than 200 times and then the corresponding values of MRE for test data are reported in Table II.

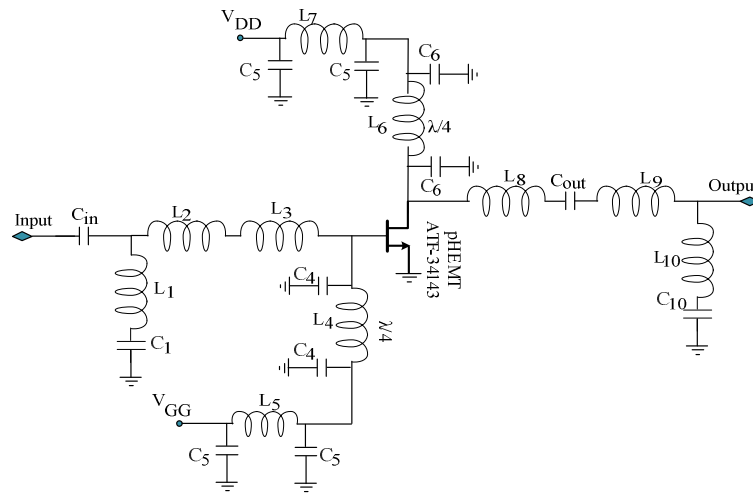Figure 3.   The LCEC of the designed Class-F amplifier.

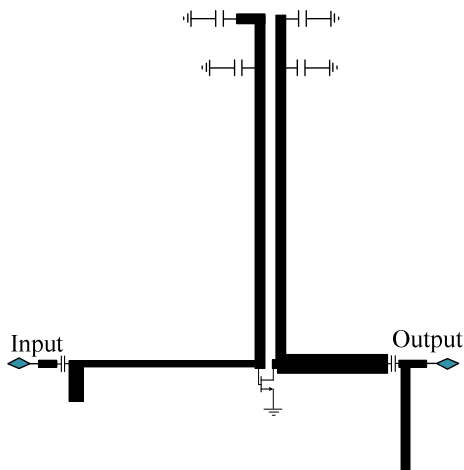Figure 4.   The layout of the designed amplifier

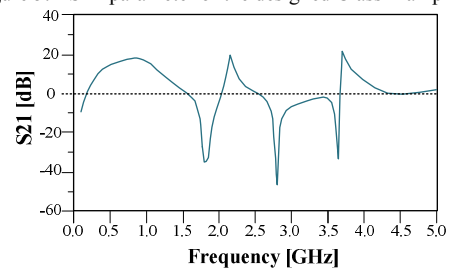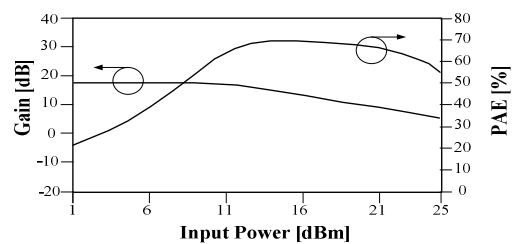Figure 5.   S21-parameter of the designed Class-F amplifier.

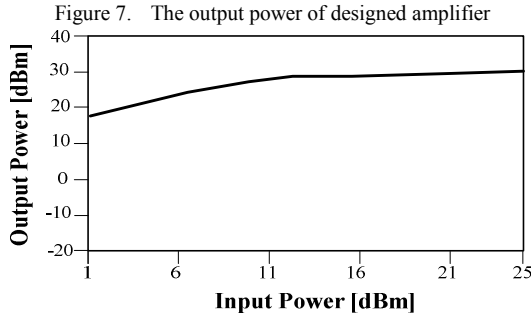Figure 6.   The gain and PAE parameters of the designed Class-F amplifier at 0.9 GHz.
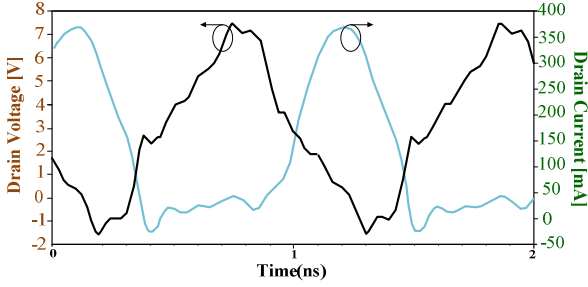
Figure 7.   The output power of designed amplifier

Figure 8.   The drain waveforms of the amplifier.

The mean relative error (MRE) percentage is written as follows.

$$\text{MRE} = \frac{\sum_{i=1}^{N}\left|Y_{\text{Re}i} - Y_{\text{Pr}i}\right|/\left|Y_{\text{Re}i}\right|}{N} \times 100 \qquad (3)$$

where, in this equation "Y" represents the data value and "N" is the total data number. Also, the "Re" and "Pr" indices represent the real and predicted values. 171 data are considered for train and 57 data are considered for the test process of the modelling.

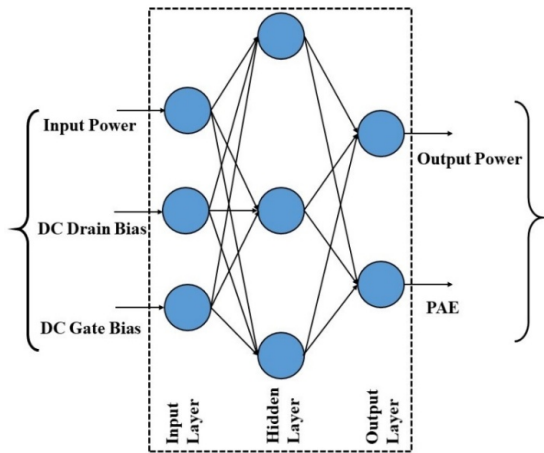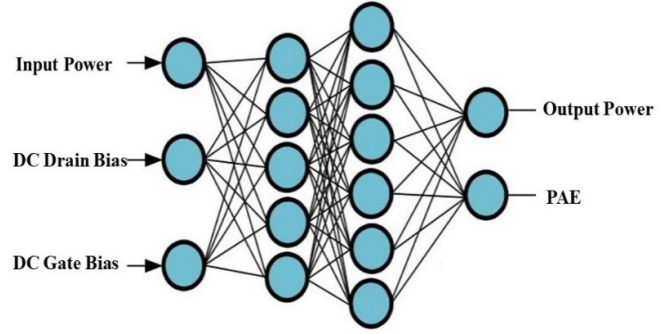Figure 9.   Considered neural network for modelling of the amplifier

Figure 10. Arcitecture of the proposed MLP neural network model


The regression diagrams for the predicted and real values of the output power in the proposed model are depicted in Fig. 11. The Real and predicted output power in the presented model is depicted in Fig. 12.

TABLE II.   THE RESULTS OF THE PROPOSED MODEL FOR TRAIN AND TEST PROCEDURES

Error-values	P_{out}(dBm)	PAE (%)
MRE Train %	0.03	0.09
MRE Test %	0.04	0.23

Figure 11. Regression diagrams for the predicted and real values of the output power in the proposed model: (a) Train and (b) Test steps.

Train

(a)

Test

(b)
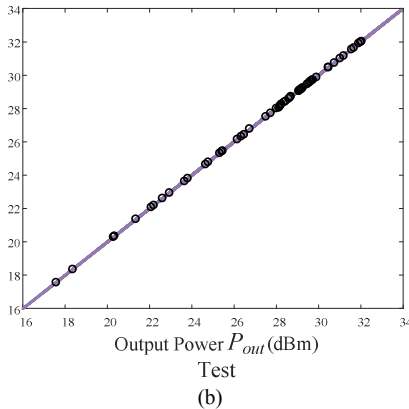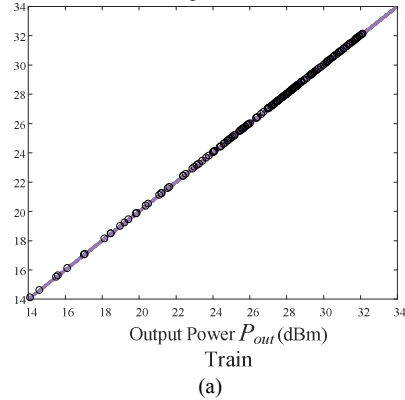
Real and predicted power added efficiency and output power for drain voltage of 5 V and gate voltage of -0.75 V is illustrated in Fig. 12. As can be seen in this Figure, the ANN has predicted the power added efficiency and output power precisely.

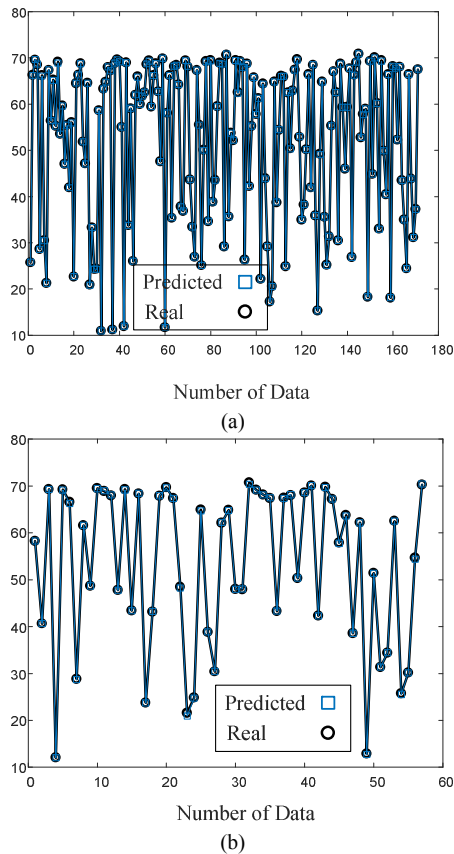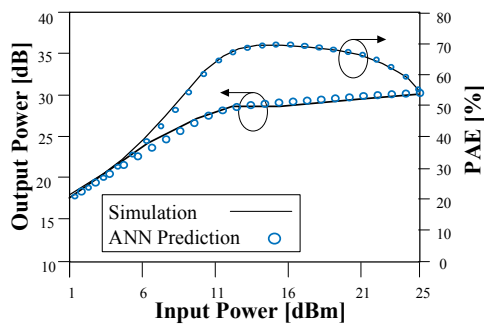Figure 12. Real and predicted power added efficiency in the proposed model: (a) Train and (b) Test steps.

(a)

(b)

Figure 13. Real and predicted power added efficiency and output power

IV. CONCLUSION

A Class-F PA is designed and modeled using neural networks. The proposed neural network model can predict the amplifier parameter correctly. The predicated parameters of the amplifier are close to the real values. Finally, the mean relative errors of the predicted parameters are calculated which are less than 0.03% and 0.09% for the predicted output power and PAE parameters.

V. ACKNOWLEDGMENT

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