Streamlined Fibonacci Charge Pump

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***Abstract* – This paper is devoted to questions of the efficiency increase of the Fibonacci charge pump (FCP). The main attention is dedicated to discovering the mechanism of the power losses in the given FCP structure. The FCP after reduction of the power losses has a flatter efficiency characteristic than the original FCP structure. Thus, the efficiency of the streamlined FCP is a greater than 70 % in a wide range of the output current (from 1.5 mA to 10 mA approx..) when the input voltage is 3 V and the designed output voltage is greater than 30 V.**

Keywords-Fibonacci charge pump; diode voltage drop; shoot-through current of an inverter.

I. INTRODUCTION

Charge pumps are a low-power alternative to DC/DC converters with inductors that produce a voltage higher than input voltage or a voltage of opposite polarity to the input.

A well-known variant of the charge pump is a Dickson charge pump (DCP) [1], [2]. The Dickson charge pump structure is optimized to a monolithic realization and a high efficiency. The main disadvantage of DCP is a relatively low voltage gain which is equal to an amplitude of the used clock. Thus, the number of stages must be relatively high for high output to input voltage ratio. For example, we must use 12-stage DCP for realization output to input voltage ratio 13, in an ideal case.

One variant of a charge pump with a higher voltage gain is a Fibonacci charge pump (FCP) [3], [4], [5]. In this architecture, stages have variable voltage gain defined as a Fibonacci number (1, 1, 2, 3, 5, 8, …). For example, we use 5-stage FCP for realization output to input voltage ratio 13, in an ideal case.

The main disadvantage of FCP is an increased sensitivity to parasitic capacitors than DCP. Thus, the FCP concept is recommended for lower frequencies than DCP [4], [5], [6] only.

II. STUDY OF FCP POWER LOSSES

The original FCP was designed in [6] for power supply voltage $V_{IN} = 3$ V and the minimal steady-state output voltage $V_{OUT} = 30$ V at the output current $I_{OUT} = 1$ mA. The auxiliary parameters were maximal ripple voltage of the output $V_R = 15$ mV and the maximal rise time of the output $t_R = 65$ ms.

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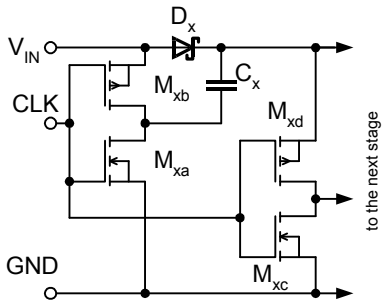

Figure 1. The one stage of the original FCP structure [6].

The original FCP structure [6] uses passive Schottky diode switches and active MOS switches working as an inverter according to Fig. 1. See Table I for their types and parameters.

TABLE I. DEVICE PARAMETERS OF ORIGINAL FCP [6], [7]

Parameter	**Value or device**
Load capacitance and transfer capacitance	$C = C_L = C_T = 2.2$ µF
Clock frequency	f = 33 kHz
NMOS transistor	2N7002 ($V_{DSS} = 60$ V, $V_{GS(th)} = 2.1$ V)
PMOS transistor	BSS84 ($V_{DSS} = -50$ V, $V_{GS(th)} = -1.7$ V)
Schottky diode	PMEG4010BEA ($V_{RRM} = 40$ V, $V_D = 0.155$ V)

The power losses of the original FCP structure [6] may be distributed to the three main parts:

- Presence of auxiliary inverters M_{xc}, M_{xd} (see Fig. 1) leads to the generation of a shoot-through current. Thus, the capacitor connected to the appropriate node is discharged by this shoot-through current [7].
- These auxiliary inverters generate the propagation delay that is gradually increased from the input to the output of the charge pump. The timing discrepancy between the stages may cause a loss of a charge. This effect is important only for a high clocking frequency [7].
- The voltage drop and a finite resistance of used diodes (see Fig. 1) leads to decreasing of the result voltage gain.

The power losses invoked by auxiliary inverters are gradually depended on the clock frequency. The study of clock frequency influence to parameters of presented FCP was performed in the previous period

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[7]. The results of this study fully verified this premise. But, no action for decreasing switching and timing losses was executed. The power losses of diodes didn't solve previously, too. The result new structure uses two techniques of decreasing power losses that are discussed in the next text.

III. Decreasing Voltage Drop of Diodes

The decreasing power losses of diodes is relatively easy to realize. This way does not require a complicated reconstruction of the circuit solution. A suitable type of diode is selected according to datasheet parameters or by DC sweep analysis performed by a circuit simulator. We select Schottky diode of type PMEG2010AEB as more suitable than original diode type PMEG4010BEA. See Table II (I_F is the forward current, V_F is the forward voltage). The reverse voltage for PMEG2010AEB is $V_R = 20$ V and for PMEG4010BEA is $V_R = 40$ V.

TABLE II. Voltage Drop of PMEG2010AEB vs. PMEG4010BEA (T_{AMB} = 25 °C) from Datasheet

I_F (mA)	PMEG2010AEB V_F (mV)	PMEG4010BEA V_F (mV)
0.1	typ. 30, max. 60	typ. 95, max. 130
1	typ. 80, max. 110	typ. 155, max. 210
10	typ. 140, max. 190	typ. 220, max. 270
100	typ. 230, max. 290	typ. 295, max. 350

The voltage drop at low currents is very important because for the original design the average forward currents of diodes are about (the symbol D_x indicates diode in stage x): 16 mA (D_1), 9.9 mA (D_2), 5.9 mA (D_3), 3.8 mA (D_4), 1.6 mA (D_5 and D_6) at output current I_{OUT} = 1.6 mA (R_L = 20 kΩ) for example. The reverse voltages of used diodes are about: 2.8 V (D_1), 5.5 V (D_2), 8.6 V (D_3), 14 V (D_4), 21.8 V (D_5), 13.8 V (D_6) at no-load output.

IV. Decreasing of Switching Losses

One possible way of decreasing shoot-through current is a decreasing of the channel conductivity of transistors. But in discrete technology, change of geometry of transistor is impossible. Thus, the conductivity of a transistor channel may be decreased by regulation of a gate voltage. The gate voltage of transistor gradually increases by stages. For example, the first stage uses the gate voltage with amplitude 3 V. But the 5th stage uses the gate voltage with an amplitude about 20 V. Thus, decreasing of the gate voltage is the most important for stages close to output, because these stages work with relatively high drain voltages and combination of a high voltage and a high channel conductivity leads to a high value of a shoot-through current.

The simplest way of decreasing a gate voltage is a usage of a capacitor divider according to Fig. 2. The first capacitor C_1 in the divider is realized as a new element, but a parasitic capacitance of MOSFET gate C_2 is used as the second capacitor. The last element is the discharging resistor R_D.

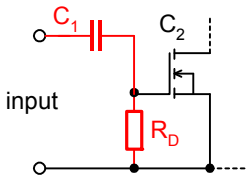

Figure 2. The capacitor divider.

The capacitor divider is used for NMOS transistor only because this solution is a relatively easy (all NMOS transistor have a source terminal connected to ground) and an absolute value of gate voltages of NMOS transistors are higher than for PMOS transistor.

V. Verification of Results by Simulations

The new FCP structure uses both techniques for decreasing power losses. The schematic diagram of the new 5-stage FCP is shown on Fig. 3.

Firstly, the effect of the voltage drop of diodes were studied independently on the second technique. Thus, elements with red color was excluded (capacitors C_{3a}, C_{3c}, C_{4a}, C_{4c}, and C_{5a} are replaced by short circuits). We used diodes D_1 to D_4 and D_6 of type PMEG2010AEB. But, the diode D_5 was type PMEG4010BEA (the design wanted a greater reverse voltage). Diodes D_1 and D_2 were parallelized for decreasing voltage drop because these diodes worked at relatively high forward current. Practically, we used three parallelly connected diodes for D_1, D_{11}, D_{111} and two parallelly connected diodes for D_2, D_{22}.

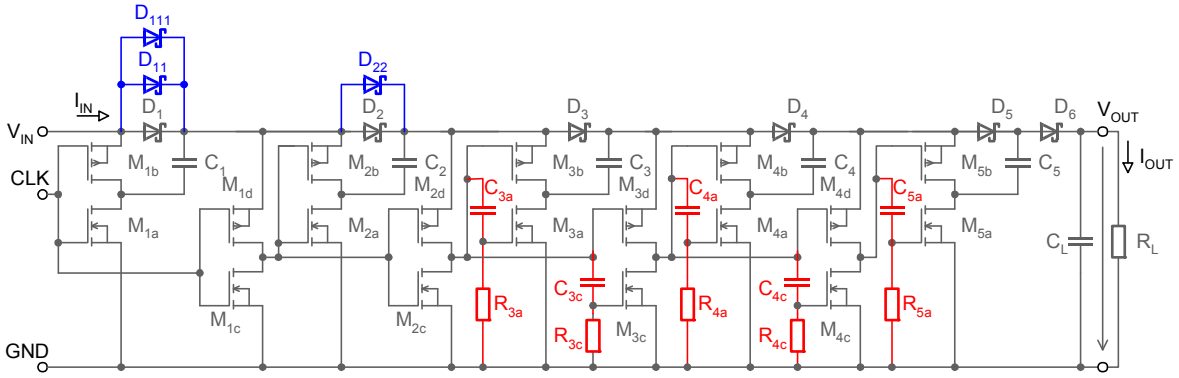

Figure 3. Schematic diagram of the new 5-stage FCP.

The effect of the new type of diodes is evident from Fig. 4 and Fig. 5 when we compare #1 and #2 courses. The efficiency characteristic (Fig. 4) is flatter than for the original solution, load characteristic (Fig. 5) reports a higher voltage at the same current than for the original solution.

The presence of diodes with a low voltage drop increases efficiency for output current greater than 2 mA. In a low output current area, the efficiency of the original solution is greater than the solution with low voltage drop diodes. This fact is caused by a shoot-through current of used transistor inverters.

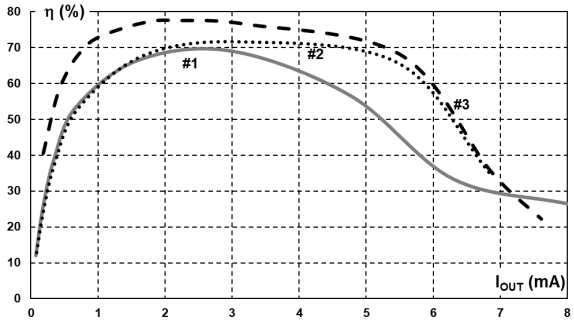

Figure 4. Efficiency vs. output current (simulations): #1 original solution, #2 effect of low voltage drop diodes only, #3 new solution.

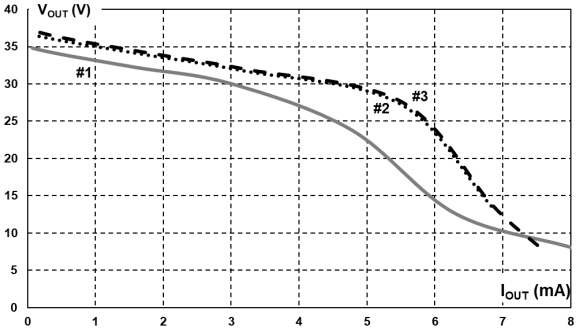

Figure 5. Output voltage vs. output current (simulations), for legend, see Fig. 4.

Secondly, the gate voltage regulation circuit was verified by simulation. The output V_{OUT} voltage of a capacitor divider according to Fig. 2 is defined as [8] (V_{IN} is the input voltage):

$$V_{OUT} = V_{IN} \frac{C_1}{C_1 + C_2} \tag{1}$$

The key question is a selection of the value of C_1 capacitance because the parasitic capacitance of MOSFET (transistor 2N7002 has the typical input capacitance $C_{iss} = 31$ pF and reverse transfer capacitance $C_{rss} = 3.5$ pF) has a nonlinear dependence on the gate and drain voltages. A too low value of capacity decreases voltage gain, but a too high value of capacity does not affect on decreasing shoot-through current. Thus, values of the capacity of C_1 capacitor was estimated after some runs of simulations.

The discharging resistor R_D has a relatively high resistance. Thus, this resistor consumes very small current. Values of all devices for the structure of the new 5-stage FCP are summarized in Table III.

TABLE III. DEVICE PARAMETERS ACCORDING TO FIG. 3

Parameter	**Value or device**
Load capacitance and transfer capacitance	$C = C_L = C_T = 2.2$ μF
Clock frequency	f = 33 kHz
Transistors	2N7002 (NMOS), BSS84 (PMOS)
Diodes	PMEG2010AEB, PMEG4010BEA (D_5)
Resistors R_{3a}, R_{3c}, R_{4a}, R_{4c}, R_{5a}	10 MΩ
Capacitor C_{3a}	1 nF
Capacitor C_{3c}	470 pF
Capacitor C_{4a}	330 pF
Capacitor C_{4c}	180 pF
Capacitor C_{5a}	100 pF

Table IV compares effective values of the drain current of all NMOS transistor for three cases: original structure [6] (#1), original structure with low voltage drop diodes (#2) and new structure (#3, see Fig. 3, capacitor values were according to Table III). We can see that a simple change of diodes let to increasing shoot-through currents, but the application of capacitive divider saves efficiency for high current and increase efficiency for a low current too because the shoot-through current is decreased at the same time.

TABLE IV. SIMULATED EFFECTIVE VALUES OF SELECTED CURRENTS (#1 ORIGINAL SOLUTION, #2 ORIGINAL SOLUTION WITH LOW VOLTAGE DROP DIODES, #3 NEW SOLUTION)

Current (mA)	**#1**	**#2**	**#3**
Id(M1a)	15.37	16.97	15.21
Id(M1c)	2.07	2.12	2.15
Id(M2a)	11.08	11.94	10.37
Id(M2c)	3.38	3.50	3.08
Id(M3a)	10.73	12.04	7.33
Id(M3c)	7.59	8.41	3.48
Id(M4a)	21.33	23.71	5.24
Id(M4c)	16.66	18.39	4.40
Id(M5a)	9.65	10.66	3.47

VI. VERIFICATION OF RESULTS BY MEASURING

The new structure of 5-stage FCP was verified by measuring in the circuit according to Fig. 6. All ammeters and voltmeters measure the average value of a current or a voltage [9], and the input and output voltages in the steady-state are close to DC. The efficiency is defined by (2) [8].

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\,\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\,\% \tag{2}$$

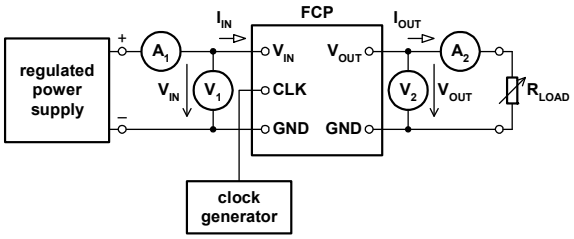

Figure 6. The circuit for V_{OUT} and η measuring.

The measured results of the original [6] and the new solutions (see Fig. 3) are confronted in Fig. 7 and 8.

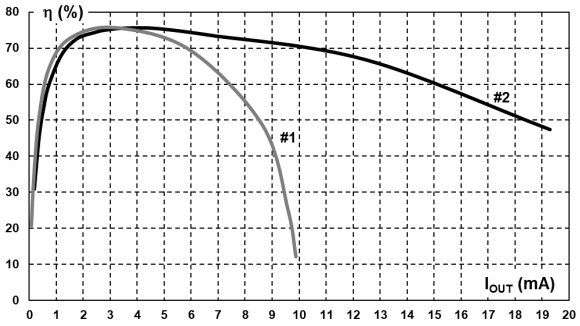

Figure 7. Efficiency vs. output current (#1 original solution according to [6], #2 new solution according to Fig. 3).

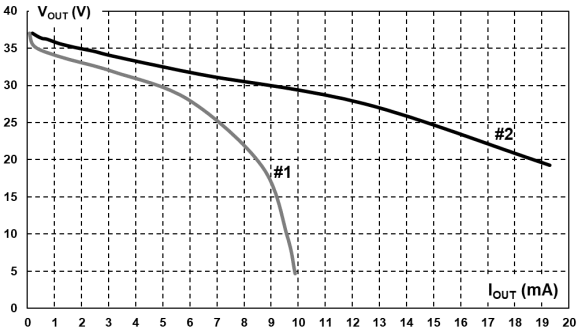

Figure 8. Output voltage vs. output current (for legend, see Fig. 6).

VII. Conclusions

The original solution has the efficiency higher than 70 % in a range of the output current approx. 1 mA to 6 mA. But the new solution has the efficiency greater than 70 % in a wider range of the output current approx. from 1.5 mA to 10 mA. Similarly, the equivalent series resistance of the new solution is about 1.5 times lower than the original solution for the output current I_{OUT} =1 mA.

For the new solution, maximal value of the efficiency is $\eta = 75.4\ \%$ at $V_{OUT} = 32.7$ V and $I_{OUT} = 4.7$ mA and for the nominal output current $I_{OUT} = 1$ mA the output voltage and the efficiency are $V_{OUT} = 35.9$ V, $\eta = 65.6\ \%$.

Thus, the described technique of decreasing a voltage drop of used diodes and decreasing switching losses of MOSFETs leads to increasing the efficiency and decreasing the output series resistance in the wide range of the output current.

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