Feasibility study towards increasing efficiency of fully on-chip DC-DC boost converter

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***Abstract*—In this paper, an investigation of the efficiency of fully on-chip DC-DC step-up converter realized in a standard 130 nm CMOS technology is presented. The converter has been designed for regulated output voltage of 1.2 V with an on-chip inductor and an output capacitor. The obtained results show that the proposed on-chip converter can achieve the efficiency up to 98 % and the output power up to 6 mW. The performed analysis investigates possibilities for the further improvement focused on the maximum efficiency and output power.**

Keywords— integrated inductor, on-chip inductor, step-up, DC-DC converter, boost converter

I. Introduction

Trends on today's market of electronic devices are focused on more efficient and low-cost devices. Therefore, it is crucial to find new, advanced, miniaturized, portable, battery-powered and low-power approaches in semiconductor industry. Scaling of CMOS technologies is one way to fulfil these requirements, since it allows devices to occupy smaller area and operate in higher frequency region or with less power consumption. With reduction of power consumption and increased demand for portable devices, the alternative methods of power supply such as energy harvesters are introduced [1]. These power harvesters, often offer only low value of the voltage output that might be insufficient for proper functionality of integrated circuits (IC) [2]. Because of this limiting aspect, requirements for preferable power management is rather obvious. Power converters commonly use external parts as capacitors or inductors. Their size, weight and cost are limiting for the use of the whole system. With further scaling of technology, integration of the entire power converter is therefore needed.

One of the common issues of integrated inductors include parasitic capacitances and resistances causing high energy losses. These parameters, resulting from the technology itself, strongly affect inductance and quality factor of an integrated inductor [3], [4], [5]. Desired conversion ratio, operating frequency and the efficiency are therefore limited.

This paper focuses on investigation of the maximum theoretical conversion efficiency and output power of an on-chip DC-DC boost converter with an integrated inductor driven by the pulse width modulation (PWM) circuit. In order to investigate impact of inductor properties (L and Q) on converter efficiency, we consider ideal PWM control circuit and all switches in the preformed analysis. Characteristics of the proposed inductor are introduced in Section II. Topology of the monolithic DC-DC step-up converter is described in Section III. In Section IV, achieved results obtained by simulation are presented. Last section discusses the improvement of the real inductor characteristics considering the achieved results.

II. Integrated inductor

Inductor used in the presented design is based on the integrated inductor implemented in a standard 130 nm CMOS technology proposed in [6]. Inductor shape is square spiral implemented in 5 metal layers with 5 rounds and dimensions 1.16 mm x 1.16 mm.

This paper further expands the theoretical usage of the proposed inductor. Characteristics of the inductor were evaluated by measurement in the frequency range from 50 MHz to 500 MHz. Method of evaluation was two-port differential measurement with floating center tap (Port 3). Extracted equivalent scheme of the inductor was then constructed using Y-parameters and adopted for simulations. The modeling and measurement methodology for the alternative schematic of the inductor was presented in [7], and the used model is shown in Fig. 1. Fig. 2(a), Fig. 2(b) and Fig. 2(c) show series resistance, inductance and quality factor respectively, with comparison to the measured values. Fig. 2(d) shows product of multiplication of inductance and quality. This parameter shows the middle course of two parameters. The maximum deviation

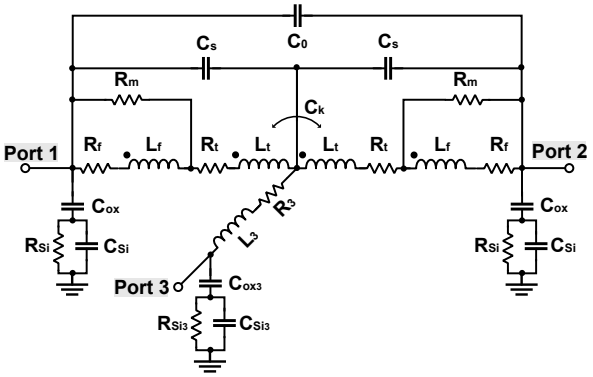

Fig. 1. The inductor model

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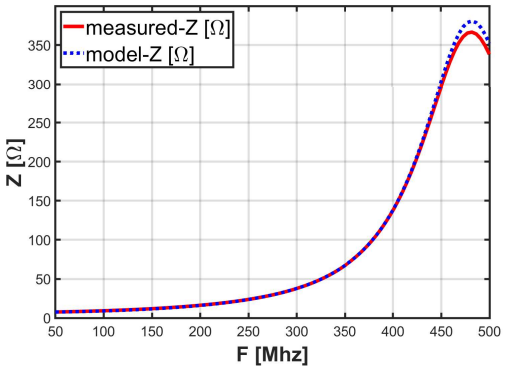
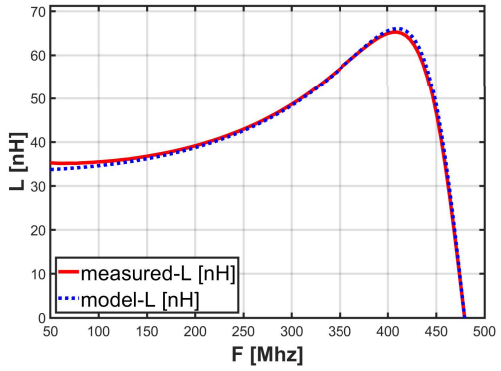
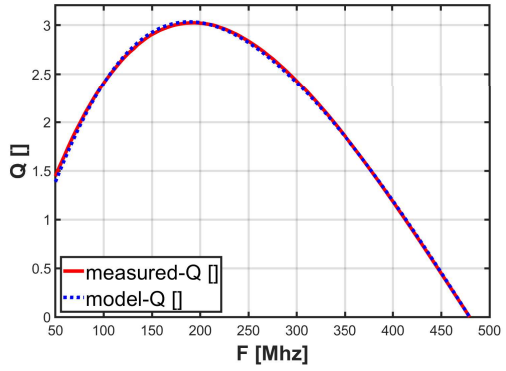


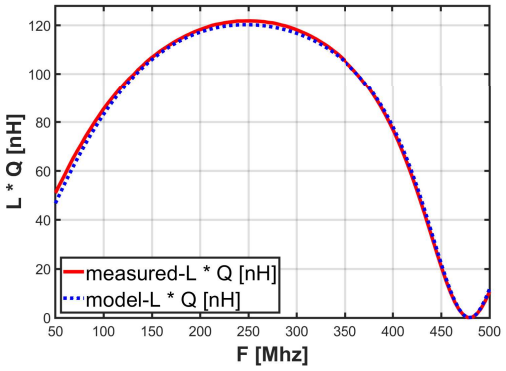
(a) Series resistance



(b) Inductance



(c) Quality factor



(d) Inductance multiplicated by quality factor

Fig. 2. Main characteristics of the integrated inductor

(obtained by simulation) of characteristics of the proposed inductor model from the measured values is 4.4 %. The inductance value at the maximum point of curves from Fig. 2(b), Fig. 2(c) and Fig. 2(d) was then captured and used in the simulations of the converter efficiency. Values of quality factor were chosen with respect to technology and another sources [8].

III. Proposed Converter Topology

The topology used for DC-DC step-up converter is a conventional boost converter. General schematic is shown in Fig. 3. The only non-ideal component in the schematic is inductor with its parasitic series resistance. Linkage of inductance, quality and series resistance of inductor was considered as follows:

$$Rs = \frac{2\pi f L}{Q} \tag{1}$$

All other components in the schematic are ideal. Ideal switches SW1 and SW2 control charging and discharging phases of the inductor, capacitor C is a filter capacitor while R_{load} represents load of the converter. It is important to note that SW1 is controlled by a signal from PWM circuit, while the SW2 behaves like an ideal diode with zero threshold voltage. Therefore, in schematic, it is replaced by diode D1. On account of using ideal components, the calculation of exact chip area is hardly possible. However, with surface of 1.3456 mm^2, the inductor will occupy significantly larger area than other parts of the converter.

The output signal from boost converter working in discontinuous conduction mode (DCM) can be divided into three phases. In the first phase, SW1 is on and SW2 is off. The voltage over the inductor is equal to the voltage Vin and current over the inductor is increasing. This current flows through SW1 into ground and in the same time, the filter capacitor discharges into load. In the second phase, SW1 is off and SW2 is on. The inductor acts like a current source and discharges into load and C1. In the third phase, SW1 and SW2 are both off. There is no current flowing through the inductor. Continuous conduction mode (CCM) is similar to DCM in the first phase. However, current through the inductor in the second phase never falls to zero. Therefore, the third phase never happens in the CCM. The power converter with the switched inductor commonly operates in CCM at higher frequencies.

IV. Achieved Results

In the analysis, we focused on finding the highest possible efficiency of power converters achieved for different inductor properties. For all simulations, the input voltage value is 0.6 V and filter capacitor with capacitance of 5 nF is used. The load was simulated with an ideal current source with current values in the range from 0.25 mA to 5 mA. Conversion ratio of the power converter is 2. Three different values of inductance and quality were chosen for the ideal inductor with series resistance, resulting in 9 simulations in total. Values of inductance were L_1 = 36.871 nH, L_2 = 42.431 nH and L_3 = 66.086 nH, based on values of inductance of the measured inductor. Chosen values

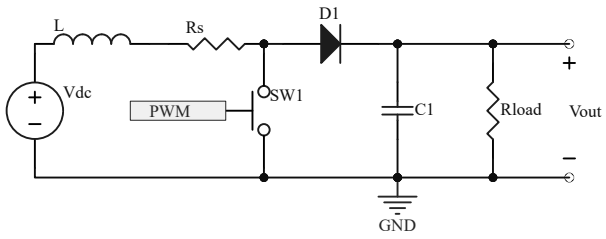


Fig. 3. Basic schematic of DC-DC step-up converter

of quality factor for inductor were Q_1 = 3, Q_2 = 9 and Q_3 = 15, based on the proposed inductor and inductors in [8]. All configurations were designed and simulated using Cadence environment with frequency in the range from 100 MHz to 800 MHz and for 130 nm CMOS technology. Simulations settings are summarised in Table I.

Tab. I. Simulation Parameters

Parameter	Unit	Parameter Value
Input Voltage	V	0.6
Conversion Ratio	-	2
Output Voltage	V	1.2
Output Current	mA	$0.25 \div 5$
Frequency range	MHz	$100 \div 800$
Quality factor	-	3, 9, 15
Inductance	nH	37.871, 42.431, 66.086

Results from simulations of the schematic model of on-chip inductor are displayed in Fig. 4. The maximum point of the efficiency is between 100 MHz and 200 MHz, which corresponds with the output power around 0.5 mW. The maximum output power is achieved at 100 MHz and corresponds with the efficiency under 15 %.

Results of ideal inductor with its series resistance are displayed in Fig. 5 and Fig. 6. Fig. 5(a) shows the maximum values of power conversion efficiency with corresponding output power while Fig. 5(b) shows the maximum output power with corresponding efficiency of DC-DC step-up power converter. For evaluation, we choose L/Q parameter, from which the series resistance of the inductor can be calculated using equation 1. From Fig. 5(a) and Fig. 5(b), one can observe that the power converter efficiency is indirectly proportional to the output current. The efficiency is highest around 200 MHz to 300 MHz at lower L/Q ratio what corresponds with low series resistance. Frequency of maximum point is close to value of peak of multiplication of inductance and quality factor shown in Fig. 2(d). The highest output power, displayed in Fig. 5(b), can be possibly reached in the range from 100 MHz to 200 MHz, however, at lower efficiency values under 70 %.

Fig. 6 shows the maximum power efficiency dependent on frequency for different inductance and quality values, and therefore, for different series resistances. All curves show peak efficiencies between 180 MHz and 250 MHz. From the maximum point, curves show almost linear decreasing trend. This

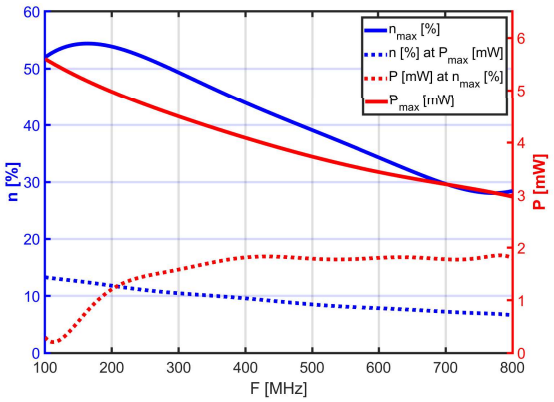
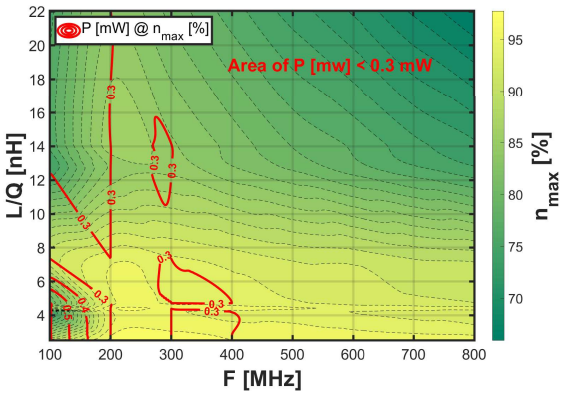
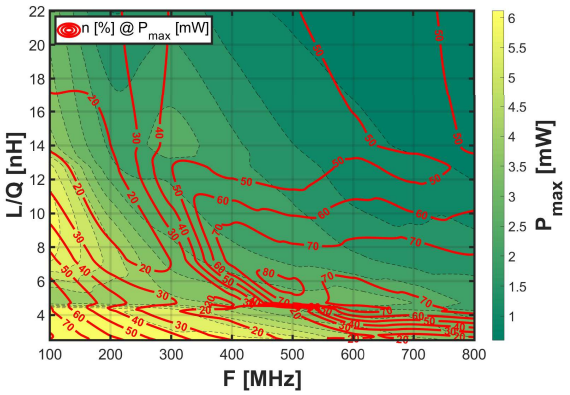


Fig. 4. Maximum power conversion efficiency and output power of model of the real inductor



(a) Maximum power conversion efficiency



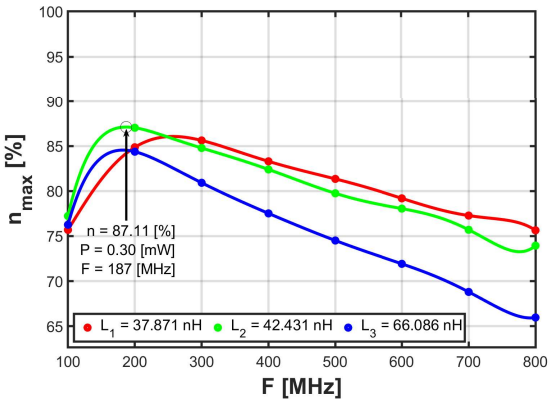
(b) Maximum output power

Fig. 5. Characteristics of the ideal integrated inductor

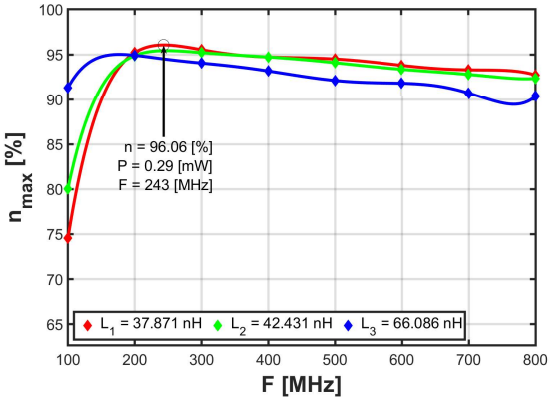
is probably due to series resistance which has the strongest impact on power dissipation at highest inductances and lowest quality factors. Best overall performance circuit displays at highest quality factor and lowest inductance value meaning lower series resistance, which was expected. All significant results of simulations are summarized in Table II.

V. Conclusion

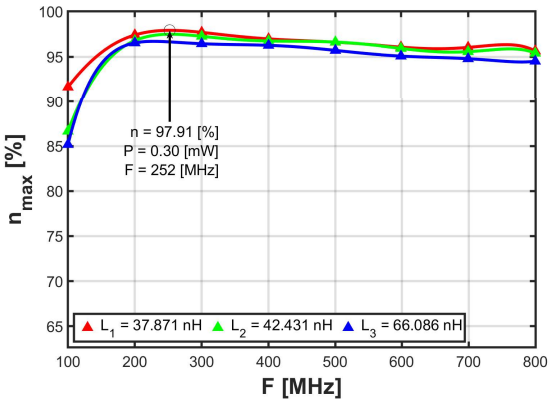
Evaluation of monolithic DC-DC step-up power converter with integrated inductor was performed in



(a) Q = 3



(b) Q = 9



(c) Q = 15

Fig. 6. Maximum efficiency for different L and Q

a standard 130 nm CMOS technology using Cadence design environment. Points of the best performance with focus on the converter efficiency were found and compared. As shown in the paper, a significant improvement in the efficiency can be obtained by enhancing the value of quality factor of the integrated inductor. Inductance value is then of lower importance in achieving better results. Lower inductance value means lower series resistance causing decrease in power dissipation in inductor. Evaluation results therefore recommend to design inductor with greater value of quality factor while maintaining reasonable inductance of the integrated inductor. In other words, the goal is to design an inductor with series resistance as low as possible. Comparison of maximum efficiency of real inductor in Fig. 4 to the ideal one with series resistance in Fig. 6(a) shows that significant loses are caused by other factors than series resistance. Finding other causes of power losses, together with finding means to create inductor with higher quality factor and lower series resistance, should be the subject of further research of power converters with the integrated switched inductor. Furthermore, all achieved results should be considered during implementation of converter directly on chip and confirmed by experimental measurements.

Tab. II. Significant results of simulations

Parameter	Unit	Inductor	L1	L2	L3
n_{max}	%	54.4	97.91	97.49	96.69
P @ n_{max}	mW	0.8	0.29	0.29	0.29
F @ n_{max}	MHz	164.4	252	254	228
Q @ n_{max}		2.98	15	15	15
P_{max}	mW	5.6	6.17	6.22	6.11
n @ P_{max}	%	13.2	55.51	69.41	71.07
F @ P_{max}	MHz	100	240	134	100
Q @ P_{max}		2.41	15	15	15

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