Experimental Verification of a Ultra-Low Voltage Charge Pump

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***Abstract*—This paper deals with the analysis of a cross coupled charge pump designed in a 130 nm CMOS technology with ultra low power supply voltage. We propose a printed circuit board, designed to experimentally verify this integrated circuit. The test board was designed to verify all function blocks of the charge pump independently, as well as the charge pump circuit as a whole. The charge pump was designed to operate at a supply voltage of 200 mV and the switching frequency of 100 kHz. The achieved experimental results prove the correct functionality of the designed charge pump integrated circuit.**

***Keywords*—charge pump; ultra low voltage design, experimental test board**

I. Introduction

Energy harvesting continues to be a challenging subject in electronics. In recent years, it is becoming increasingly interesting, as applications such as energy autonomous systems are becoming more and more popular. A large number of energy harvesting solutions have been published in recent research, focusing on converting various forms of energy into electrical power [1]. Thermoelectric generators, piezoelectric harvesters, wireless radio frequency (RF) harvesting and solar cells are among the most frequently utilized forms of energy harvesting devices [2]. Usually these are used in conjunction with a backup power source or energy storage device, such as a battery because the harvested energy has in most cases noncontinuous nature. The systems based on energy harvesting fundamentals must have power supervisor called power management unit (see Fig. 1). The main function of the power management unit is to properly utilize all available power sources, as well as provide a stable supply voltage for system. As the voltage provided by the various energy harvesters is commonly very limited, a step-up voltage converter is often required. A charge pump (CP) can be used for this purpose, mainly in applications with low power consumption. CPs have been traditionally adopted in application such as nonvolatile memories, SRAMs, RF antenna switch controllers and LCD drivers. Nowadays a CP is more and more commonly used for adapting voltage levels between two or more blocks in energy systems [4]. Their key advantages over more traditionally used inductor based switched mode voltage converters are low power dissipation, smaller form factor, and higher power efficiency. They needed a minimum number of external components to function and are therefore more suited for application in integrated circuits [5].

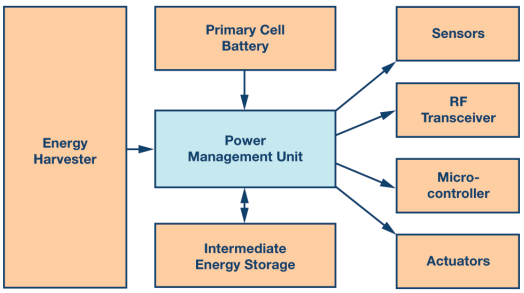

Fig. 1: Block schematic of a energy harvester system [3].

The path of integrated circuits from design to application is a difficult one and contains many important steps. One of them is testing. This is especially true during prototype development. The designer of an integrated circuit must keep the testability of the circuit in mind. This means the tester must have the ability to monitor signal in the important nodes of the circuit (observability) and the ability to insert an external signal into these nodes (controllability) [6].

The main focus of this paper is on the testing procedure of an integrated CP circuit. For this purpose dedicated hardware (HW) was developed, in the form of a printed circuit board (PCB). Details on the developed HW, the measurement of individual circuit blocks as well as the CP as a whole are provided in later sections of this paper.

The rest of the paper is organized as follows: Section 2 gives insight on the CP integrated circuit under test. Section 3 deals with the description of the developed PCB. Section 4 provides an overview of the achieved results. Section 5 gives a summary and concludes the paper.

II. Description of the Cross-Coupled Charge Pump Under Test

The block diagram of the whole charge pump system is depicted in Fig. 2. It contains seven distinct functional blocks:

- Frequency Divider
- Low Frequency Clock Booster
- High Frequency Clock Booster

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- Switched Capacitor Voltage Divider
- Charge Pump Driver
- Low Voltage Comparator
- Charge Pump Core

The frequency divider was designed for a maximum input frequency of 1 MHz. Its function is to divide the input external clock frequency by half and create two non-overlapping clock signals that are later used to control the switching of the CP core. The purpose of both of the clock booster blocks is to double the amplitude of their respective input clock signals. This is done to improve the efficiency of the switch transistors in the CP core. The voltage divider is based on the switched capacitor approach and it is driven by the high frequency clock booster. It provides a divided output voltage to the comparator.

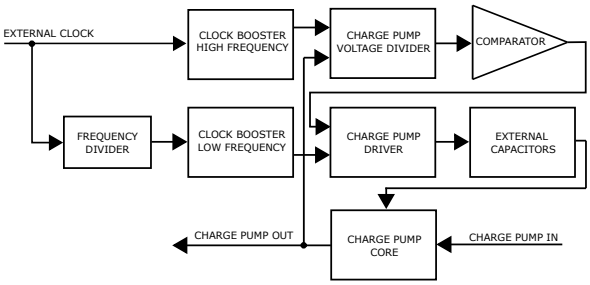

Fig. 2: Block diagram of the charge pump circuit under test.

The next block is a comparator. This component controls the switching of the CP core driver, depending on the output voltage. Its reference voltage and hysteresis levels can be externally adjusted to control the behavior of the CP as a whole. The charge pump driver generates the non-overlapping clock signals with sufficient driving capability to reliably charge a flying external capacitors. It is controlled by the digital output signal of the comparator. If the signal from the comparator is at logic zero, the driver is enabled and generates the signal used to drive the external capacitors. The main part of charge pump is the charge pump core consisting of three parallel branches, each with three stages arranged into cascade. All stages are build on cross coupled architecture.

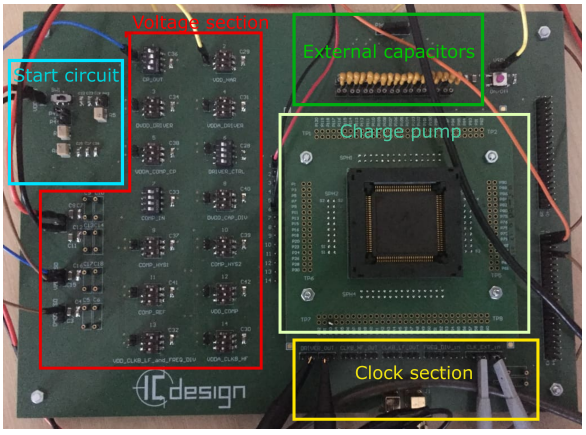

Fig. 3: Photograph of the developed test PCB.

III. Printed Circuit Board Used for Experimental Verification

A PCB was designed to experimentally verify the proposed cross-coupled CP circuit. It was designed to allow us to independently evaluate the individual circuit blocks of the CP, or verify the CP as a whole. To achieve easy reconfiguration of the test setup the test board was divided into different blocks:

- Voltage Section
- Clock Section
- Start Circuit with Load Resistor
- External Capacitors Section

The **Voltage Section** was created using DIP type switches. The DIP switches are used to allow the various input pins of the CP circuit to be connected to two different voltage supply domains (VDD1, VDD2), be grounded or let floating if needed.. This is depicted in Fig. 4. The output of the CP can also be connected to VDD1, VDD2, grounded, or connected to a load resistor. This gives us the ability to provide the supply voltage for the various circuit blocks of the CP from its output. This approach gives us a high degree of flexibility during testing of different circuit blocks of the CP.

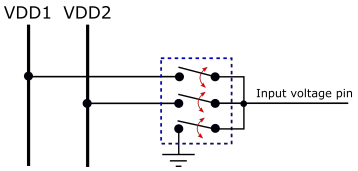

Fig. 4: Possible connections of the charge pump input pins.

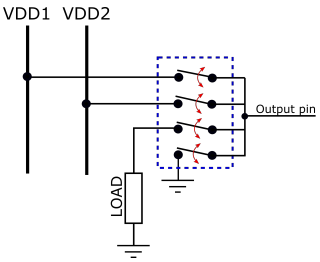

Fig. 5: Possible connections of the charge pump output pins.

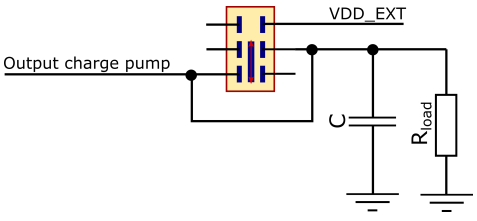

Fig. 6: Start circuit schematic diagram.

The **Clock Section** was designed in a similar fashion. We used pin headers with jumpers instead of DIP switches because pin headers have better

TABLE I: Charge pump integrated circuit pins according to their power supply connection

Power supply from CP output	Power supply from Input
VDDA COMP CP	VDD HAR
DVDD CAP DIV	DVDD DRIVER
VDD COMP	VDDA DRIVER
	COMP REF
	CLKB LF
	FREQ DIV
	CLKB HF

insulating properties in an open state for high frequency signals, due to lower parasitic capacitance. This results in lower cross-talk between the different part of the circuit. The middle pins in the pin headers are connected to CP input pins. The left pins in the pin headers are grounded. The right pins in the pin headers are intended for a signals from a waveform generator which is connected to the PCB via SMA coaxial connectors.

The **External Capacitors Section** is divided into nine sections of two capacitors each. Leaded capacitors are connected using female pin header connectors, to ease testing with different capacitor values. These capacitors are connected to the CP core, to each nine stages (total of 2×9 capacitors bank). They are driven by the external clock signal, or the internal CP driver block, according to the connection of the jumpers in the Clock section pin headers. All clock signal paths from the clock section to the CP clock input pins have identical lengths. This ensures that the signals from all external capacitors come to the CP core with the same amount of delay, ensuring proper timing of the non-overlapping clock signals.

When the charge pump was tested as a whole, some blocks of the CP had their power supply pins connected to the input of the CP (representing the harvester output voltage), and other blocks were powered from the CP output. These connections are summarized in Tab.I. Such easy handling of proper voltage domain was achieved by DIP switches in the voltage section, as shown in Fig. 4 and Fig. 5, where output of the CP was connect to VDD1 and input voltage to VDD2 respectively. Now we can connect the pins of the various CP blocks as necessary.

A proper start-up procedure has to be followed to ensure the functionality of the circuit blocks powered from the CP output. For this purpose the **Start Circuit Section** of the PCB is utilized, as shown in Fig. 6. This circuit consists of a variable load resistor, smoothing capacitors and slide switches. It enables us to precharge the output of the CP to its operating voltage from an external supply. After disconnection, energy stored in smoothing capacitor ensures powering of CP directly from its output during hot-start phase.

IV. Measurement Results

The functionality of the CP as a whole is shown in Fig. 7. We can see how all of the circuit blocks of the CP work. The reference voltage of the comparator was set to 200 mV and $2nd$ level hysteresis was used. While the output voltage of the CP is below 400 mV, the output of the comparator remains at logic zero, and the CP driver is enabled. This causes the CP to charge the output capacitor, thus the output voltage rises. When the output voltage rises above a certain threshold, the output of the comparator goes to logic high. This disables the CP driver, thus stoping the charging of the output. During this time the output of the comparator copies the output voltage, as this is its supply voltage. As soon as the output voltage falls sufficiently, the comparator output goes back to logic low, repeating the whole operational cycle. During this measurement the load resistor was set to 87 $k\Omega$ and the output capacity was 162.2 μF.

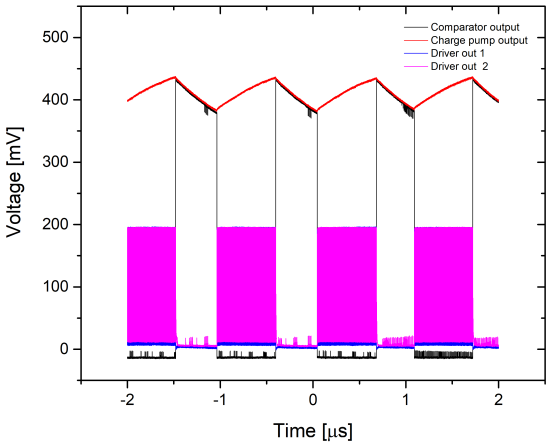

Fig. 7: Measured waveforms demonstrating the functionality of the CP as a whole.

The Fig. 8 shows the output signal from the frequency divider. The frequency divider has been independently tested with the input frequency of 100 KHz and power supply voltage of 200 mV. We can see that the output signal has half the frequency of the input.

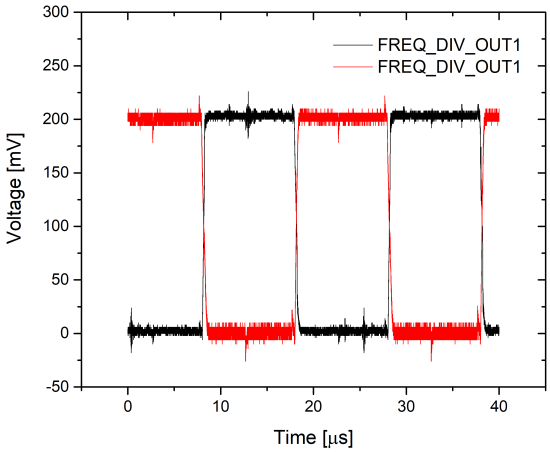

Fig. 8: Output signal from the frequency divider, with input signal frequency of 100 KHz.

Also the clock booster circuit has been tested as separated block with a power supply voltage of 200 mV. The input signal of the low frequency clock booster was the output of the frequency divider. The input signal to high frequency clock booster was the external clock signal from the generator. In both cases the input signal amplitude is 200 mV. In Fig. 9 and Fig. 10 we can see the output signals of both booster blocks have more than double the amplitude of their

input signals.

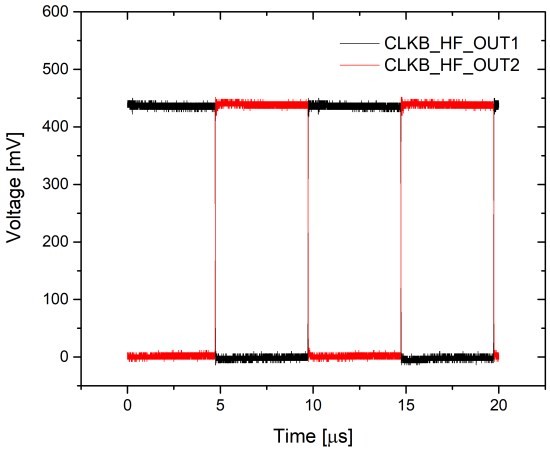

Fig. 9: Output signal from the high frequency clock booster.

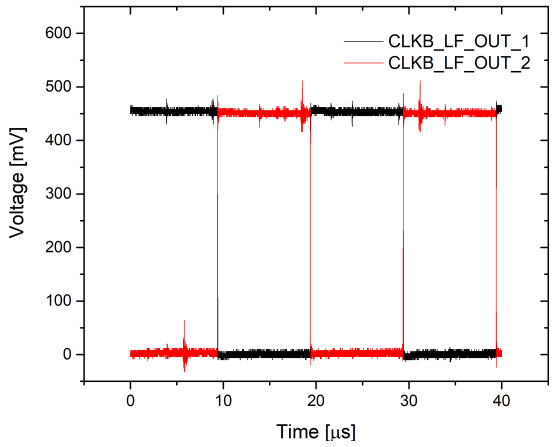

Fig. 10: Output signal from the low frequency clock booster.

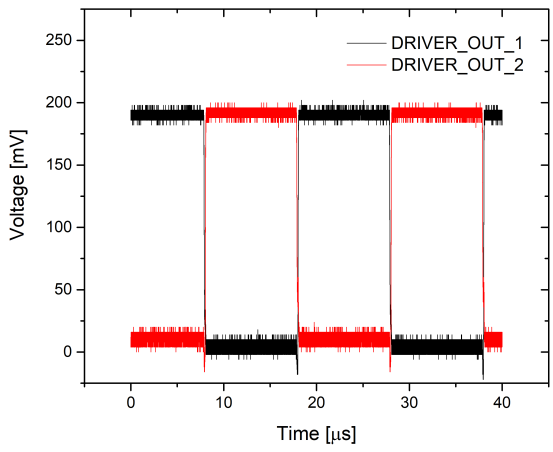

Fig. 11: Output signal from the CP driver.

Finally to demonstrate PCB versatility, the Fig. 11 shows the output signal of the CP driver itself. This signal was connected to the external capacitors. This signal has an amplitude of 200 mV and frequency of 50 kHz.

V. Conclusion

In this paper a measurement procedure for the verification of a integrated charge pump circuit was presented. We have experimentally verified the functionality of the proposed cross-coupled CP with designed test PCB. The tests were performed with an input voltage of 200 mV feeding CP. The frequency of the external clock signal was set to 100 kHz. All described blocks of the proposed CP were verified separately, and their correct function was confirm. After that the CP was tested as a whole, by connecting the circuit blocks as shown in Fig. 2. The achieved experimental results prove that the designed CP as well as the proposed test PCB work correctly. The output voltage of the CP fluctuated around 400 mV. The amount of fluctuation depends on the load resistor and the level of hysteresis set in the comparator.

VI. Acknowledgement

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