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Very High Resolution Time Measurement Systems

Doctoral Thesis

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Abstract

The thesis deals with systems dedicated to time measurement with very high resolution. The resolution is in the order of picoseconds. The necessary part of the systems is their synchronization which is described in the thesis. These kinds of systems with such resolution follow from current experiments in particle physics. The first part is focused on possible level signaling and transmission media in the time measurement systems. The second part introduces the time-to-digital converters which are used in time measurement systems, as well as measurements and tests with designed TDC with very high resolution. The third part describes the system with several nodes intended to timestamp application (time measurement). The system includes synchronization among the nodes and the synchronization principle is explained. The functionality is tested and measurement results are shown. Other usage of designed devices and the synchronization in experiments in particle physics is mentioned in the last part.

Keywords

Delay measurement, FPGA, Particle physics experiments, Propagation delay, Synchronization, TDC, THS788, Timestamps, Time measurement, Time to digital converter, Very high resolution

Declaration

Předkládám tímto k obhajobě dizertační práci zpracovanou na Fakultě elektrotechnické Západočeské univerzity v Plzni. Prohlašuji, že jsem tuto práci vypracoval samostatně, s použitím odborné literatury a pramenů uvedených v seznamu, který je součástí této dizertační práce. Dále prohlašuji, že veškerý software, použitý při řešení této dizertační práce, je legální.

I hereby submit this thesis for doctoral defense. I declare that all work has been done independently. All used literature and sources are cited and listed in this document. Only legal and licenced software has been used.

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List of Abbreviations

ADC - Analog-to-Digital Converter

ATLAS - A Toroidal LHC ApparatuS

CERN - the European Organization for Nuclear Research

DUT - Device Under Test

DWDM - Dense Wavelenght Divison Multiplexing

FIFO - First In, First Out

FPGA - Field Programmable Gate Array

FTDI - Future Technology Devices International

GPS - Global Positioning System

INL - Integral Non-Linearity

ITU - International Telecommunication Union

LAB - Logic Array Block

LE - Logic Element

LHC - Large Hadron Collider

LSB - Least Significant Bit

LUT - Look-Up Table

LVDS - Low-Voltage Differential Signaling

PC - Personal Computer

PCB - Printed Circuit Board

PLL - Phase Locked Loop

PSI - Paul Scherrer Institute

SEB - Single Event Burnout

SEE - Single Event Effect

SEL - Single Event Latch-up

SEU - Single Event Upset

SRS - Standford Research Systems

TDC - Time-to-Digital Converter

TOTEM - TOTal, Elastic and diffractive cross-section Measurement

TI - Texas Instruments

TMU - Time Measurement Unit

UART - Universal Asynchronous Receiver/Transmitter

USB - Univesal Serial Bus

VHDL - VHSIC Hardware Description Language

VHSIC - Very High Speed Integrated Circuit

Chapter 1

Introduction

Timing with very high resolution, i.e. tens of picoseconds, is desired in current experiments in physics. Specifically, research in particle physics. The experiments are conducted in facilities with accelerators. There are several accelerators, for example LHC[1]at CERN[2].

Due to the speed of particles moving close to the speed of light and the connected calculation, very precise timing measurements with very high resolution are needed. There is an effort to increase the resolution up to at least 10-30ps. For example, this resolution is necessary for detection of particles in the detectors approximately 200 meters far from the interaction point and their matching in TOTEM Experiment at CERN. The resolution corresponds to a distance of 1cm according to the particle speed.

The timing problems can be seen from two points of view. One is focused on the signal distribution with defined timing (jitter, delay). While the other deals with time converters. These converters are called time-to-digital converters (TDC). The time-to-digital converters (TDC) are devices used for conversion of time (continuous quantity) to a number (discrete quantity). The TDC is in principle a stopwatch. The time resolution is related to the resolution of the signals propagation (clock signal, reset signal, input signals). The main purpose of TDCs is to measure time between events.

On the market, there can be found several solutions for TDCs. But mostly they are only for specific applications and general purpose TDCs have limited resolution. Thus, the effort is to concentrate on high resolution TDCs for wider areaa of application. A solution from the market with designed readouts is mentioned.

The work is divided into 10 parts (including introduction and conclusions). The parts correspond with the explanation mentioned in the previous paragraph. The first main part, after the introduction and motivation part, deals with time measurement. The history of time, its measurements, common definitions and standards are described. The next part is focused on signal distribution, i.e. how signals propagate and how the time reference is set. After that, time-to-digital converters are explained in the chapter, which is divided into three subsections. Techniques and methods used in time to digital converters are shown in the overview of the first subsection. The interest is devoted to methods using digital blocks, because Field Programmable Gate Array (FPGA) is used for one type of designed TDC.

[1]LHC - Large Hadron Collider, the world's largest colliders, Geneva, Switzerland
[2]CERN - the European Organization for Nuclear Research, Geneva, Switzerland

The other types of designed TDC readouts are described, which are based on a special timing chip. The interest is devoted to TDCs based on a timing chip. The next subsection discusses the possibility of errors, which may or may not effect the measurement, i.e. the resolution of the measurement is not capable of recognizing errors. The measurements with designed TDC are described in the following subsections. The goal is a characterization of the time-to-digital converters, i.e. where are the limits of TDCs. The following part describes a clock distribution system and proceeds with signal distribution, which gives high resolution and accuracy. Resolution and accuracy are necessary for taking data from several TDCs in different places. The particular block diagram used for the distribution system is shown. The measurements are described with discussion of results. The last chapter is focused on other usage of designed TDCs and experiments with TDCs are shown. At the end, the conclusions are mentioned.

Chapter 2

Motivation

The motivation to develop the time distribution system is progress in particle physics. Especially diffraction physics as higher and higher energies need more precise time measurements. Physicists should be able to improve their findings when analyzing data with a higher resolution of measurements. The TDCs help the precision of time measurement.

2.1 High energy physics

Two beams with opposite direction of the particle's flow are in the accelerators for particle physics exploration. At the specific points, the beams are crossed (cross section). These points are called interaction points at which particles collide. The figure below shows the particle collision simulation.

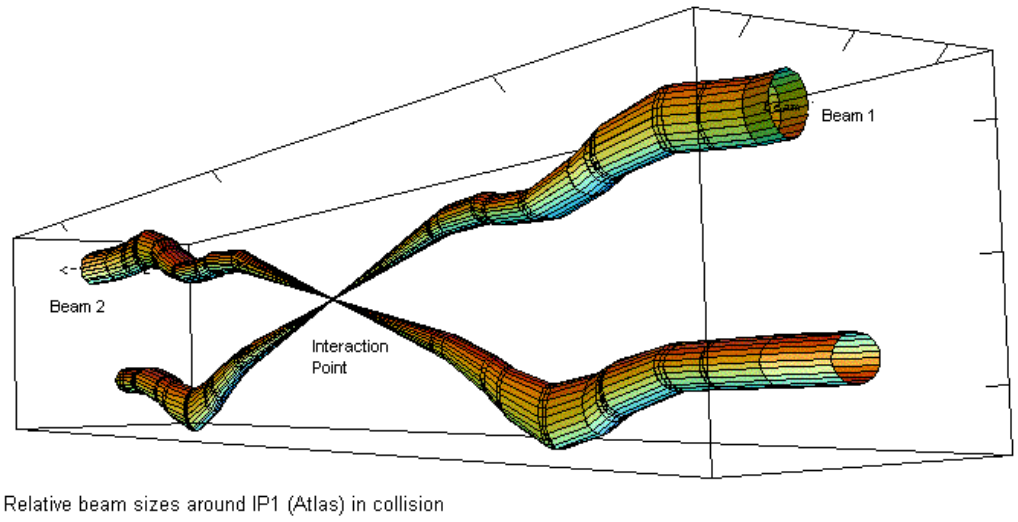


Figure 2.1: Beams in collision [22]

Specifically at CERN [21], the energy per proton has been 13TeV since 2015 (7TeV before). The total cross section is 110mbarns [22] meaning the probability of interaction between small particles. One barn is $10^{-28}m^2$(it is a cross section of a uranium nucleus).

The total cross section can be distinguished into:

- Inelastic
- Single diffractive
- Elastic

The collision produces different products according to the type of the collision mentioned above. They are detected with several detectors, which are around the interaction point. The time of flight of the particles is measured between the detectors for their defining. We can calculate the time resolution of the time distribution system to fulfill the needs of physicists. An example for the decay into mesons is shown below.

The decay is at a distance of 3.9cm. For the speed of light, it means 130ps from the collision to the decay. This result leads into the resolution of the TDC. The resolution should be ten times better for a reasonable measurement. In the same way, the resolution for decays into other particles can be calculated. The photo of the interaction point at CERN is shown in Fig. 2.2 [18]

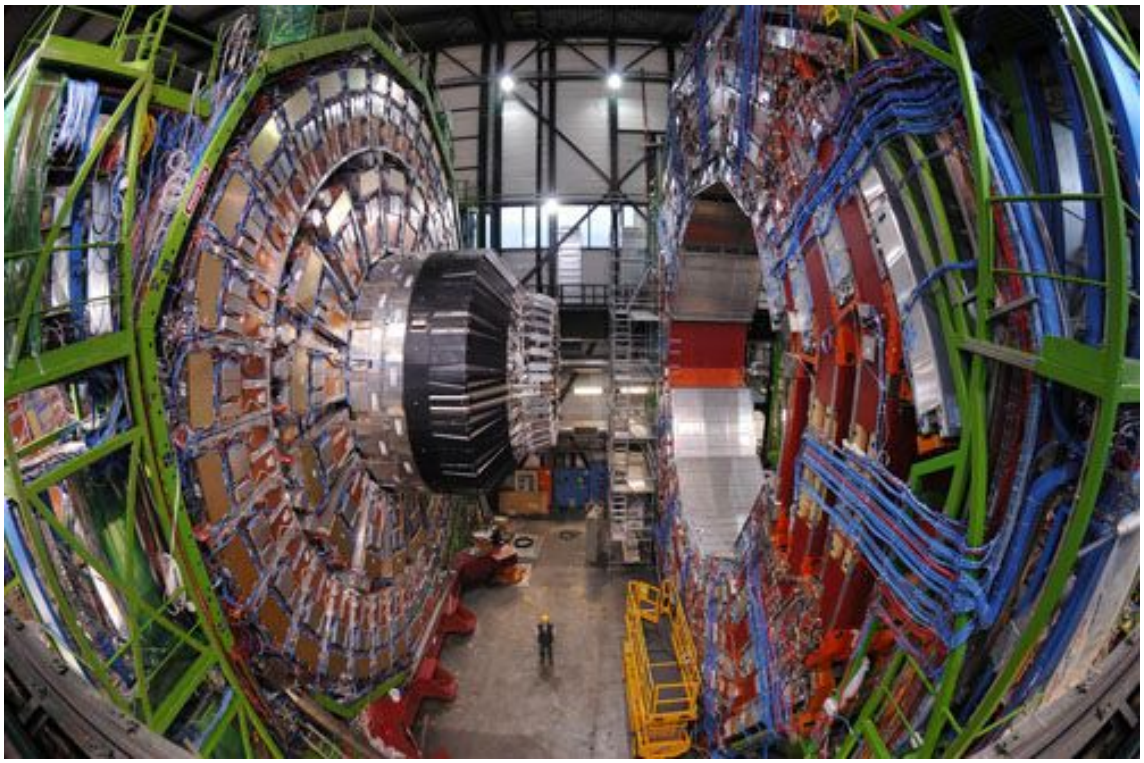


Figure 2.2: Interaction point with detectors at CERN

2.2 Behavior of TDC in harsh environments - SEE in TDC

Because the time distribution system should work in a radiation environment, the single event effect (SEE) should be taken into account. The time distribution system composed of TDC and FPGA should be evaluated from two point of view.

- Behaviour in radiation environment
- Detection of errors

The behaviour in radiation environment means single event effects in the components which can cause a malfunction of the time measurement.

Another factor is how to detect the single event effects in the component. It means using the TDC for detection of SEEs. The single event effect is caused by an energetic particle. There are several single event effects that can occur and change the behaviour of the system.

Main types of SEEs:

- Single event upset (SEU)
- Single event latch-up (SEL)
- Single event burnout (SEB)

A single event upset (SEU) is one type of SEE. The SEUs can be taken as soft errors because they are nondestructive. They cause a pulse which can flip a memory cell or a register. After that, the value is taken as a regular value by the rest of the hardware and it causes undesired behaviour. The system can be restored very easily by setting it to the defined state. The precaution for this type of error is a redundant structure of the system. The behaviour of the redundant system is based on a majority voter. Memory cells also include SRAM which is used as a configuration element for some FPGAs.

The single event latch-up is considered a hard error with a potentially destructive effect. It results in a high current and creates a path between power rails. The effect can be removed by powering down the device.

The single event burnout can occur in power MOSFETs. The high energy particle causes a current which activates the parasitic bipolar transistor. This leads to the destruction of the MOSFET.

There are other types of single event effects. Such as single event gate rupture (related to power MOSFETs as SEB).

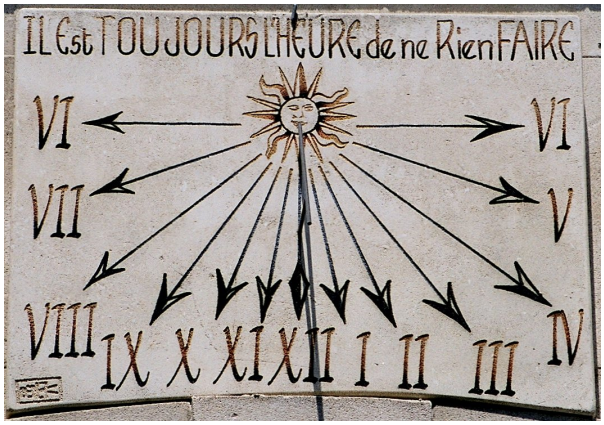
Chapter 3

Time measurement

Time is a continuous quantity. It belongs to the seven fundamental physical quantities. Time is represented by one second as a primary unit. Time is used for recording events when they happen (past, present, future). Throughout history, the way of recording time has developed from simple to very advanced methods, which are able to differentiate events up to very small fractions of a second, such as microseconds, nanoseconds, picoseconds. This progress is connected to science, especially particle physics, where it is very important to be able to differentiate events within nanoseconds and picoseconds.

3.1 History of time measurement

In history, the effort of time measurement was focused on dividing the day into smaller parts. One of the devices is a sundial (Fig. 3.1a [25]), which has been known for more than three thousand years. But the sundial is only able to measure time during the day, not at night. Also in the same era, the hourglass (Fig.3.1b [20]) was invented. It measures a small period of time during the day.



(a) Sundial

(b) Hourglass

Figure 3.1: Time measurement devices

In the early medieval age (11th century), mechanical clocks were invented. Mechanical clocks are still used, for example as a watch. And they went through significant development with more precise manufacturing technology.

The calendar is used in order to record longer time periods. There were many types of calendars in history with the purpose of dividing years into days.

3.2 Presen possibilities

Present possibilities came from the progress in electronics. Modern devices are based on semiconductor components, which allow increasing resolution and accuracy of time measurement, i.e. microseconds up to picoseconds. A clock generator is needed for time measurement. It is called an atomic clock, which is based on the electronic transition frequency of the electromagnetic spectrum of atoms. The atomic clock is based on an atomic standard, it means the isotope of a suitable element. The most common isotopes are caesium (^{133}Cs) or rubidium (^{87}Rb). These clocks are used for time distribution services.

3.3 Standards

The commonly used standars are:

- Caesium standard (approximately 9.192 GHz)
- Rubidium standard (approx. 6.834 GHz)

The standards differ in working frequency, accuracy and stability. The Caesium standard is an accurate standard used for the definition of a second in SI. The working frequency of the Caesium standard is 9 192 631 770 Hz. The Caesium standard is a primary frequency standard. The frequency accuracy of the standard is $\pm 10^{-13}$s and stability is $<10^{-14}$ (according to Microsemi frequency standards [23]). In frequency standard domain, the stability is reffered as Allan deviation. An example of the Caesium standard is shown in Fig. 3.2 [19].

Figure 3.2: Microsemi brand Caesium standard

Another commonly used standard is the Rubidium standard. The working frequency is 6 834 682 610.904 Hz. The accuracy is less within one or two orders than the accuracy of the Ceasium standard. It is about $\pm 10^{-11}$s and the stability $<10^{-12}$ or $<10^{-13}$ [23]. Thus the Rubidium standard is the secondary frequency standard. It is widely used in many applications, such as television broadcasting, base stations for cellular networks or global positioning systems (GPS). Additionaly on the market, there can be found other types of frequency standards or references. Here are a few examples:

- GPS Disciplined Oscillators (requires GPS antenna, Fig. 3.3 [24]
- Rubidium Oscillators
- Quartz Oscillators
- Hydrogen Maser

Figure 3.3: GPS Disciplined Oscillator

The parameters of selected standards or references are shown in the following table (Tab. 3.1).

Table 3.1: Selected frequency & time standards

Standard	*Accuracy*	*Stability*
Caesium	$\pm 10^{-13}$	$<10^{-14}$
Rubidium	$\pm 10^{-11}$	$<10^{-13}$
GPS Disciplined Oscillators	$\pm 10^{-12}$	$<10^{-11}$

Further, we recognize two different stability terms, short-term stability and long-term stability. Short-term stability refers to seconds, maximum hundreds of seconds, the long-term stability refers to days and more.

Chapter 4

Signal distribution and synchronization

If we want to measure time, it means obtaining information about an event (or events) at a specific moment and the information is obtained from a signal. Thus, getting the information is a signal distribution. The signal distribution can be realized in an electrical or optical way. The need for time measurement is primary in experiments in particle physics, in which there are many detectors. These detectors are in different places. In other words, the distance (path) for signals vary according to the position of the detector. The path can vary in distances or the transmission media used. The signals from a central unit (main control unit) propagate through the transmission media according to the used material. For example the velocity of propagation of coaxial cables is determined by the dielectric material, the velocity of propagation of optical cables is determined by the refractive index. The idea of the signal distribution is shown in Fig. (4.1)

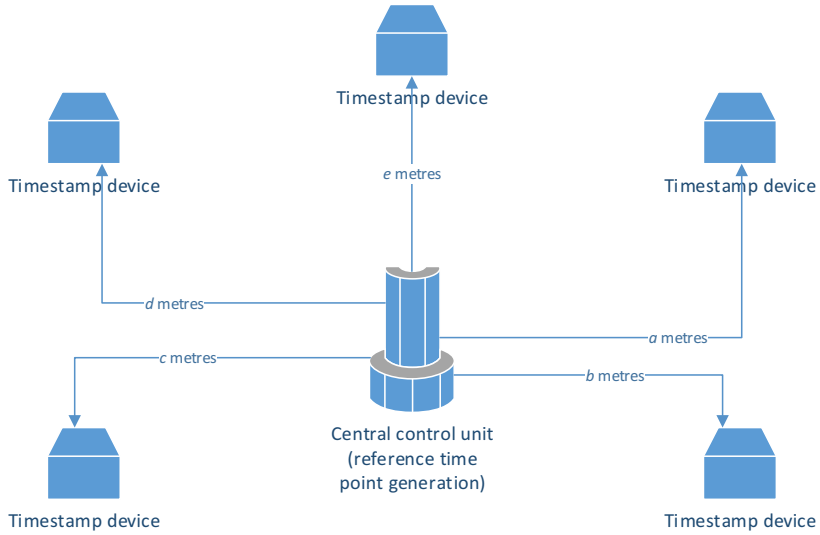


Figure 4.1: Signal distribution

In the system, the different transmission media can be used for a specific reason (long distance or availability, etc.) and cables have different lengths. In that case the propagation delay changes accordingly to the place, i.e. the information from the central unit arrives at a different time. That is why each place has to be synchronized with the central timing unit. In Fig. 4.1, there are a central unit (in the middle) and 5 timestamp devices, which generate timestamps for the corresponding detectors. Further, the different connection length is seen. The timestamp is related to the trigger (reference time point) that is provided by the central unit, but timestamps among the devices can not be combined together in this configuration, they are not synchronized.

The principle of the synchronization is a propagation delay measurement and it is shown in the time diagram in the following figure (Fig. 4.2).

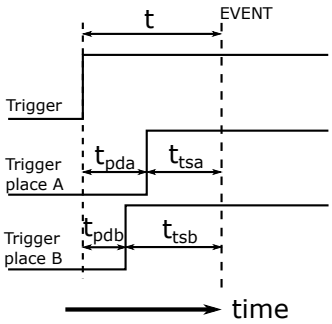


Figure 4.2: Synchronization principle

The trigger signal propagates in two places, the first place A in t_{pda} (propagation delay to place A) and the second place B in t_{pdb}. After that an event occurs and the timestamp device gives timestamp t_{tsa} or t_{tsb}. The synchronized timestamp is given by formula 4.1 for place A:

$$t = t_{pda} + t_{tsa} \tag{4.1}$$

For place B, it is given by formula 4.2:

$$t = t_{pdb} + t_{tsb} \tag{4.2}$$

There are three ways to synchronize timestamps:

- Cable characterization in advance
- Continuously measurement of the propagation delay
- Combination of both previous method

The cable characterization in advance requires making a measurement of each cable used for the installation of the whole system. After that, the measured propagation delay is stored in each device and the produced timestamps are synchronized immediately without

any other measurement. It is a big advantage of this approach. But the environment parameters in the system can vary, such as temperature. The propagation delay will be changed and the error will grow according to the intensity of the change of the environment conditions.

The second method removes the disadvantage of the first method because the propagation delay is measured continuously and the measurement is made under the present condition. But the method requires three conditions. The first condition is the most important. The propagation delay measurement unit has to be included in the central unit. The second condition is a return path for the trigger signal to the timestamp devices for the propagation delay measurement. And the third condition is a splitter in the timestamp device for a trigger signal (if it is used for the propagation delay measurement).

According to the assumption that the forward path and the return path are the same, the propagation delay is twice as long and it has to be divided by a factor of two. Then the timestamps are synchronized online in readout software. In principle, it can be synchronized in hardware too, but it requires an extra communication data channel between the central unit and the timestamp device. Therefore the current propagation delay is computed in the central unit and it is sent to the timestamp device where it is immediately used for timestamp correction.

The third way is a combination of the previous methods. The cables are measured separately. After the installation, a table with cables and their directions (to the timestamp device or from the timestamp device) is established. According to the table, the ratio of forward and return paths are computed. Then the method goes on with the continuous measurement of the propagation delay. The measured propagation delay has to be divided by the ratio computed before. In the previous method, the assumption was the same paths and the propagation delay divided by a factor of two. Thus the last method removes the problem with the necessity of the same cables (length, type). Also another advantage is implied from that, the parameters of the cables vary according to the environment but the computed ratio of the forward and the return paths are the same. Then the propagation delay is computed for the actual condition.

The propagation delay of each path is measured by the central unit and the synchronization is done by one of the previous methods. As already mentioned, the cables can be different. There are two options in principle:

- Electrical cables (coaxial cable, twisted pair cable)
- Optical cables

4.1 Electrical transmission media

As electrical transmission media, coaxial cables or twisted pair cables are usually used for longer distances. The choice depends on the signaling used. There are two types of signaling:

- Single-ended signaling

- Differential signaling

4.1.1 Single-ended signaling

Single-ended signaling is used in many applications. The signal is transferred through the voltage level via a conductor. The signal is related to the common reference, which is usually a ground with zero potential. The coaxial cable is used as transmission media, the inner conductor in the coaxial cable transfers the signal, the shielding is used for the common reference. The principle of single-ended signaling is shown in Fig. 4.3.

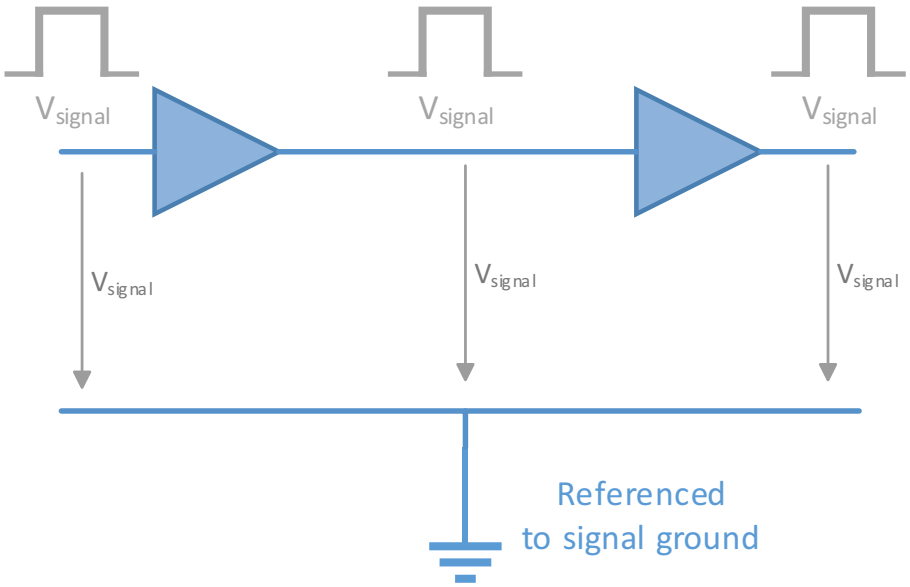


Figure 4.3: Single-ended signaling

The signaling levels depend on transferring an analogue or a digital signal. The analogue signal is chosen with respect of other components. The digital signal is limited by common standards. For example, the common standards are TTL, CMOS, LVTTL, LVCMOS. The following table (Tab. 4.1) shows output voltage levels of the common standards for the digital transfer.

Table 4.1: Common standards - voltage levels

Standard	V_{OL} *(maximal)*	V_{OL} *(typical)*	V_{OH} *(minimal)*	V_{OH} *(typical)*
TTL	0.4 V	0 V	2.4 V	5 V
CMOS	0.5 V	0 V	4.5 V	5 V
LVTTL	0.4 V	0 V	2.4 V	3.3 V
LVCMOS	0.33 V	0 V	3 V	3.3 V

In single-ended signaling, the transmission media has a characteristic impedance and the transfer line should be terminated properly. The characteristic impedance for the coaxial cable in measurement is 50 Ω. The proper termination guarantees the limitation of the signal reflection.

The disadvantage is the influence of interference which is crucial with analogue value. The interference during digital transfer can be limited with higher voltage level, i.e. CMOS instead of LVCMOS.

4.1.2 Differential signaling

Differential signaling is based on the transmission of two complementary signals, which are usually called p-signals (as a positive signal) and n-signals (as a negative signal). There are two important voltage levels in differential signaling: common-mode voltage (V_{CM}), differential-mode voltage (V_{DM}).

The common-mode voltage level is the average value of a p-signal and n-signal with respect to the ground. The differential-mode voltage is the difference between the p-signal and the n-signal, thus it is a useful signal. The principal is shown in Fig. 4.4. The usage of differential signaling these days is in very high speed serial lines. Several types of transmission mediae are used, such as ribbon cables, unshielded twisted pair cables (UTP), shielded twisted pair cables (STP), SCSI cables, etc.

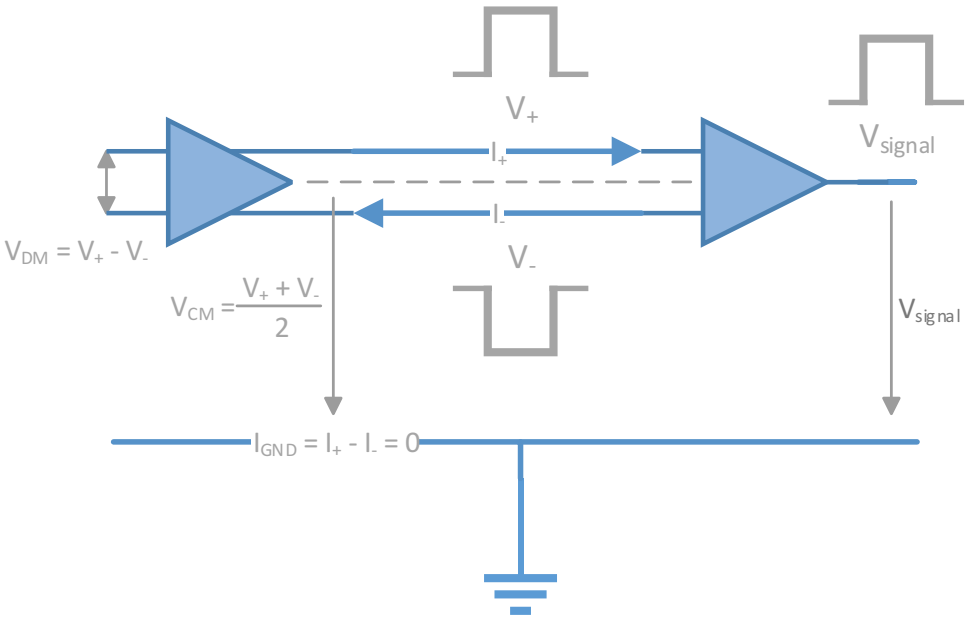


Figure 4.4: Differential signaling

Differential signaling is commonly used for digital transfers. There are many standards, such as PECL, ECL, LVDS, SLVS, CML, etc. The main differences are the levels of the common-mode voltage and differential-mode voltage.

Like single-ended signaling, differential signaling requires proper termination. The termination is usually 100Ω equivalent resistance between the p-signal and the n-signal. The chosen way of termination, i.e. resistor values and their connections, depends on the coupling used (DC coupling or AC coupling). The big advantage of differential signaling is a resistance to interference and also there is no need of the ground connection with AC coupling.

4.2 Optical transmission media

As already mentioned in the introduction of this section, the cables used for signal distribution can be optical cables instead of electrical cables. The optical transmission media has become very popular recently. They are often used for primary connection in wide area networks (WAN) or metropolitan area networks (MAN). They can be divided into two categories:

- Single-mode fibers
- Multi-mode fibers

Single-mode fibers are used for long distances and the core of the fiber has a very small diameter (9 μm). The multi-mode fiber is used for shorter distance and it is used for more wavelengths, which is ensured by the variable refractive index of the fiber. In that case the light is bent smoothly according to the refractive index. The core diameter is 50 μm or 62.5 μm. The advantage of optical media is a bigger resistance to the disturbances from the environment (for example temperature) than electrical media. But the disadvantage is the necessity of several very expensive parts, such as lasers, optical-to-electro converters, etc.

The basic structure of the optical connection with a respect to time measurement is shown in the following figure (Fig. 4.5)

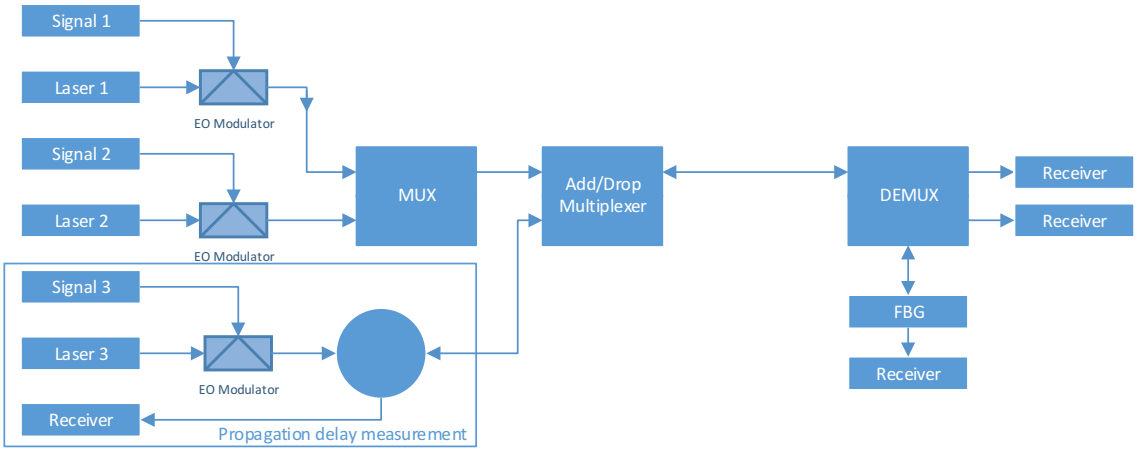


Figure 4.5: Structure of optical interconnection

The basic principle of the system is transmitting the delay measurement (synchronization) signal to the timestamp device. The other signals (clock, reset, etc.) are also transmitted to the timestamp devices. The electrical signals are transformed to the optical signal using electro-optical modulators. Then signals are combined with the Dense Wavelength Divison Multiplexing (DWDM) multiplexer (MUX in the figure). The signal, which is used for the delay measurement of the whole transmission line, is added into the DWDM multiplex using the add/drop multiplexer (OADM). In the place with the timestamp device, there is a demultiplexer (DEMUX) to separate each signal by wavelength. The delay measurement signal has to be propagated back to the central control unit in

the same fiber, which requires a reflection of the wavelength used for this signal. A special component for the reflection is used before the demultiplexing and it is called fiber bragg grating (FBG). The system requires the following parts:

- Electro-optical modulator
- DWDM Multiplexer and demultiplexer
- OADM Multiplexer
- FBG

Their principles are explained in the following subsections.

4.2.1 Electro-optical modulator

An electro-optical modulator is an analog intensity (optical amplitude) modulator. The modulation is caused by changing the refractive index of the material using a modulating voltage. $LiNbO_3$ is the material, which the modulator is made from.

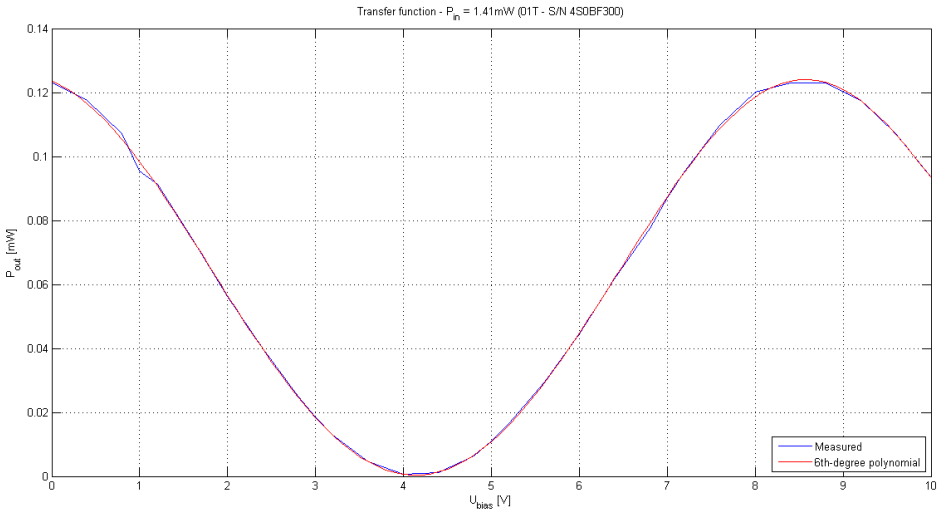


Figure 4.6: Transfer function of the electro-optical modulator

The modulating voltage consists of a bias voltage (U_{bias}) and an RF voltage. The bias voltage determines the working point of the modulator. The modulator works as an amplitude modulator and its transfer function is a sine wave. It is shown in Fig. 4.6 (Output optical power - P_{out} vs. bias voltage - U_{bias}). Three working points are possible, MIN, MAX and quadrature, depending on the position at the transfer function. The MIN and MAX working points are used for the digital communication. The quadrature working point is used for analog applications and it is located in the middle of the linear region of the transfer function. But a problem with the working point is its stability. The transfer function moves in the horizontal axis. It is caused by the material which the modulator is made from. That is why the bias voltage has to be controlled to keep the same position of the working point.

Control is feasible in two ways. The first way is superimposing a 1kHz tone signal to the modulating signal. It allows a photodiode in the modulator (created during the manufacturing). The photodiode is used for feedback measurement of the effect of the superimposing tone signal. The tone signal causes additional 2nd and 3rd harmonic distortion in the signal. The best setting is the lowest harmonic distortion caused by a 1kHz tone signal. Another way to control the bias voltage is by comparing the input optical power with the output optical power. The advantage of this method is that there is no additional signal in the modulating signal. It means no additional jitter. A disadvantage is adding optocouplers in front of and behind the modulator. The following figure (Fig. 4.7) shows inputs and outputs of the modulator.

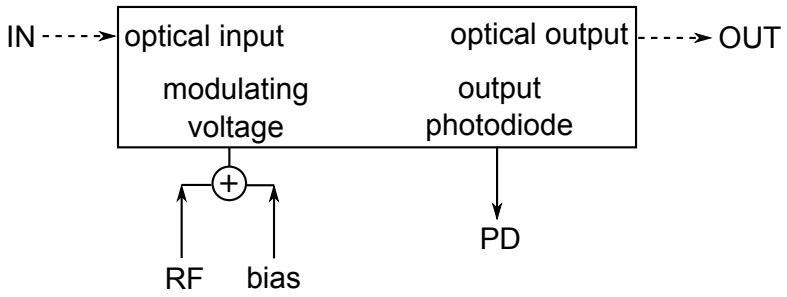


Figure 4.7: Inputs and outputs of EO modulator

4.2.2 DWDM Multiplexer and demultiplexer

There are 4 channels in the multiplexer and demultiplexer for DWDM multiplex. Inputs are labeled with a specific number of the channel (according to ITU) on the multiplexer and vice versa on the demultiplexer.

4.2.3 OADM Multiplexer

The add/drop multiplexer has two inputs. The first input is for one way communication. The second input is named add/drop. The function is that the signal can be transmitted in both ways through this port. This feature is used for the delay measurement in the system.

4.2.4 FBG

The FBG is a component which behaves as a reflector for a signal with a specific wavelength. The structure of the FBG is set for the specific wavelength that is reflected by the manufacturer. The other wavelengths pass through the fiber bragg grating without influence.

Chapter 5

Time-to-digital converters

The time to digital converter is a stopwatch in principle. The task is to measure time between events or start-stop and after the measurement, the TDC gives the digital value which represents the time between the start and stop events.. There can be many formats of the number but the most common is a standard binary value where the LSB corresponds to one time unit. In that case, the LSB determines the resolution of the TDC.

Probably the simplest TDC is a counter where the clock signal sets the resolution and stability. This type of TDC is made only from digital blocks. The counter is shown in Fig. 5.1. Converters can also be made from analogue blocks instead of digital blocks, but the final stage in converters is the implementation of an analog-to-digital converter or a coder. The TDCs differ in the way the LSB is created. This is possible to do by analogue components or digital components. The method used depends on the desired resolution. A resolution around 100ps corresponds to the frequency above 10GHz. That is the reason why a more sophisticated method has to be chosen than a simple counter.

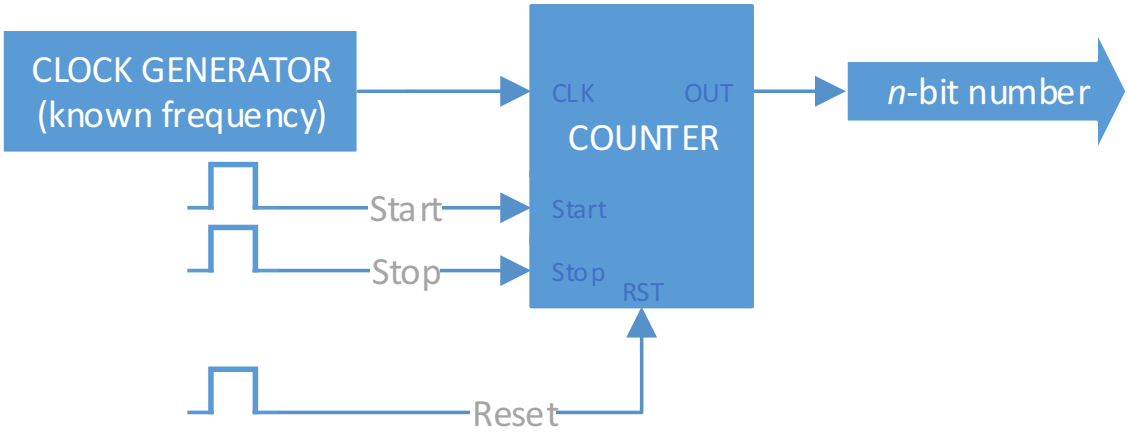


Figure 5.1: Simple TDC with a counter

The more sophisticated method lies in the design of a chain of delay elements. The delay element can be estabilished from D-flip-flops for high frequencies. Using capacitors instead of D-flip-flops is a better way. They allow higher resolution and they have another advantage. The delay can be adjusted by the voltage, which can be controlled.

5.1 Overview

Most TDCs divide the functionality into two blocks. One block is dedicated to increasing the dynamic range of the whole measurement, e.g. seconds or hundreds of seconds. The second block provides the high resolution, e.g. tens of picoseconds.

The coarse counter is suitable for increasing the dynamic range. The counter runs on a very stable frequency. This frequency can be obtained from a stable clock generator or a Phase-Locked-Loop (PLL) which is connected to the stable clock generator. A GPS standard is able to be used as the clock generator. The GPS standard produces a 10MHz signal with 1ps stability, meaning a period of 100ns. The resolution of 100ns is small even as the resolution of the coarse counter. The smaller resolution of the coarse counter, the higher requirements of the fine measurement circuitry. It can complicate the design of the fine measurement circuitry. Nowdays, counters are capable of running on frequencies higher than 100MHz, i.e. 10ns resolution at least. The FPGA makes such counters possible. The counter in FPGA is synchronous, that means every flip-flop reacts simultaneously. An asynchronous implementation of the counter is not convenient because the whole system in FPGA is designed as synchronous. Furthermore the addition of a synchronization stage complicates the design. The width of the counter corresponds to the dynamic range. The dynamic range is doubled with an increasing bit width of one.

The fine measurement circuitry can be designed in several ways. Commonly used methods are:

- Tapped delay line
- Vernier method
- Time-to-amplitude converter (requires analog-to-digital converter at the output in order to establish TDC, often called ramp TDC)
- Ring oscillator

5.1.1 Tapped delay line

The main principle is based on the chain of delay elements. The delay element determines the resolution. It is shown in Fig. 5.2.

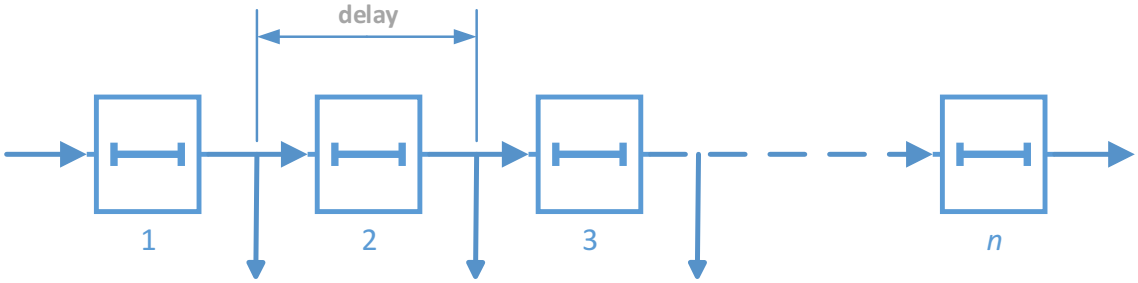


Figure 5.2: Structure of tapped delay line

The delay element can be established as a repeater, that is the simple way. The propagation delay of the repeater depends on the technology. It can be adjusted during the designing phase and is usually fixed, there is a possibility to control the propagation delay by voltage. In that case, the delay element is based on a capacitor (varicap). In digital systems, the delay element is the D-flip-flop or the wire (form of connection in the device) can be used as the delay element.

Taps in the delay line (Fig. 5.2) determine the resolution. In the simplest case, the output is in a thermometric code, that is why the coder is needed in order to obtain the number in the binary code. It is a simple logic circuit.

5.1.2 Vernier method

The Vernier method [15] is based on generating two signals with the frequency of $f_1$and f_2. The periods ($T_1$and T_2) of these signals are related to each other with either formula 5.1 or 5.2. Parameter m is the number of fractions of period T_1.

$$T_2 = T_1 \cdot \frac{m-1}{m} \tag{5.1}$$

$$T_2 = T_1 \cdot \frac{m+1}{m} \tag{5.2}$$

The method uses coincidences of the generators and the time intervals between the start or stop signal and coincidences of the generators is measured with counters. The block diagram of the one possible solution of the Vernier method is shown in Fig. 5.3.

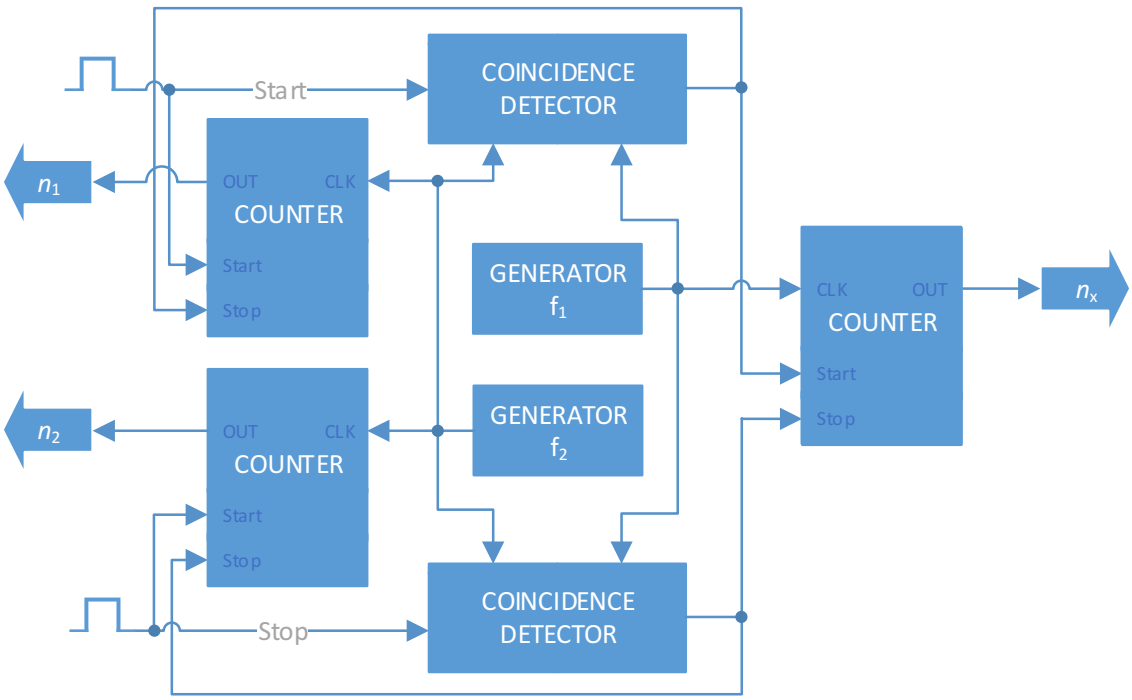


Figure 5.3: Block diagram of Vernier method

The measured time interval (t_x) is given by formula 5.3 and formula 5.4.

$$n_1 \cdot T_2 + n_x \cdot T_1 = t_x + n_2 \cdot T_2 \tag{5.3}$$

$$t_x = (n_1 - n_2) \cdot T_2 + n_x \cdot T_1 \tag{5.4}$$

5.1.3 Ramp TDC

The ramp method can be composed of 2 conversions. The first part is the time-to-analog conversion and the second part is the analog-to-digital conversion. The block diagram can be seen in Fig. 5.4.

The main part of the time-to-analog conversion is an integrator, which integrates the constant current. The integration process is executed with start signal and it is ended with stop signal. After the integration process, the value stored in the integrator is converted with the analog-to-digital converter. The result corresponds to the measured time interval. The current for the integrator, the range and the step of the analog-to-digital converter determine the resolution of the ramp TDC.

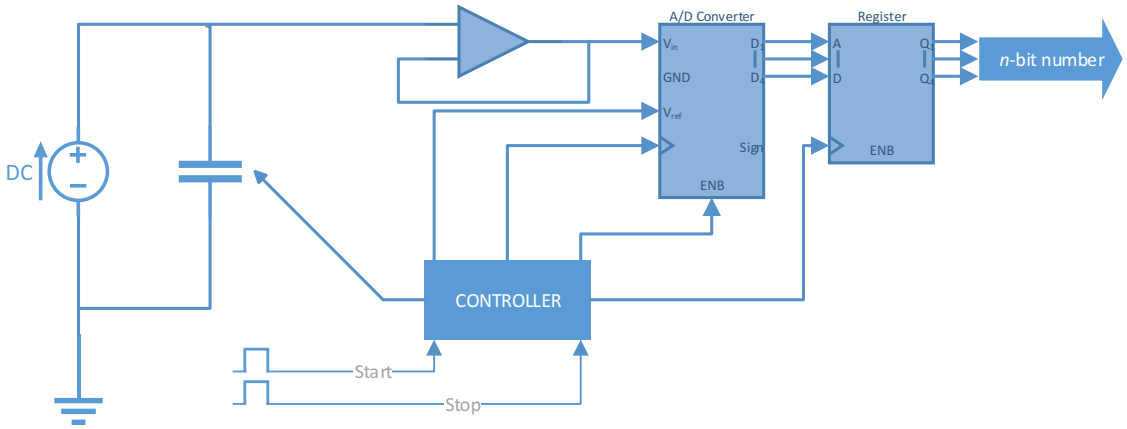


Figure 5.4: Block diagram of Ramp TDC

5.1.4 Timing chips

Timing integrated circuits with unusual architecture can be found as a product of research institutes, that are concerned with precise timing. For example, one of them is the DRS chip from PSI[1]. This chip is for a wave reconstruction and it can be used as TDC with control circuitry, such as FPGA.

Another possibilty of finding timing chips is on the market. A few chips dedicated for TDC are commercially available on the market. It is only a basic component without any controlling. That is why it is not simple to use these chips and there are no suitable evaluation boards on the market. Table 5.1 shows chips on the market.

[1] PSI - Paul Scherrer Institute, Switzerland

Table 5.1: TDCs available on the market

Manufacturer	*Symbol*	*Resolution*	*Measurement range*
TI	TDC7200	55 ps	8 ms
TI	THS788	13 ps	7 s
AMS	TDC-GP22	22 ps	4 ms
AMS	TDC-GPX	10 ps	10 µs
AMS	TDC-GPX2	10 ps	16 s
MAXIM	MAX35101	20 ps	8 ms

An example from the market is THS788 [6] from TI[2], the resolution of this chip is 13ps according to the datasheet. This chip can be used for comparison with other methods, such as FPGA based TDC.

5.1.5 Other methods

The other methods can also be done in an offline analysis. One example is a correlation. Suppose, there are original and delayed signals. If the correlation function is computed, the maximum can be found. The correlation is computed according to formula 5.5. The shift of the correlation to its maximum corresponds to the delay. The resolution of this method is a sampling period of the taken samples. So it is in the order of nanoseconds. There are some ways to increase the resolution, for example a non-even distribution of samples with a specific shape of the measured signal.

$$(f * g)(n) = \sum_{m=-\infty}^{\infty} f(m) \cdot g(m+n) \tag{5.5}$$

The correlation method is able to be performed online via hardware. The computing requirements for the hardware are high because of multiplications.

Several interesting methods can be found in the papers, such as using a quadrature clock [13], subnanosecond TDC using FPGA I/O resources [11], etc.

[2]TI - Texas Instruments Incorporated

5.2 TDC based on FPGA

Several ways exist to implement TDC in FPGA [12]. The TDC performs 2 measurements, the coarse and the fine measurement. Modern FPGAs including low-cost families can run on a frequency of almost 500MHz, high-end families (Stratix 10) can run on 1GHz. The frequency is used for the coarse measurement which is based on the counter. It can be seen in Fig. 5.5.

Another type of measurement is a fine measurement. It determines the resolution of the time measurement, i.e. least significant bit. The delay of one element determines the resolution.

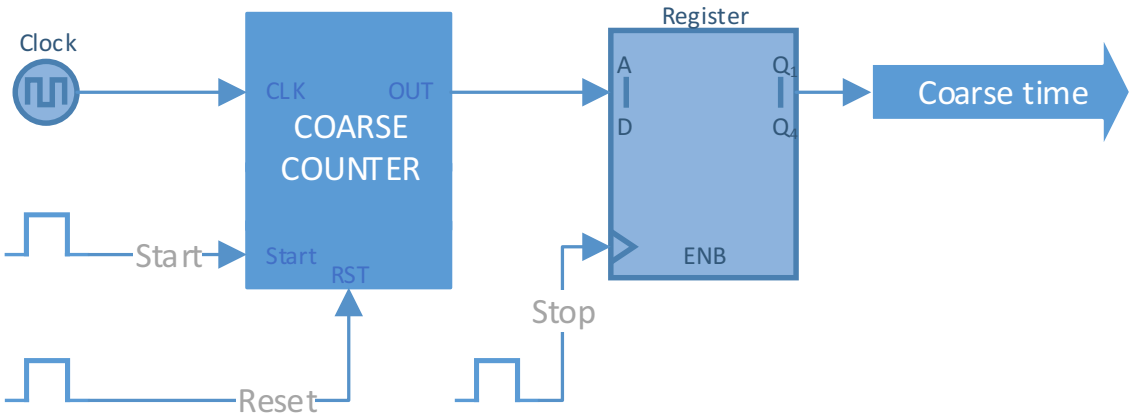


Figure 5.5: Coarse measurement

The delay element can be designed in different ways. In the first step, the delay can be obtained using a phase-locked loop. An option of a phase shift output is used. For example, the development kit DE0-nano [8] with Cyclone IV device family [3] has PLL with phase shifting by 45°. That means a delay of approximately 265ps, when the period of the output clock of PLL is 2120ps (maximum output frequency of 470MHz). The block diagram of a PLL based delay line is shown in Fig. 5.6.

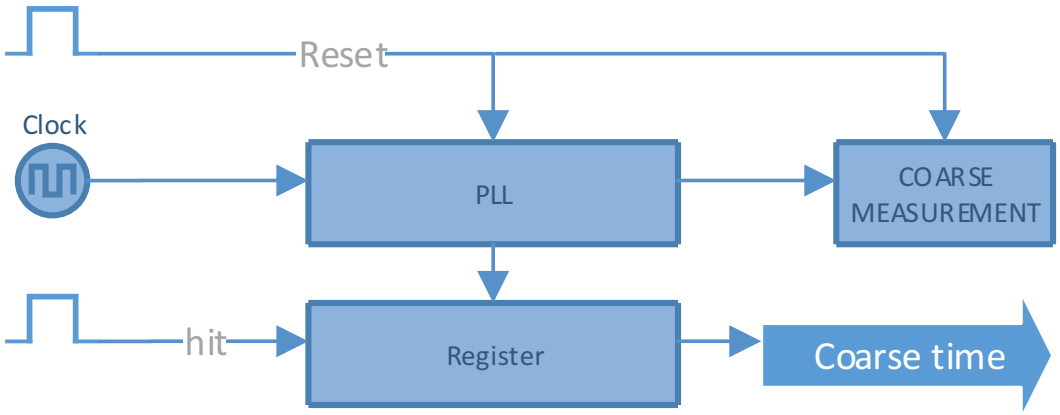


Figure 5.6: Fine measurement with PLL

A possibility of delay from 3ps to 100ps is in FPGAs from Xilinx using the clock

management. But it cannot be used, because of the limited number of these delay elements in FPGA. It would be about 200-800 elements for 600ps-2400ps total delay. Only 4 or 6 clock management units are in most FPGAs. The resolution of 265 ps (obtained by phase shifting) is not high enough, ten times higher resolution is needed. That is the reason for using the fastest connection in FPGA, where taps can be placed. The fastest connection is carry between logic elements (look-up tables). They are basic elements of the structure of FPGA. For Cyclone IV the delay of one carry is 58ps according to the simulation (it will be mentioned in Subchapter 5.2.2).

5.2.1 Carry chain

Logic Array Blocks (LAB) are basic building elements in FPGAs. They consist of Logic Elements (LE). The logic elements contain look-up tables (LUT), D flip-flops, multiplexers and interconnections. The structure is shown in Fig. 5.7.

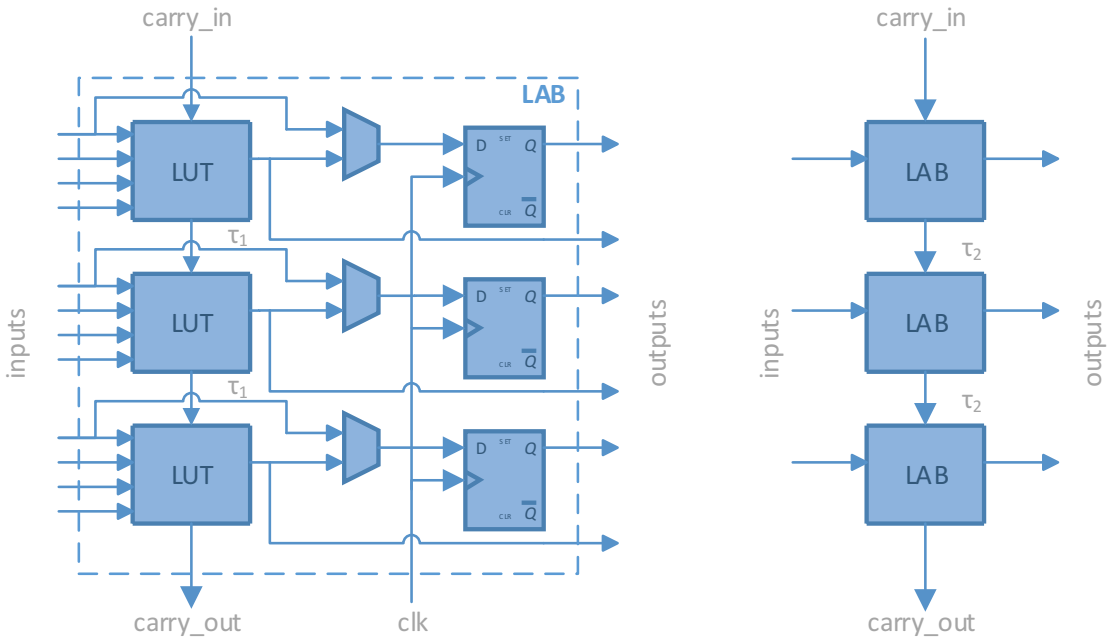


Figure 5.7: Simple structure of logic blocks in FPGA

The carry connection is between the look-up tables or logic array blocks. The carry connection brings another problem with the delay line. The path between the logic array blocks is not the same as the path between look-up tables (τ_1 and τ_2 in Fig. 5.7). The delay from the output of the LUT to D flip-flop is not important from a delay line point of view, because it is the same in each logic element. The carry connection exists in the adder. The adder is used for the carry chain structure of n elements. The N-bit adder equals a carry chain of n-elements. It is better to write the n-bit adder in VHDL [16] instead of using generated component from a library due to the adjustability of the adder component. Then, the output of the adder is used as taps from the delay line. The output of the LUT is connected to the D flip-flop which represents one bit of a register. It can be seen in Fig. 5.8.

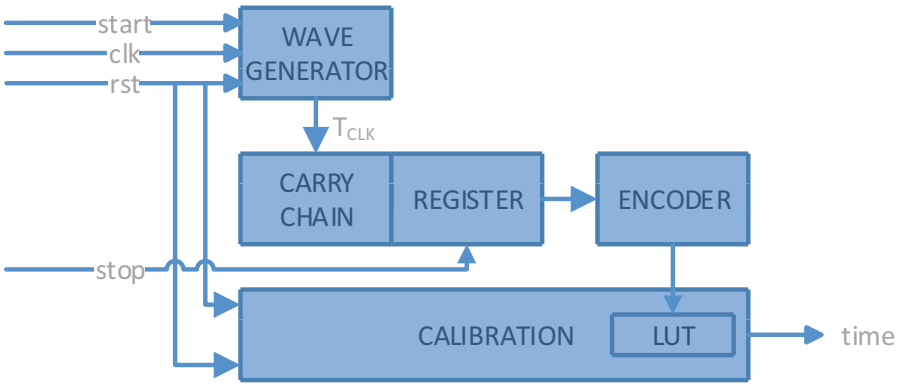


Figure 5.8: Fine measurement with carry chain

The delay is longer between LABs than between LUTs. That is why a wave generator is necessary. The wave generator transmits a signal with one transition or several transitions from 0 to 1 and vice versa via carry chain [14]. The signal is transmitted periodically. One transition corresponds to a thermometric code on the output of the carry chain. A simple combinatorial logic detects a position of the transition. It is shown in Fig. 5.9. Then an encoder is applied from the one-hot code to the binary code. That is a lower part (lower bits) of the final number, the higher part (higher bits) is obtained by the coarse counter. The number of delay elements should be to the power of 2 due to the complexity of the encoder.

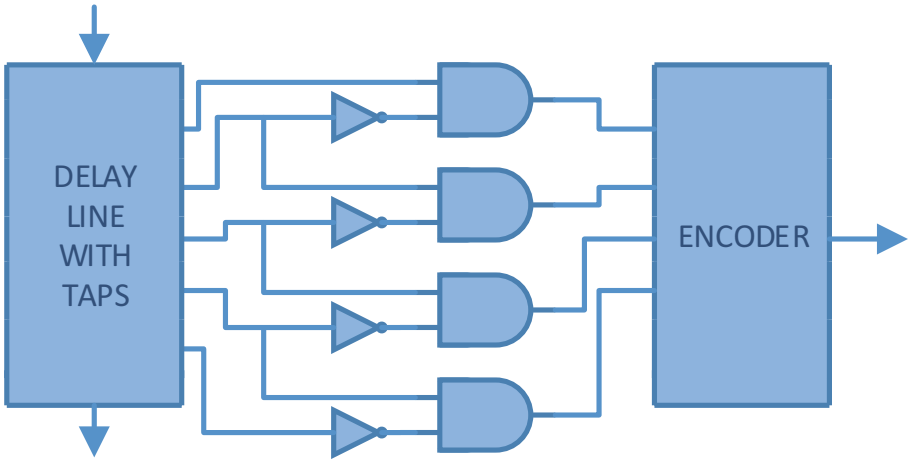


Figure 5.9: Detection of transition

The important blocks in Fig. 5.8 were mentioned except for a calibration unit. The goal of the calibration unit is to establish a look-up-table with time values. It is due to different delays especially between LUTs and LABs (τ_1 and τ_2). The calibration consists of 3 phases. The unit contains a histogram and calculation algorithm. The initialization of a RAM for the histogram is the first phase. Making a histogram from random hits is the second phase. The computation of time values and saving them into LUT is the last phase. The time values (t_i) depend on the count of all hits, on the count of hits for each element ($hits_\mathrm{i}$) and on clock period of the wave (T_CLK). The period of the wave corresponds to the length of the carry chain. The time values are computed with the following formula:

$$t_{\mathrm{i}} = \frac{T_{\mathrm{CLK}} \cdot hits_{\mathrm{j}}}{\sum\limits_{\mathrm{j}} hits_{\mathrm{j}}} + \sum_{\mathrm{k}=0}^{\mathrm{i}-1} t_{\mathrm{k}} \tag{5.6}$$

If the count of the hits per each element is the same, the increment will be the same.

Several transitions are needed for obtaining better resolution because of the possibility of longer delay between logic array blocks. In that case, the encoder has to be much more sophisticated. It has to be divided into 2 parts, one part for 0-1 transitions and another part for 1-0 transitions. More transitions in the wave ensure more accurate localization of longer delays in the carry chain. It is caused by averaging the position. When the wave propagates via longer delay, the gap with zeros or ones between positions of the transitions is lengthened. Here is an example for an 8-bit carry chain: the carry chain output changes from 110011110 to 11000111. It is shown in Fig. 5.10.

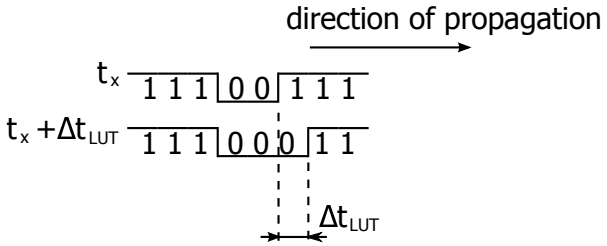


Figure 5.10: Example of wave propagatio for 8-bit of carry chain

The following two figure shows a logic element in FPGA for a better illustration of the carry structure implementation. Fig. 5.11 shows the logic element of the Cyclone IV device family, Fig. 5.12 shows the Cyclone V device family [2].

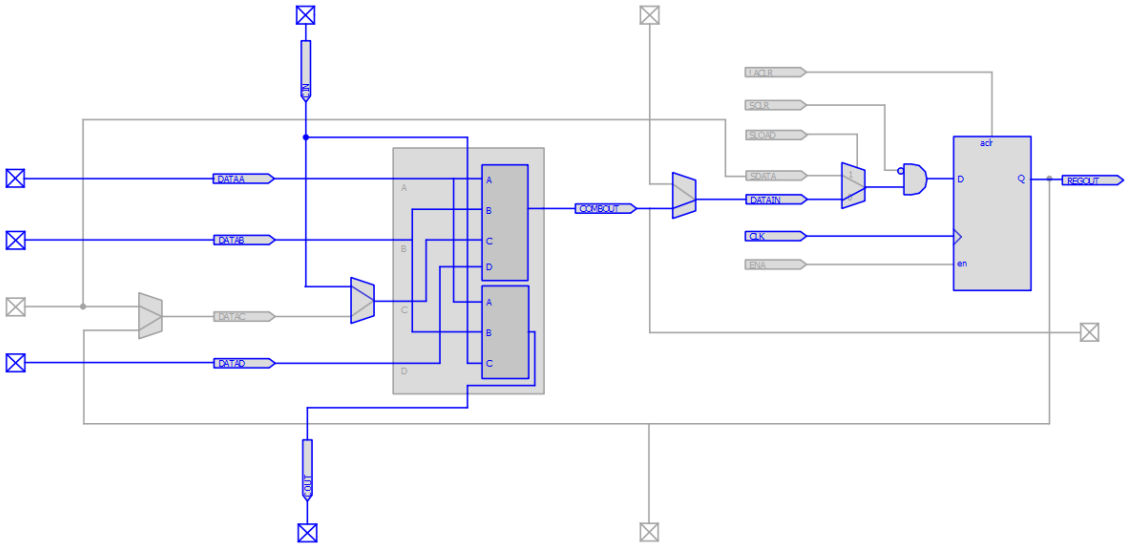


Figure 5.11: Logic element in Cyclone IV device family

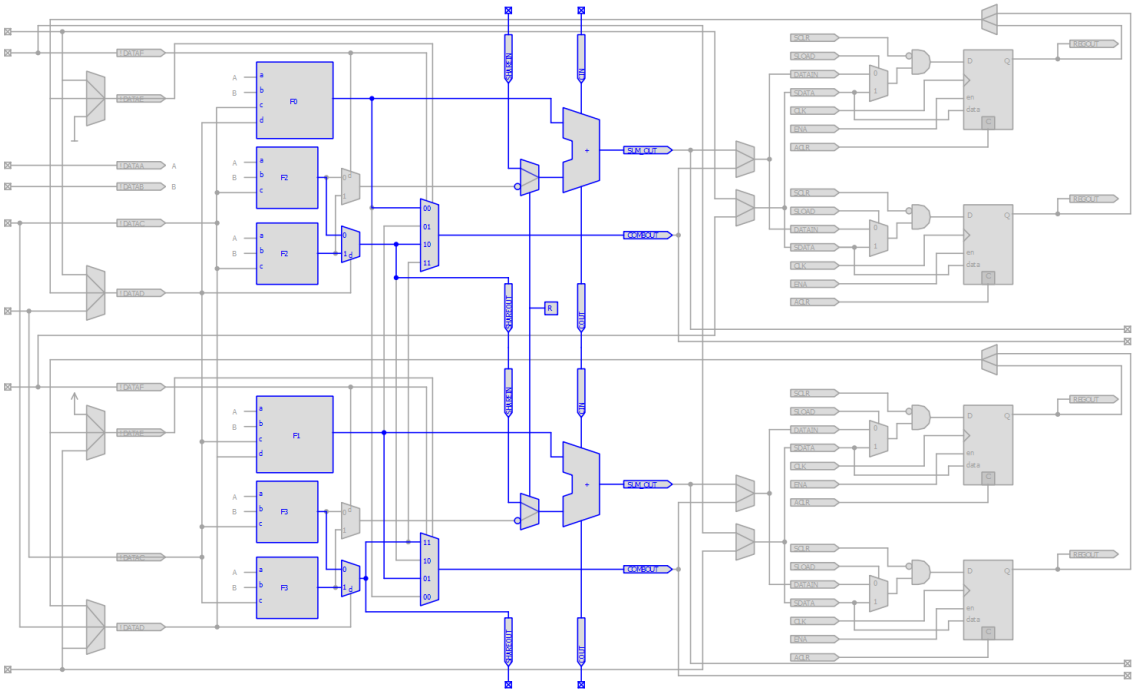


Figure 5.12: Logic element in Cyclone V device family

The structure is quite different. The adder is already presented in the Cyclone V device family and the carry exists between adders. The input of the adder is not used, because one input has to be in the logic value 0 and another input has to be in the logic value 1. Then, the signal propagates via the carry chain. The synthesizer and its optimizations removes the adder and they substitute it by gates and constant values. The solution controls the input signals of the adder with a dedicated signal which switches the values on adder inputs. It means one combination during reset and another one during the running. It can be seen simply in following VHDL code.

```
process(sw)
begin
    if (sw = '0') then
        a <= (others => '0');
        b <= (others => '1');
    else
        a <= (others => '0');
        b <= (others => '0');
    end if;
end process;
```

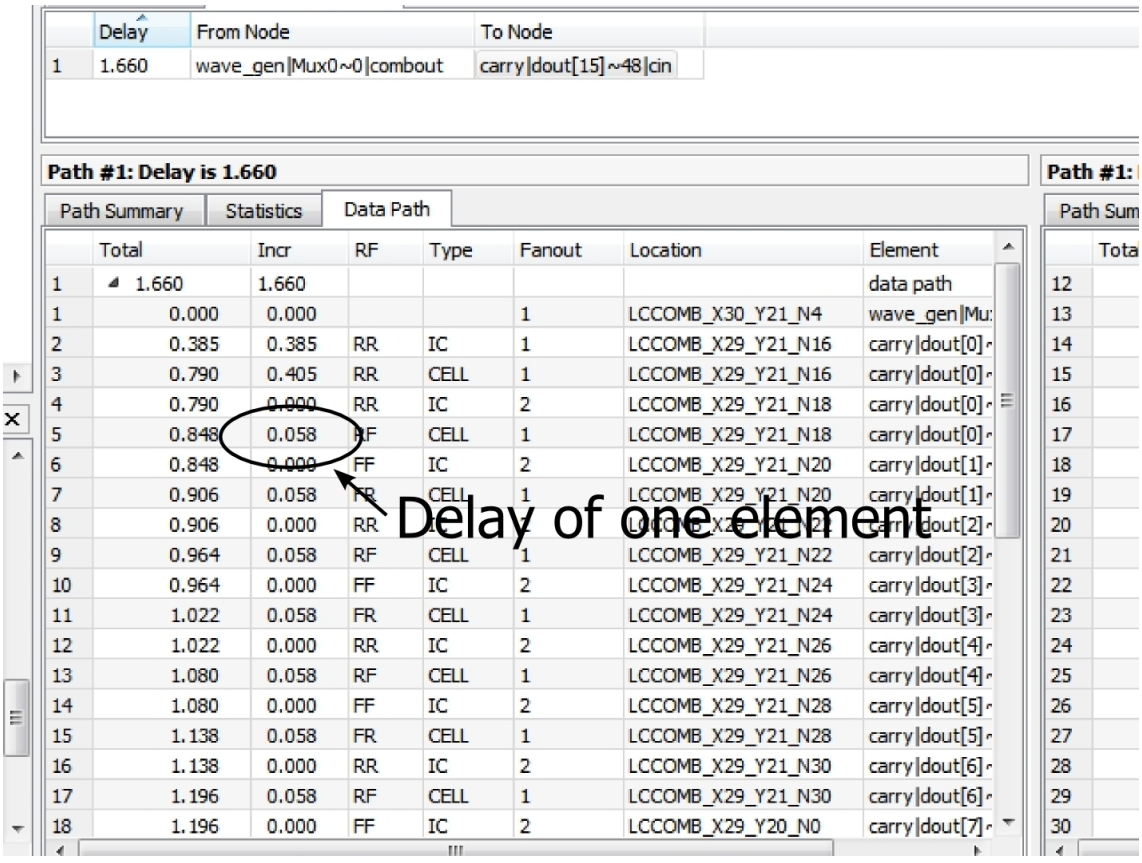
It results in that synthesizer putting the adder in the right way instead of gates and constant values. The usage of FPGA resources for a 5-bit calibration unit, i.e. 32bit long carry chain, is in Table 5.2.

Table 5.2: The usage of FPGA for 5-bit calibration unit

Logic utilizations (ALMs)	*275*
Total registers	195
Total memory bits	1280
Total PLLs	1/4

5.2.2 Simulations

The simulations were done for 2 Cyclone device families. The first device family is a DE0-nano development kit, which is populated with Cyclone IV. The second device family is the Cyclone V GX Starter kit [7], which is populated with 5CGXFC5C6F27C7 FPGA. You can see the TimeQuest Timing Analyzer output from Quartus II software for Cyclone IV (DE0-nano development kit) in Fig. 5.13. The TimeQuest Timing Analyzer is used for the timing analysis of the delay between elements of the carry chain structure. The delay is 58ps for Cyclone IV E.



	Delay	From Node	To Node
1	1.660	wave_gen|Mux0~0|combout	carry|dout[15]~48|cin

Path #1: Delay is 1.660

Path Summary | Statistics | Data Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	1.660	1.660					data path
1	0.000	0.000			1	LCCOMB_X30_Y21_N4	wave_gen|Mu:
2	0.385	0.385	RR	IC	1	LCCOMB_X29_Y21_N16	carry|dout[0]~
3	0.790	0.405	RR	CELL	1	LCCOMB_X29_Y21_N16	carry|dout[0]~
4	0.790	0.000	RR	IC	2	LCCOMB_X29_Y21_N18	carry|dout[0]~
5	0.848	0.058	RF	CELL	1	LCCOMB_X29_Y21_N18	carry|dout[0]~
6	0.848	0.000	FF	IC	2	LCCOMB_X29_Y21_N20	carry|dout[1]~
7	0.906	0.058	FR	CELL	1	LCCOMB_X29_Y21_N20	carry|dout[1]~
8	0.906	0.000	RR	IC	2	LCCOMB_X29_Y21_N22	carry|dout[2]~
9	0.964	0.058	RF	CELL	1	LCCOMB_X29_Y21_N22	carry|dout[2]~
10	0.964	0.000	FF	IC	2	LCCOMB_X29_Y21_N24	carry|dout[3]~
11	1.022	0.058	FR	CELL	1	LCCOMB_X29_Y21_N24	carry|dout[3]~
12	1.022	0.000	RR	IC	2	LCCOMB_X29_Y21_N26	carry|dout[4]~
13	1.080	0.058	RF	CELL	1	LCCOMB_X29_Y21_N26	carry|dout[4]~
14	1.080	0.000	FF	IC	2	LCCOMB_X29_Y21_N28	carry|dout[5]~
15	1.138	0.058	FR	CELL	1	LCCOMB_X29_Y21_N28	carry|dout[5]~
16	1.138	0.000	RR	IC	2	LCCOMB_X29_Y21_N30	carry|dout[6]~
17	1.196	0.058	RF	CELL	1	LCCOMB_X29_Y21_N30	carry|dout[6]~
18	1.196	0.000	FF	IC	2	LCCOMB_X29_Y20_N0	carry|dout[7]~

Figure 5.13: Cyclone IV - TimeQuest Analyzer

The functionality of the carry chain with 16 elements can be seen in Fig. 5.14. This simulation is done in ModelSim from Mentor Graphics using an sdo (standard delay format output) file generated by Quartus.

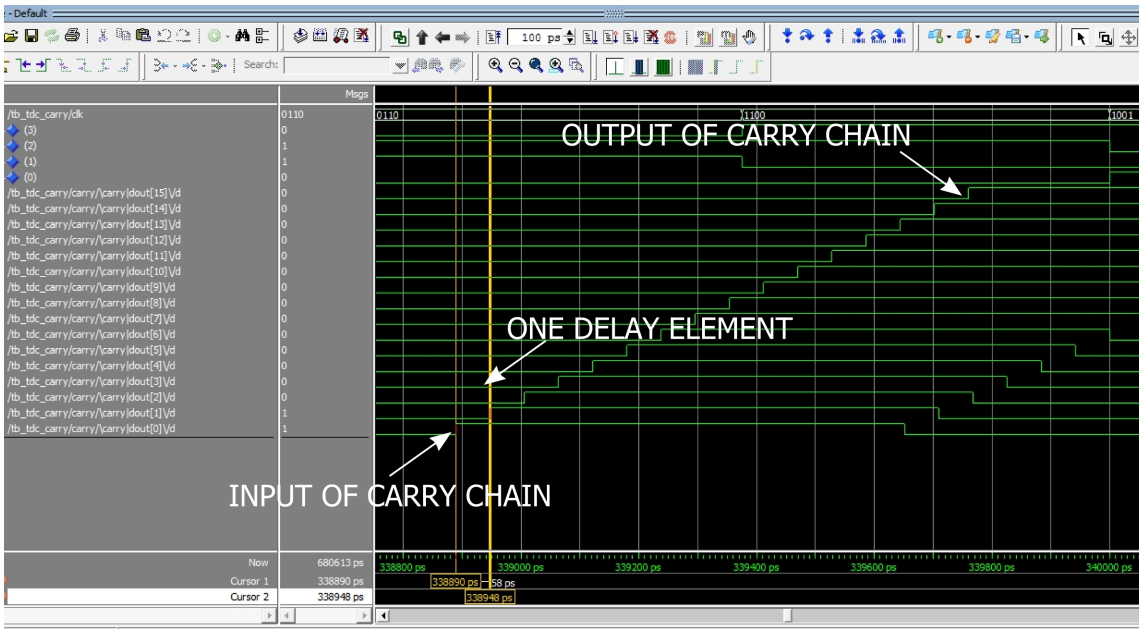


Figure 5.14: Cyclone IV - Simulation of carry chain

The problem with different paths was mentioned in the previous part (Subsection 5.2.1, second paragraph). A wave with several transitions is shown in Fig. 5.15.

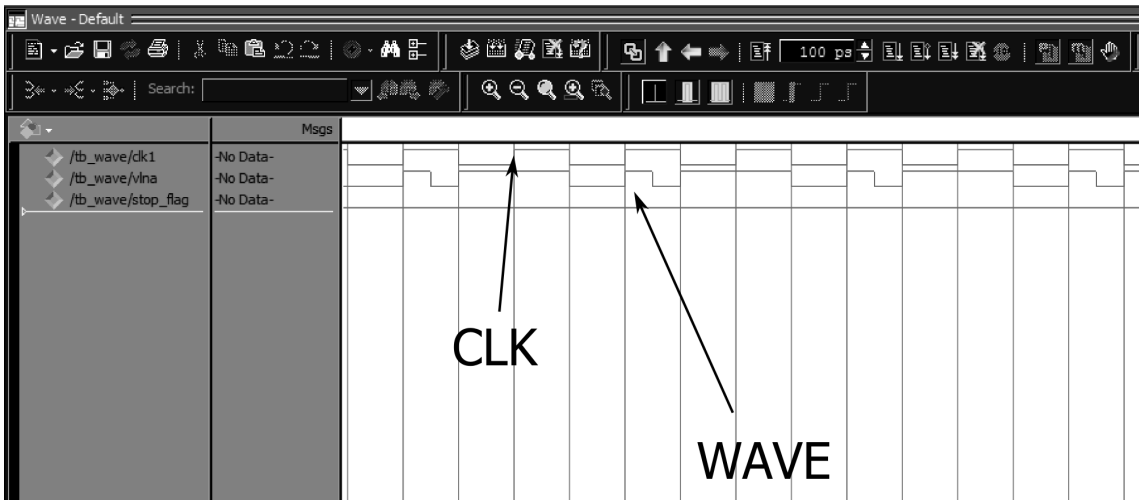


Figure 5.15: One possible shape of the wave

A problem with simulations is generating sdo files for Cyclone V, the comparison with TimeQuest Timing Analyzer results for the Cyclone V family is not possible because there is no sdo data for this family from the manufacturer. It is good to divide the simulations into 2 parts for the first look. The part without the carry chain structure and the simulation of the carry chain structure using sdo files. Without the sdo files, the simulation of the carry chain structure is useless. The heart of the whole system is the calibration unit, where the look-up-table with computed time values is established according to the calibration. The calibration process is divided into 3 phases as mentioned in the previous part.

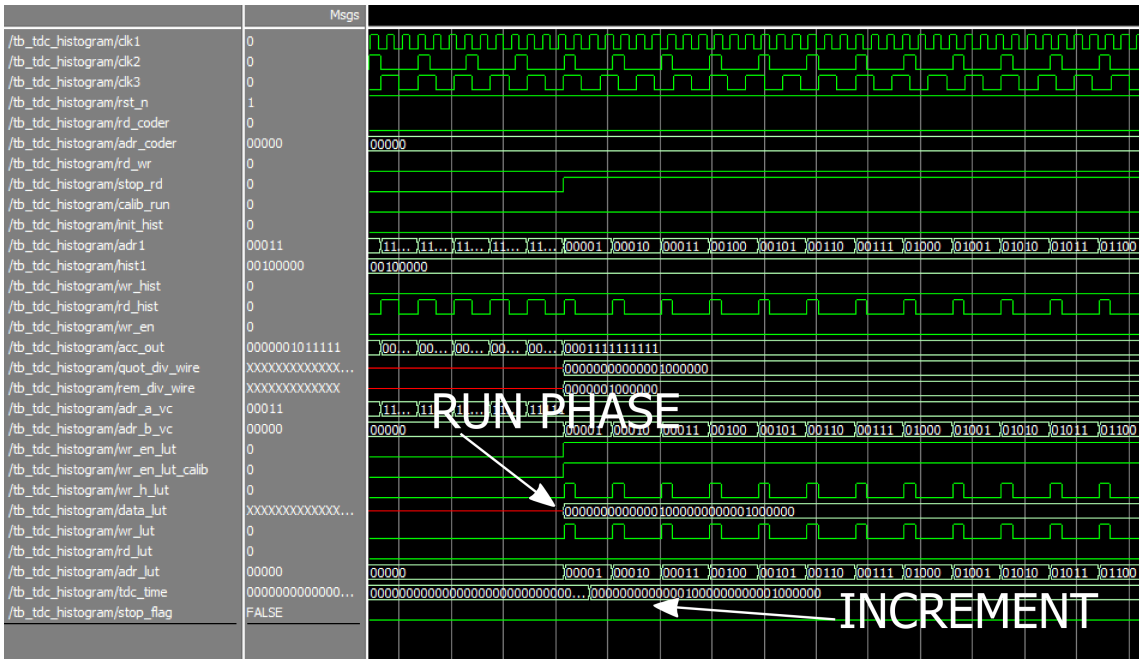


Figure 5.16: Simulation of calibration unit

Fig. 5.16 shows the end of the last phase. It is a reading of a look-up-table where time values (increment) obtained by calibration are stored. Time values are calculated according to formula 5.6. The hits are evenly distributed. Thus, the read increment of the delay is the same for each address.

FPGAs are primarily meant for synchronous systems. This assumption and the necessity of the calibration (seen in previous figures) make the implementation in FPGAs very difficult. Thus the effort should be focused on TDCs based on special timing chips which are dedicated to the time measurement.

5.3 TDC with the THS788 - USB2.0

THS788 is a chip from TI, which can be found on the market since March 2010. No evaluation boards or application notes are available. THS788 is a high speed time measurement device with high resolution. It measures time between signal on sync input and event input. Basic parameters of the chip are shown in Table 5.3. Event inputs and result outputs are LVDS compatible. A host serial interface ensures all programming of THS788 and the interface uses an LVCMOS standard.

Table 5.3: Parameters of THS788

Parameters	*Value*
Supply voltage	3.3V
Number of channels	4
Resolution (LSB)	13ps
Range	Up to 7s
Event input rate	Up to 200MHz

The evaluation board was designed for test purposes and measurements. The block diagram is shown in Fig. 5.17. The main part is the THS788 chip, which has LVDS compatible event inputs. That is why LVDS drivers are used as translators from a single-ended 50Ω signal. An FPGA is used as a controller. The development kit with FPGA is used due to the first implementation and understanding of THS788 behaviour. Communication with a PC is provided with an FTDI chip as the UART.

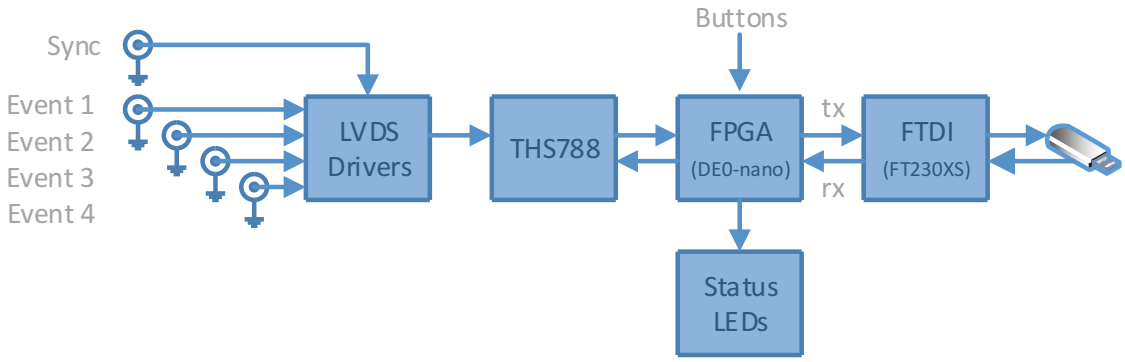


Figure 5.17: Block diagram of evaluation board with THS788

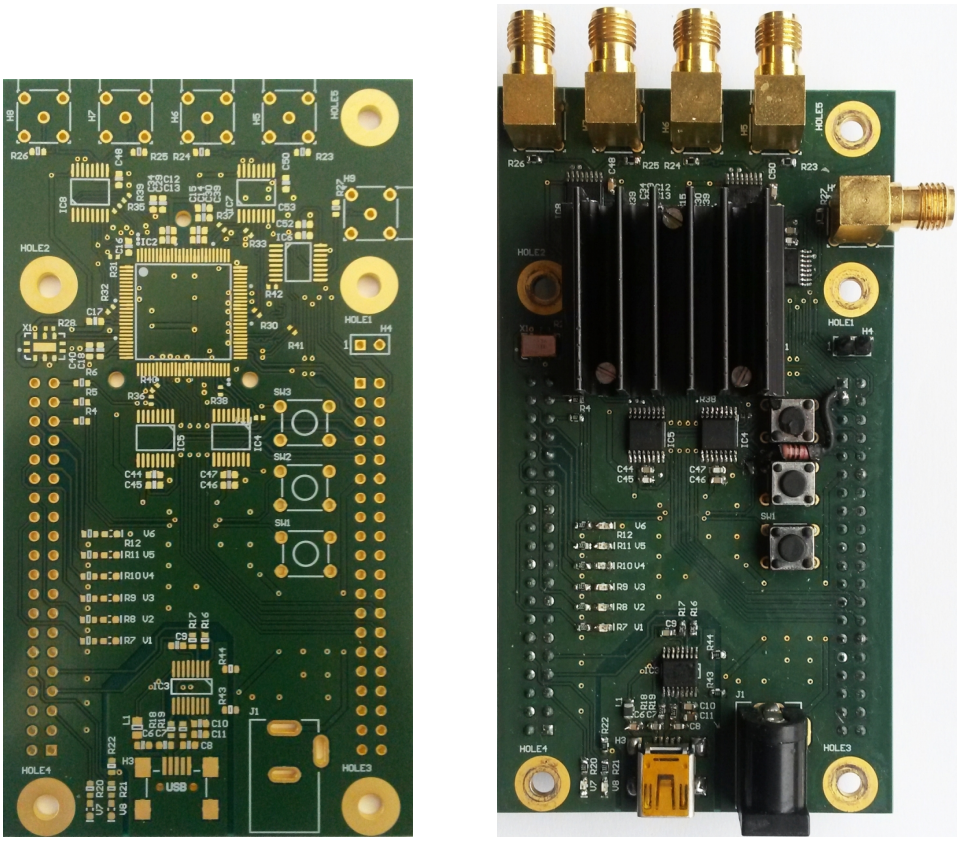
The DE0-nano development kit from Terasic[3] is populated with a Cyclone IV chip (EP4CE22F17C6). The development kit contains two 2×20pin headers which are used for communtication with THS788. The kit features an analog-to-digital converter. The die temperature of THS788 is measured by the ADC available on the kit. After the functionality test of the evaluation board with an FPGA development kit, the next step is considering to design a new TDC with improved parameters. The FPGA development kit is a good solution as a baseboard platform, but the FPGA uses only necessary additional components on the kit.

[3]Terasic Technologies Inc., Taiwan

A short description of the evaluation board is in the next subsection (Subsection 5.3.1).

5.3.1 Evaluation board THS788

The board designed in Altium designer was manufactured for test purposes. The basic components on the board and communication between the FPGA and the computer has already been tested. Because of that, a firmware was developed for read-out of the THS788. The next figure shows PCB - (a) unpopulated and (b) populated.



(a) Unpopulated (b) Populated

Figure 5.18: Evaluation board

The measuring single ended inputs of TDC on PCB are populated with SMA connectors with a 50Ω impedance. The board is populated with LVDS transceivers SN65LVDS049 [5] from TI. These chips contain drivers and receivers. The receivers are used for results interface of the THS788 in order to have LVCMOS inputs for FPGA data processing. Table 5.4 shows the features of LVDS transceivers. The UART is chosen for communication between TDC and the FTDI chip. The USB ensures the communication between FTDI chip and the computer. The FTDI chip FT230XS [10] emulates a virtual COM port in the computer. The parameters are in Table 5.5.

Table 5.4: Parameters of LVDS transceivers

Parameter	*Value*
Supply voltage	3.3V
Signal rate	400Mbps
Driver propagation delay	1.4ns
Receiver propagation delay	1.9ns
Channel-to-channel skew	50ps

Table 5.5: Parameters of FT230XS

Parameter	*Value*
Supply voltage	5V
Data rate	300Bd - 3MBd
Output	3.3V CMOS

In the next figure (Fig. 5.19), the whole TDC can be seen, i.e. the evaluation board with the THS788 connected to the DE0-nano development kit.

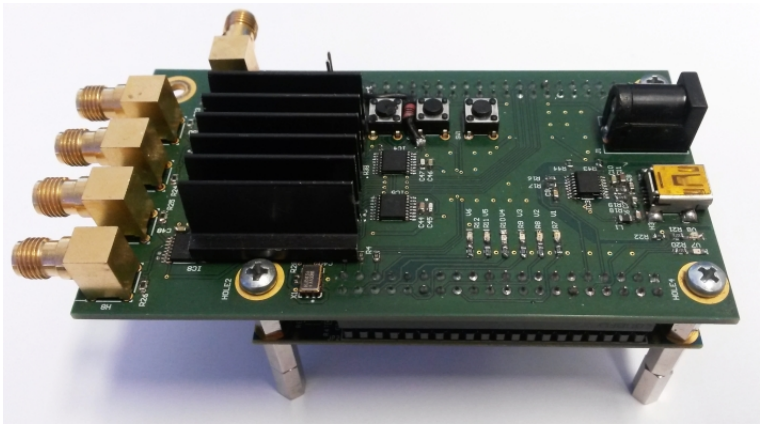


Figure 5.19: Photo of the TDC device

5.3.2 TDC read-out system in FPGA

The read-out firmware was designed in VHDL. The system is divided into several parts:

- a control unit
- a host state machine
- a result processing unit
- a temperature unit
- a communication unit

The block diagram is shown in Fig. 5.20. The communication unit uses standard UART protocol. It is established between the TDC and a computer. A specific packet with a header (55_{H}) and a tail ($\mathrm{AF_H}$) ensures the correct control data, otherwise the data is not used. A finite state machine has to gather the data into the packet (the description of the packet will be mentioned in Subsection 5.4.1).

The control unit switches between the communication unit and the host state machine or the communication unit and the result processing unit.

The host state machine controls communication between the FPGA and the THS788. It ensures the correct reading and writing process of control registers in THS788.

The result processing unit is responsible for the result interface of the THS788 chip. The interface has its own clock domain, which is generated by the THS788. It can be from 75MHz up to 300MHz. Because of the resynchronization to another clock domain, the FIFO in FPGA is necessary.

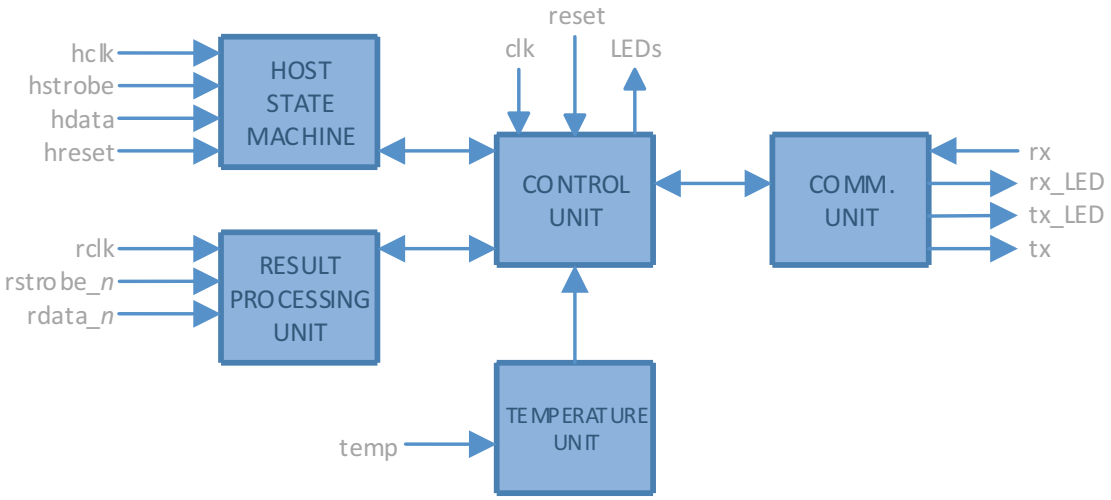


Figure 5.20: Block diagram of control firmware

The temperature unit controls the ADC on the DE0-Nano development kit and it computes the die temperature of the THS788 according to the obtained number from the ADC. The temperature measurement is made continuously and the die temperature is put into every packet transmitted to the PC. The ADC on the DE0-Nano kit is ADC128S022. It is a 12-bit converter. The reference voltage is 3.3V (U_{ref}) . The resolution of the converter (ΔU_{ADC}) is obtained by the following formula.

$$\Delta U_{ADC} = \frac{U_{ref}}{2^n} = \frac{3.3}{2^{12}} = 0.0008V = 0.8mV \tag{5.7}$$

According to the THS788 datasheet, the temperature dependence ($U_{1\mathrm{C}}$) is 5mV per 1°C. The temperature resolution of one bit of ADC ($\Delta \mathrm{T_{ADC}}$) is computed by formula 5.8.

$$\Delta T_{ADC} = \frac{\Delta U_{ADC}}{U_{1C}} = \frac{0.8}{5} = 0.16\frac{^\circ C}{b} \tag{5.8}$$

The temperature resolution is sufficient for 8-bit unsigned representation (1 bit is 1°C), which is used in the read-out system.

5.3.3 THS788 Power dissipation

The temperature can effect the stability of the results even if there is an internal compensation. Because of that, there has to be a heatsink on the chip or some kind of active cooling. The TEMP pin of the THS788 provides the voltage corresponding to the die temperature. The pin can be used for active cooling. Parameteres for passive cooling are shown in Table 5.6.

Table 5.6: Thermal parameters of THS788

Parameter		*Value*
Junction temperature (max)	υ_j	105°C
Ambient temperature	υ_a	25°C
Resistance - junction to pad	R_{jc}	3.11W/°C
Resistance - pad to heatsink	R_{cs}	0.2W/°C
Total power	P	3.0525W

The heatsink parametrs should be calculated from thermal resistances mentioned above. It is done with the following formula (5.9):

$$P \leq \frac{\vartheta_j - \vartheta_a}{R_{jc} + R_{cs} + R_{sa}} \tag{5.9}$$

After putting the values into formula 5.9:

$$3.0525 \leq \frac{105 - 25}{3.11 + 0.2 + R_{sa}} \tag{5.10}$$

Now the parameter of the thermal resistance of the heatsink is obtained.

$$R_{sa} = 22.998 \frac{W}{°C} \tag{5.11}$$

The results correspond to operation of all 4 channels, 300MHz clock frequency of results interface and 34bits wide result word.

The temperature measurement was made without heatsink using the TEMP pin of THS788, which provides the information about die temperature. The ADC on the DE0-Nano is used for the measurement. The conversion from Volts into the degrees of Celsius is done in FPGA with integer representation. The following figure shows one hour measurement with the THS788 in different modes. The used modes for the measurement are:

- RCLK (result clock) disabled and all channells disabled
- RCLK enabled and all channels disabled
- RCLK enabled, channel 1 enabled and channel 2-4 disabled
- RCLK enabled, channel 1-2 enabled and channel 3-4 disabled

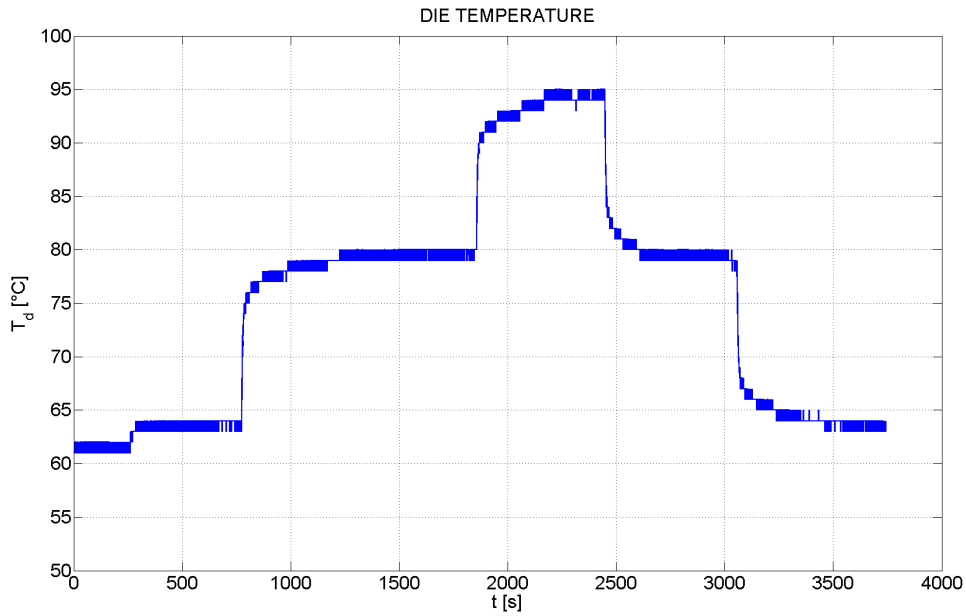


Figure 5.21: Die temperature of the THS788 in different modes

The temperature is shown in Fig. 5.21. The first mode (up to 250s) is with disabled RCLK generation (quiet mode). After several minutes, the RCLK are enabled (250s-750s, the second mode). It causes an increase in temperature of 2°C. Then the first channel is enabled (750s-1850s) and after several minutes the second channel is enabled (1850s-2500s). Then the channels are disabled one by one.

From the plot, the temperature dependance on the number of running channels can be seen. It is 15°C per enabled channel without any heatsink. The third and the fourth channels are disabled as a precaution and they are not used for the measurement, because the final temperature would probably be above120°C.

5.4 TDC with the THS788 - USB3.0 with return channel

According to the previous TDC with USB2.0, the new version of TDC was designed in order to increase the data throughput and to make synchronization easier. The main difference is in the communication between TDC and the PC and the return channel dedicated to the synchronization.

The communication is established with the FTDI chip FT600Q [9] via USB3.0. The FTDI chip is a USB3.0 to FIFO bridge. The parameters of the chip are in Tab. 5.7. The width of the FIFO bridge is 16b. The clock frequency of the FIFO is either 66MHz or 100MHz. According to the frequency and the FIFO width, the maximum data rate is either 1.056Gbps or 1.6Gbps, which is significantly better than the previous version.

Table 5.7: Parameters of FT600Q

Parameter	*Value*
Supply voltage	3.3V
Data rate (FIFO)	Up to 1.6Gbps
FIFO Width	16b

The synchronization principle of several TDCs is mentioned in the previous chapter. Due to the synchronization based on the propagation delay measurement, the return channel is added into the TDC. The synchronization signal to the TDC propagates into the timing chip itself and back through the return channel. A block diagram is shown in Fig. 5.22.

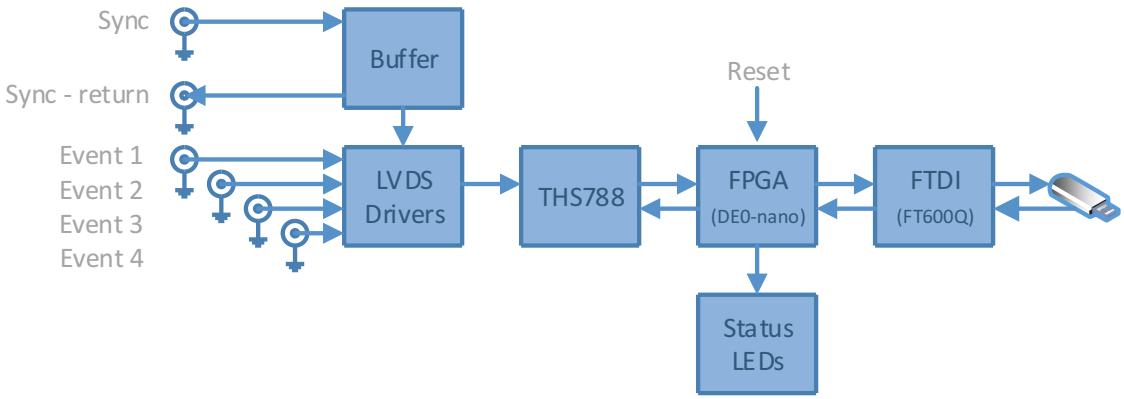


Figure 5.22: Block diagram of TDC with USB3.0

The block diagram is very similar to the previous version of TDC described in the section before. The main difference is the return channel as already mentiond. The return channel is provided with the clock buffer chip CDCLVC1102 [4] from TI. The main interesting parameters of the chip are in Tab. 5.8. The communication with the THS788 chip is done by the FPGA in the development kit, it is the same as the previous version.

Table 5.8: Parameters of CDCLVC1102

Parameter	*Value*
Supply voltage	2.5V or 3.3V
Additive jitter	$<$ 100fs
Pin-to-pin skew	$<$ 50ps
Maximum frequency	250MHz (3.3V)

The TDC with USB 3.0 was designed as a fully operational stand-alone device. The assembled PCB of the TDC with a passive heatsink from the top view is shown in Fig 5.23. The TDC in the housing is seen in Fig. 5.24 from the measurement inputs side and in Fig. 5.25 from the communication side (microUSB 3.0 connector, status LEDs, reset button and power jack connector).

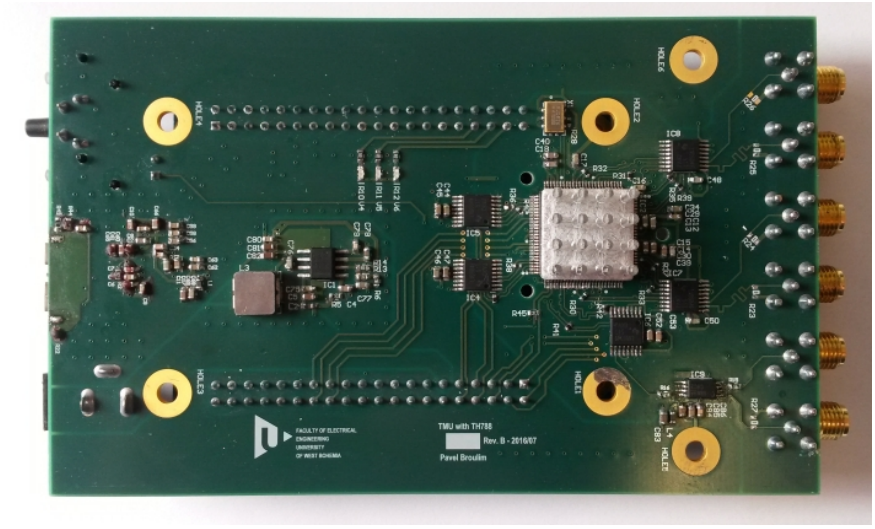


Figure 5.23: Top view of assembled PCB of TDC with USB3.0

Figure 5.24: Photo of TDC with USB3.0 from the measurement inputs side

Figure 5.25: Photo of TDC with USB3.0 from the communication side

5.4.1 Simulations

Because the main part is the same as the previous version, only the necessary simulations of the firmware in FPGA were done. The reported simulations are done for communication between FPGA and FTDI. The next figures show the write operation (from FPGA to FTDI) and read operation (from FTDI to FPGA). The communication uses a 64 bit wide packet with the header (55_{H}) and the tail ($\mathrm{AF_H}$) for the communication from the device, the structure is in Tab. 5.9. It means 48 bits for data. The packet is divided into 4 subpackets with 16b for FTDI. These subpackets are written into FTDI FIFO successively. It is seen in Fig. 5.26 for two different test packets, the whole packet as fifo_write_data_in signal and subpackets as ftdi_data signal (bidirectional FTDI 16 bit wide FIFO bus). In addition, there are other FTDI signals, with names corresponding to the pin name of the FTDI chip.

Table 5.9: Data packet from TDC

Head	*Data*	*Channel ID*	*Temperature*	*Tail*
8b	40b	2b	6b	8b
55_{H}	-	-	-	$\mathrm{AF_H}$

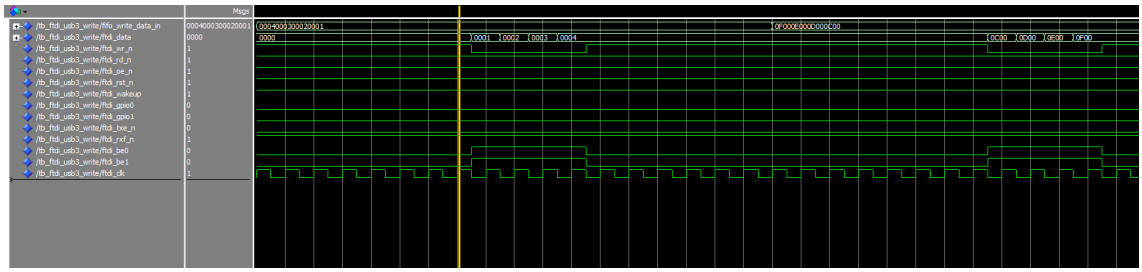


Figure 5.26: Simulation - Writing to FTDI

The packet for the communication into the device is only 48b wide. The header and

the tail are the same. The structure of the packet is in Tab. 5.10. The packet is wider in comparison with TDC with USB2.0 because of requirements for the width, which is a multiple of 16.

Table 5.10: Configuration packet to TDC

Head	*Operation code*	*Data*	*Tail*
8b	8b	24b	8b
55_H	-	-	AF_H

The operation code contains information about the mode of operation and an address of registers in the THS788. There are four modes, read registers, write regiters, idle and read results. The reading operation for the test packet ($5501020304AF_H$) is in Fig. 5.27. The signal names are the same as the write operation simulation. The received packet is stored in the received FIFO in 3 subpacktes (16 bit wide FTDI bus and 48 bit wide packet), the signal name is fifo_read_data_out.

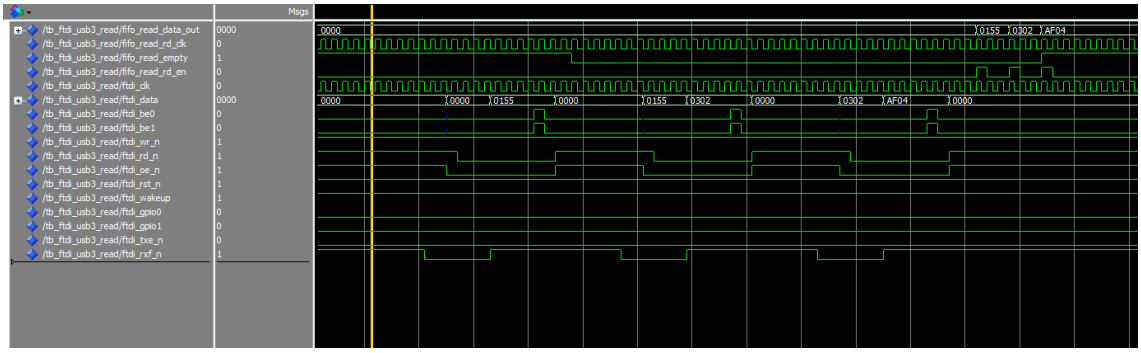


Figure 5.27: Simulation - Reading from FTDI

5.4.2 PC Control application

The control application is written in three versions (the full version, the lite version and the user version) in the C# language in Microsoft Visual studio as .NET application, which requires .NET framework.

The full version is an application, which allows access to registers in TDC by a user and to change values in the registers according to the user.

The lite version is a click-and-log application, which allows setting of the TDC by one click on the button.

The necessity of using the TDC by people who are not familiar with the TDC has led to development of the user version.

Full version

The full version is designed for reading and setting all registers, changing the TDC modes (four modes, read registers, write regiters, idle and read results) and data logging. The main purpose is debbugging. The screenshot of the full version is in Fig. 5.28.

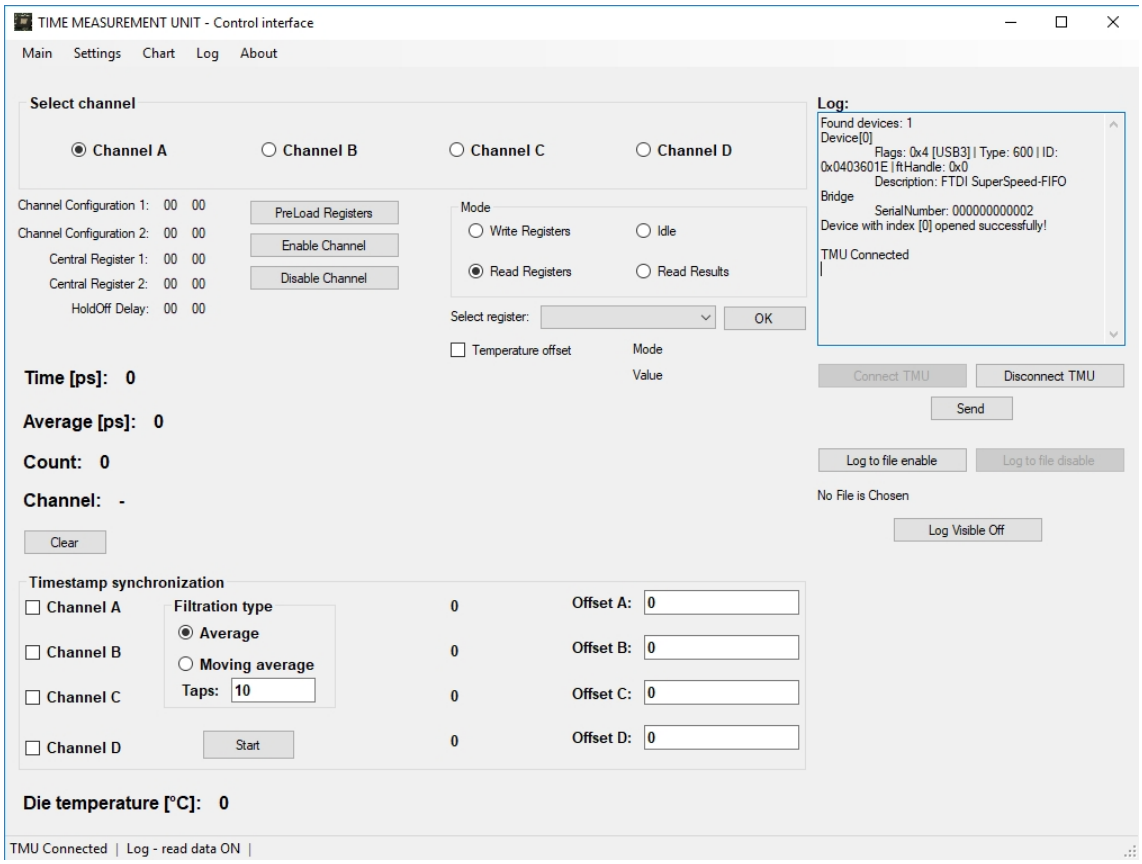
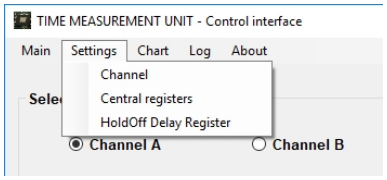
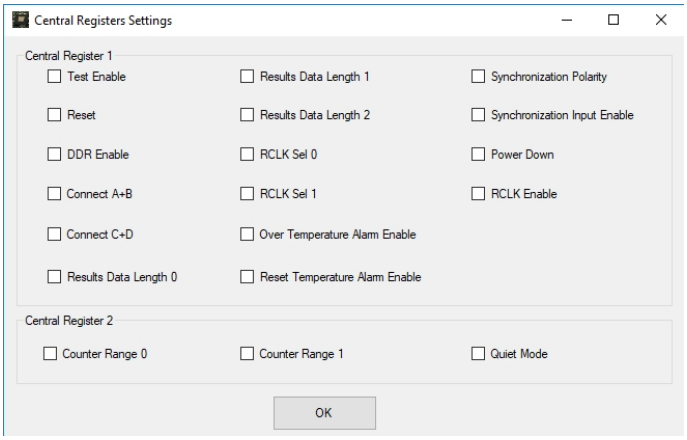


Figure 5.28: Screenshot of the full version

The connection with TDC is established by the Connect TMU button (on the right in the screenshot). The application searches all connected FTDI devices and select the TDC device according to the serial number. The split menu allows the register to be chosen, whose bits will be set. After the choice, the new window with bits in selected register will show. The next figure shows the split menu (Fig. 5.29a) and bit setting (Fig. 5.29b).



(a) Split menu



(b) Bit setting

Figure 5.29: Register settings

The channel being configured is chosen with the radio buttons. The operation mode is chosen with radio buttons (Mode group in the middle of the screenshot). After putting the

right values into the register and selecting the modes, the operation is confirmed by clicking on the OK button and the configuration packet is prepared. Then the configuration packet is sent using the Send button. The proper setting is confirmed by receiving the confirmation packet with $AAAAAA_H$ in the data field. The measured time interval is shown next to the label Time with the corresponding channel and the count of all received measurements for the channel of the last received value. It is convenient only for a slow data rate when the functionality is mainly tested (debbugging). For a higher data rate, it is necessary to save data into the file.

Lite version

This version is based on the full version, the communication core is the same, but the motivation is an application with easy and quick settings for taking data. As already mentioned, the lite version is a click-and-log application. The application provides the list of connected TDC devices. The TDC device can be opened. The lite version is focused on debbugging like the full version. There are 4 configurations of the measurement:

- measurement between the rising edge and the rising edge
- measurement between the rising edge and the falling edge
- measurement between the falling edge and the rising edge
- measurement between the falling edge and the falling edge

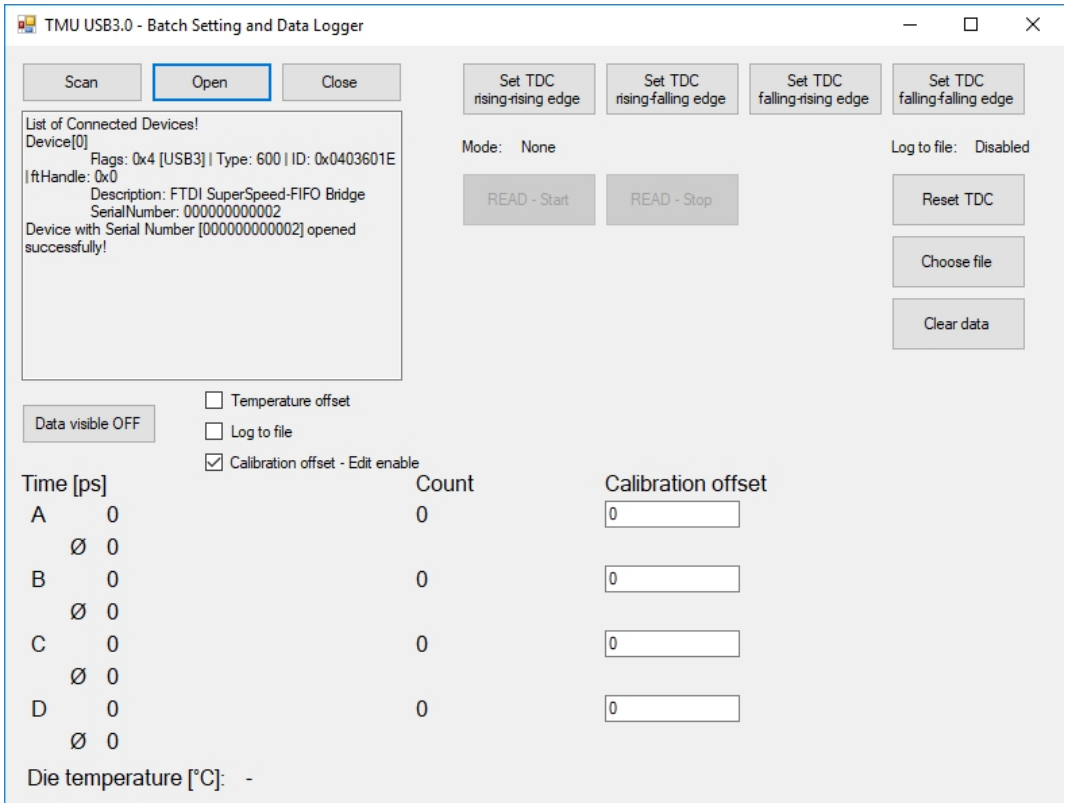


Figure 5.30: Screenshot of the lite version

The user selects one of the configurations. After that, the configuration is set and all channels are enabled. The next function of the lite version is logging data. The data can be saved into a selected file (new or existing) in text form. The 3 numbers are saved into the file, time interval, die temperatutere and channel id. The screenshot of the application is in Fig. 5.30 and the screenshot of the saved file is in Fig. 5.31.

In the screenshot, the buttons for the scan and opening or closing the device are seen on the left side. The configuration of the measurement is set with 4 buttons on the top. Read - start button and Read - stop button control the results read from the TDC. The file for data logging is placed on the right side. The current data can be seen on the bottom side.

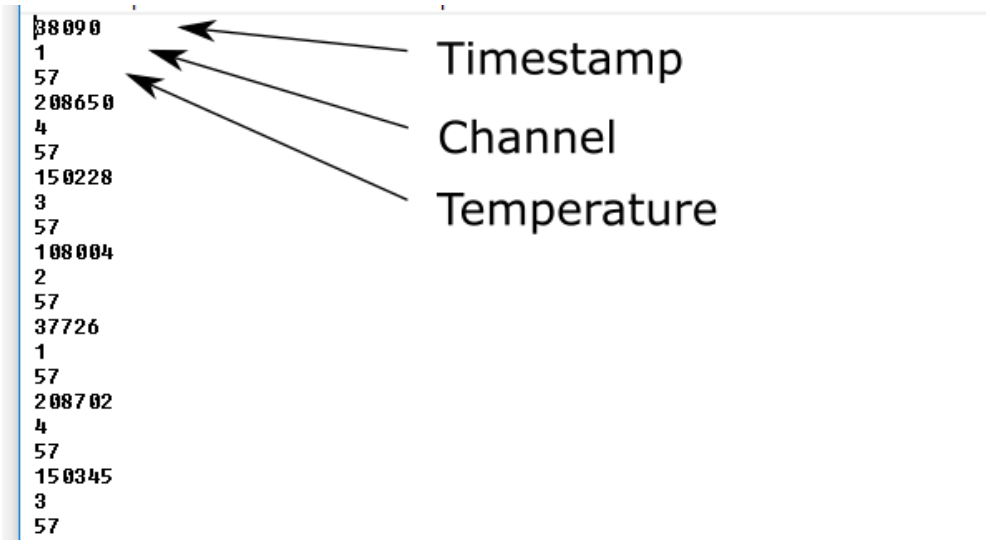


Figure 5.31: Sample of the text file

User version

Because of requests for using TDC in experiments, it was also necessary to prepare a control application in a more user friendly version for people who are not familier with TDCs. The main difference between the user version and the lite version is channel setting. The user version allows enabling channels separetly (lite version enables or disables all channels at once). The other options of measurement are kept and they can be chosen. The screenshot of the application is in Fig. 5.32

You can see the tabs with configuration settings in the screenshot. All settings for measurement (edge, start, stop, log to file, etc.) are done through these tabs. The tabs are shown in Fig. 5.33. One of the tabs is intended for calibration. The calibration data can be filled in the tab and the TDC uses them. A detailed description of the calibration is in Subsection 7.2.1.

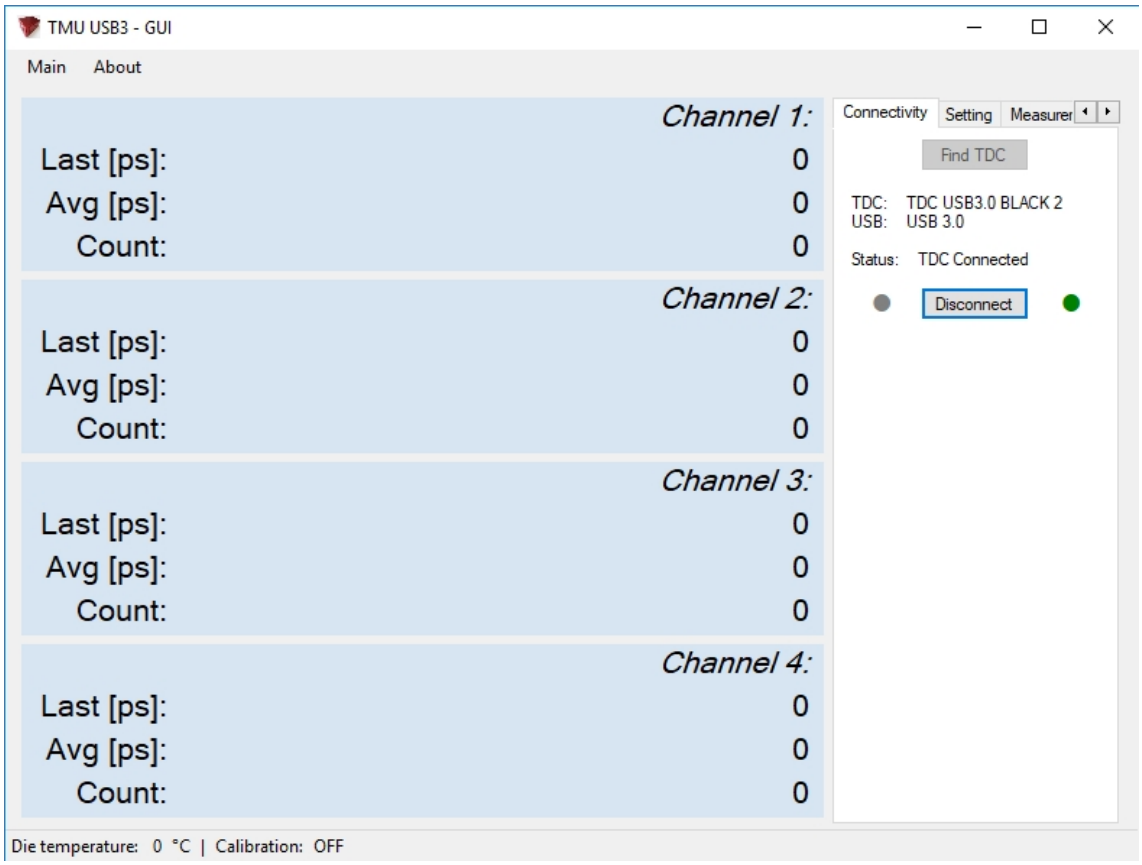


Figure 5.32: Screenshot of the user version

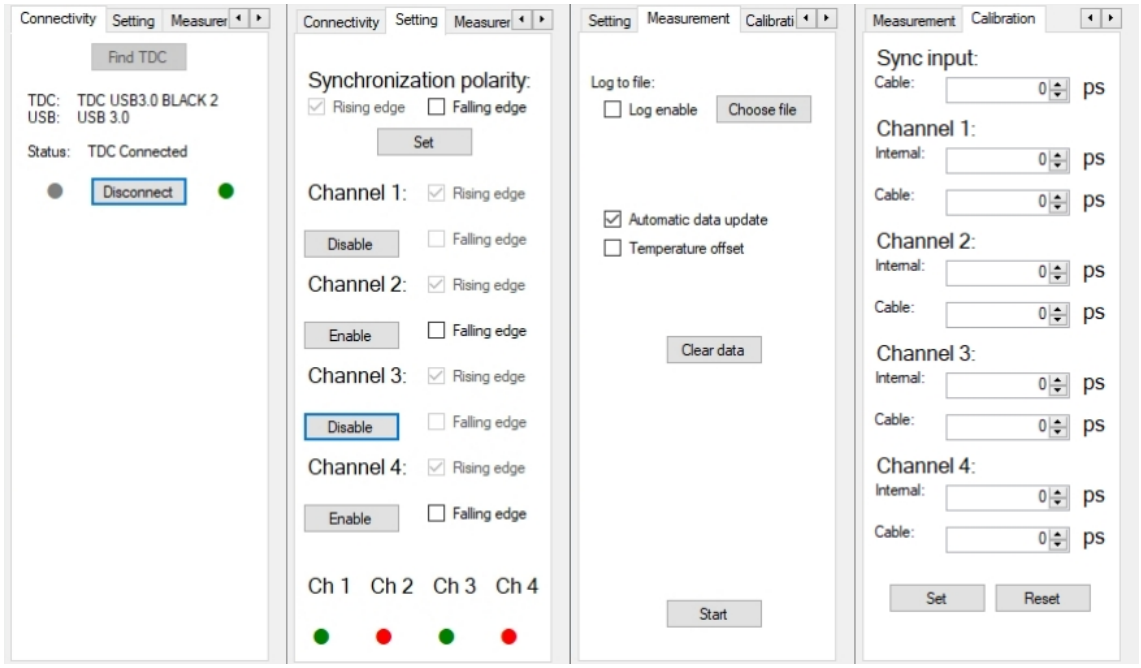


Figure 5.33: Tabs for TDC configuration

Chapter 6

Error analysis

Currently, time measurement is a very relevant problem, especially with very high resolution. The desired resolution reaches common values of jitter of the high speed components (in order of picoseconds or hundreds of femtoseconds). Thus an error and uncertainty of the measurement have to be analyzed. The question is how to decrease the error and the uncertainty to their minimum. The question leads to two solutions. The first way is focused on component selection. The other deals with the electrical parameters of the components. The pros and cons of each will be shown and summarized.

6.1 Component selection

This approach is based on focusing on the specific parameters of components, which results in the choice of component. Suppose that time measurement (TDC) has a specific resolution (t_{TM}) and the rising (t_{r}) or the falling (t_{f}) edge of the measured signal has its duration. When the edge of the signal is faster than the resolution of the time measurement, the influence of the jitter, drift and other timing parameters will be minimized. The relation between the rising edge and the resolution of the time measurement is described with formula 6.1. Formula 6.2 describes the relation between the falling edge and the resolution.

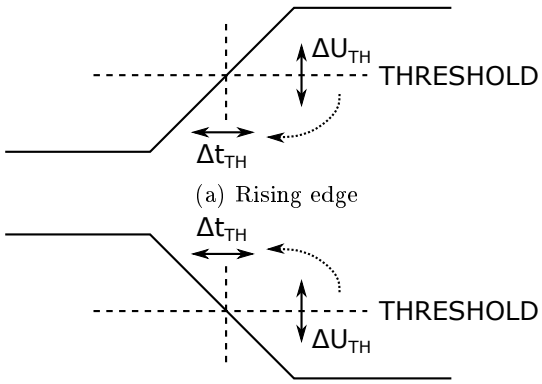
$$t_{TM} \gg t_r \tag{6.1}$$

$$t_{TM} \gg t_f \tag{6.2}$$

Meeting these requirements reduces the error and the uncertainty as mentioned before. The error is caused either by fluctuation of the threshold of components input or the jitter. If the formulas are followed, the error or uncertainty will be under the capability of the time measurement.

6.2 Parameters selection

In the datasheet, there are several important parameters, such as jitter, skew, drift with the temperature, supply voltage, etc. For the following formulas and calculations, suppose the time measurement with the resolution t_{TM} and the rising (falling) edge are related to 1V (t_{r1V}, t_{f1V}). The input of time measurement has a threshold which can vary with supply voltage, temperature, etc. This is shown for the rising edge and the falling edge in the following figure (Fig. 6.1).



(a) Rising edge

(b) Falling edge

Figure 6.1: Threshold variation

The following calculations will give us the limit of the slope of the rising edge or the falling edge (the measurement can use both) which is enough to not degrade the resolution of the time measurement. In other words, the slope of the edge, which is in the interval of the threshold voltage related to the resolution of time measurement. Using the following calculations with particular values will be mentioned in Section 6.3 which is focused on the TDC with the THS788 chip.

6.2.1 Influence of the threshold drift with supply voltage – $\Delta U_{\mathrm{THsupply}}$ [V/V]

$$\Delta U_{THsuppmax} = \Delta U_{THsupply} \cdot \Delta U_{supply} \tag{6.3}$$

$$t_{r1V} = \frac{t_{TM}}{\Delta U_{THsuppmax}} \tag{6.4}$$

$$t_{f1V} = \frac{t_{TM}}{\Delta U_{THsuppmax}} \tag{6.5}$$

Formulas 6.4 and 6.5 give the condition for the rising or the falling edge of the measured signal (will be used for calculation with the THS788 chip, Section 6.3).

6.2.2 Influence of the threshold drift with temperature – ΔU_{THtemp} [V/°C]

$$\Delta U_{THsuppmax} = \Delta U_{THtemp} \cdot \Delta T \tag{6.6}$$

$$t_{r1V} = \frac{t_{TM}}{\Delta U_{THtempmax}} \tag{6.7}$$

$$t_{f1V} = \frac{t_{TM}}{\Delta U_{THtempmax}} \tag{6.8}$$

6.2.3 Combination of several influences

The influence of the supply voltage and the temperature are combined together which create the next formulas:

$$\Delta U_{TH} = \Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T \tag{6.9}$$

For the rising edge:

$$t_{r1V} = \frac{t_{TM}}{\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T} \tag{6.10}$$

For the falling edge:

$$t_{f1V} = \frac{t_{TM}}{\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T} \tag{6.11}$$

The denominator in formulas 6.10 and 6.11 can be extended by increments of other influences. From the formulas, the real resolution of the time measurement (t_{TMreal}) can be computed according to the components used. Formula 6.12 is for the rising edge and formula 6.13 is for the falling edge.

$$t_{TMreal} = t_{r1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \tag{6.12}$$

$$t_{TMreal} = t_{f1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \tag{6.13}$$

Then the absolute error ($\Delta error$) is:

$$\Delta error = \mid t_{TMreal} - t_{TM} \mid \tag{6.14}$$

For the rising edge:

$$\Delta error = \mid t_{r1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \mid \tag{6.15}$$

For the falling edge:

$$\Delta error = \mid t_{f1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \mid \tag{6.16}$$

The relative error ($error_{\mathrm{rel}}$) is:

$$error_{rel} = \frac{\Delta error}{t_{TM}} \tag{6.17}$$

The computed resolution is substituted with formula 6.15 or 6.16.
For the rising edge:

$$error_{rel} = \frac{\mid t_{r1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \mid}{t_{TM}} \tag{6.18}$$

For the falling edge:

$$error_{rel} = \frac{\mid t_{f1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \mid}{t_{TM}} \tag{6.19}$$

From the absolute error, the error interval is determined by formula 6.20.

$$\begin{aligned} \langle -t_{r1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T), \\ + t_{r1V} \cdot (\Delta U_{THsupply} \cdot \Delta U_{supply} + \Delta U_{THtemp} \cdot \Delta T) \rangle \end{aligned} \tag{6.20}$$

These values are applied to different signaling levels and a comparison is provided. The signal can be distributed as a single-ended signal or a differential signal. The amplitude of the rising edge or falling edge is calculated as a difference between high level (U_{H}) and low level (U_{L}). For the single-ended signal:

$$U_{edge} = U_H - U_L \tag{6.21}$$

For the differential signal:

$$U_{edge} = (U_{Hp} - U_{Hn}) - (U_{Lp} - U_{Ln}) \tag{6.22}$$

The transition is considered a linear transition. The edge voltage difference (U_{edge})is adjusted to the common standard between 10% of the edge voltage difference and 90% of the edge voltage difference used in datasheets. The adjusted edge voltage difference (U_{edgeadj}) is then obtained.

$$U_{edgeadj} = 0.8 \cdot U_{edge} \tag{6.23}$$

In the following table (Tab. 6.1), the edge voltage difference (U_{edge}) and the adjusted edge voltage difference (U_{edgeadj}) are shown for several signaling levels. The adjusted edge voltage difference can be used in calculations for the selection of components with the following steps:

- Calculation of the rising (falling) edge related to 1V (t_{r1V}, t_{f1V}) corresponding to the time measurement resolution (t_{TM})
- Specifying the signal levels (CMOS, LVPECL, LVDS, etc.)

- Calculation of the rising (falling) edge related to the chosen standard
- Finding proper components on the market

Table 6.1: Voltage levels

Signal level	U_{edge}[V]	U_{edgeadj}[V]
TTL	5	4
CMOS	3.3	2.64
CML	1.6	1.28
LVPECL	1.6	1.28
ECL	1.6	1.28
LVDS	0.8	0.64

The next table shows the relation among signal levels when the length of the rising edge or the falling edge is kept.

Table 6.2: Voltage levels

	TTL	*CMOS*	*CML*	*LVPECL*	*ECL*	*LVDS*
TTL	1	0.66	0.32	0.32	0.32	0.16
CMOS	1.51	1	0.48	0.48	0.48	0.24
CML	3.125	2.06	1	1	1	0.5
LVPECL	3.125	2.06	1	1	1	0.5
ECL	3.125	2.06	1	1	1	0.5
LVDS	6.25	4.125	2	2	2	1

From the tables it is seen that LVDS signals are the most convenient, when the slope rising (falling) edge is the same and it is determined with the power supply, the temperature, etc. But it is always good to consider other conditions which follow up from the system, e.g. already used components in the system, the length of the interconnections, etc.

6.2.4 Fluctuation of the power supply

When the same rising edge (the time interval) has to be used, the fluctuation of the power supply or the fluctuation of the temperature can be different. It is computed by the following formulas. Suppose we have two power supplies with $\Delta U_{\text{supply1}}$ and $\Delta U_{\text{supply2}}$ and have signal levels of U_{edge1} and U_{edge2}.

$$t_{rA} = t_{rB} \tag{6.24}$$

$$t_{rA1V} \cdot U_{edge1} = t_{rB1V} \cdot U_{edge2} \tag{6.25}$$

$$\frac{t_{TM}}{\Delta U_{THsupply} \cdot \Delta U_{supply1}} \cdot U_{edge1} = \frac{t_{TM}}{\Delta U_{THsupply} \cdot \Delta U_{supply2}} \cdot U_{edge2} \tag{6.26}$$

$$\Delta U_{supply1} = k \cdot \Delta U_{supply2} \tag{6.27}$$

$$\frac{t_{TM}}{\Delta U_{THsupply} \cdot k \cdot \Delta U_{supply2}} \cdot U_{edge1} = \frac{t_{TM}}{\Delta U_{THsupply} \cdot \Delta U_{supply2}} \cdot U_{edge2} \tag{6.28}$$

$$k = \frac{U_{edge1}}{U_{edge2}} \tag{6.29}$$

When the same time interval of the rising edge is kept, the fluctuation of the power supply used can be k (formula 6.29) times higher for the higher edge voltage difference. The k ratio is given for common signal levels in Table 6.2. If the same power source is used, the steepest rising edge or falling edge will have a higher edge voltage difference. It results in trying to choose signal levels (standards) with low amplitudes.

6.2.5 Jitter analysis of the rising and falling edge

Analysis of the jitter is divided into 2 parts. The first part is focused on the jitter less than the resolution of the time measurement, i.e. following formula 6.30 (6.31). In that case, the jittter does not degrade the resolution t_{TM}.

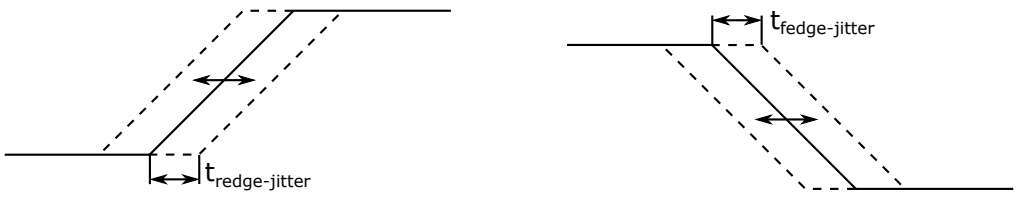
$$t_{TM} \gg t_{redge-jitter} \tag{6.30}$$

$$t_{TM} \gg t_{fedge-jitter} \tag{6.31}$$

The other part of the analysis is of jitter higher than the resolution t_{TM}. The idea is shown in Fig. 6.2. In that case, the error is proportional to the jitter (see formula 6.32).

$$error_{jitter} = 2 \cdot t_{redge-jitter} \tag{6.32}$$

$$error_{jitter} = \pm t_{redge-jitter} \tag{6.33}$$



(a) Rising edge (b) Falling edge

Figure 6.2: Jitter

6.3 Error analysis with the THS788 chip

In the previous chapter, the TDC device with THS788 is described. The formulas mentioned in Section 6.2 help to find parameters of signals which are applied on the input of TDC and the signals don't worsen the time resolution of TDC. Sections 5.3 and 5.4 deal with TDC based on the THS788 chip. We can put its LSB time resolution into the aforementioned formulas. Suppose the rise time of the signal on the input of the TDC board is 1ns (t_{r}) at 3.3V CMOS signal level and the time resolution (t_{TM}) of TDC is 13 ps according to the datasheet.

$$t_{r1V} = \frac{t_r}{3.3} \tag{6.34}$$

$$t_{r1V} = \frac{1 \cdot 10^{-9}}{3.3} = 0.303 \frac{ns}{V} \tag{6.35}$$

$$\Delta U_{TH} = \frac{t_{TM}}{t_{r1V}} \tag{6.36}$$

$$\Delta U_{TH} = \frac{13 \cdot 10^{-12}}{0.303 \cdot 10^{-9}} = 0.0429V = 42.9mV \tag{6.37}$$

These results mean that the fluctuation of the threshold level due to supply voltage, temperature, etc., which is less than 42.9mV, is negligible because it is under the recognition capability of the TDC.

We also use the opposite approach of the calculation. If the fluctuation of the threshold level is known, the maximum rise time of the measured signal can be computed. Suppose the fluctuation (ΔU_{TH}) is 25mV and the TDC resolution (t_{TM}) is 13ps.

$$t_{r1V} = \frac{t_{TM}}{\Delta U_{TH}} \tag{6.38}$$

$$t_{r1V} = \frac{13 \cdot 10^{-12}}{0.025} = 0.52 \cdot 10^{-9} = 0.52ns \tag{6.39}$$

The slope of 0.52ns results in a rising edge of 1.716ns for 3.3V CMOS signal level which is achievable with common components on the market.

Chapter 7

Measurements with designed TDCs

An important part of designing TDC is its testing and measuring. This chapter is divided into two parts according to the designed TDCs. To be specific, the first part is focused on the TDC with communication based on USB2.0, which is primarily designed as a board for a functionality test. The other part deals with TDC with communication via USB3.0 for a higher data rate. This TDC is improved according to experiences with the former TDC.

7.1 TDC with the THS788 - USB2.0

The TDC with USB2.0 is the first prototype of the designed TDC. The prototype was tested for functionality of the THS788. It means measurements of time differences between two signals, pulse width, etc. The first functionality test was done by a continuous input signal measurement. It should measure the quality of the splitter, whose parameters are known and checked with oscilloscope. The measured test setup is shown in Fig. 7.1.

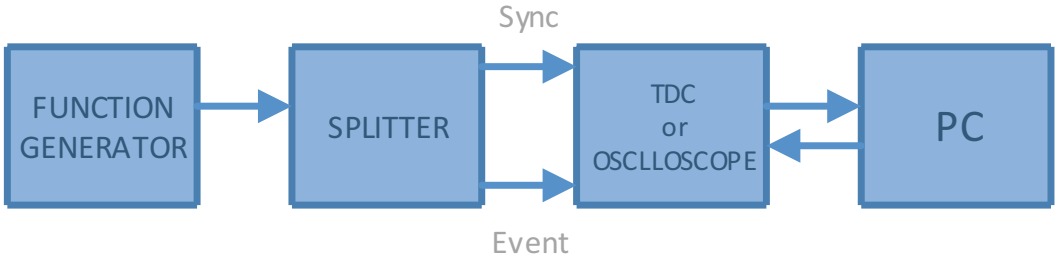


Figure 7.1: Test setup

Table 7.1: Parameters of the generated signal

Parameter	*Value*
Mean	-30fs
Min	-1.2ps
Max	98.8ps
Δt	100ps
Standard deviation	10.203ps

The interconnection in the test setup was established with the same cable (material, length, etc.) using a splitter with a 50Ω impedance on the input and outputs. In the setup, the time measurement unit measures the jitter of the edge in generated signal (time difference between sync input and event input). The time difference should be zero. This was proved by an oscilloscope and its statistical measurement calculations. The results are shown in Tab. 7.1. The mean value is almost zero, corresponding to the previous assumption. The maximum time difference is 100ps. The next figure (Fig. 7.2) shows the histogram of the data which is taken by TDC with the read-out system. The histogram is fitted with the Gauss probability distribution function. The difference between the maximum and the minimum value is 260ps. It can be seen in Tab. 7.2.

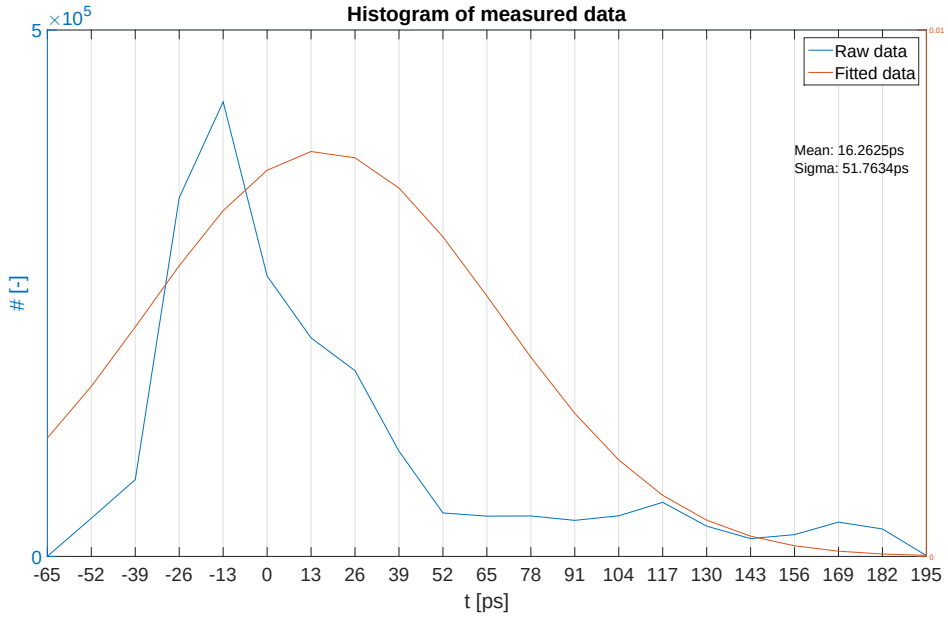


Figure 7.2: Histogram of measured data by TDC

Table 7.2: Measured parameters of the generated signal by TDC

Parameter	*Value*
Mean	16.2625ps
Min	-65ps
Max	195ps
Δt	260ps
Standard deviation	51.7634ps
Samples	4500000

The histogram was also taken for two different ambient temperatures, which were provided by a climatic chamber. The histograms are plotted in Fig. 7.3. The difference between ambient temperatures is 20°C. The die temperature is 40°C during the 10°C ambient temperature. During a temperature of 30°C, the die temperature is 50°C. Each temperature was set constant for 24 hours in the climatic chamber. The difference of 20°C has minimal effect on the results. The statistical parameters are in Tab. 7.3.

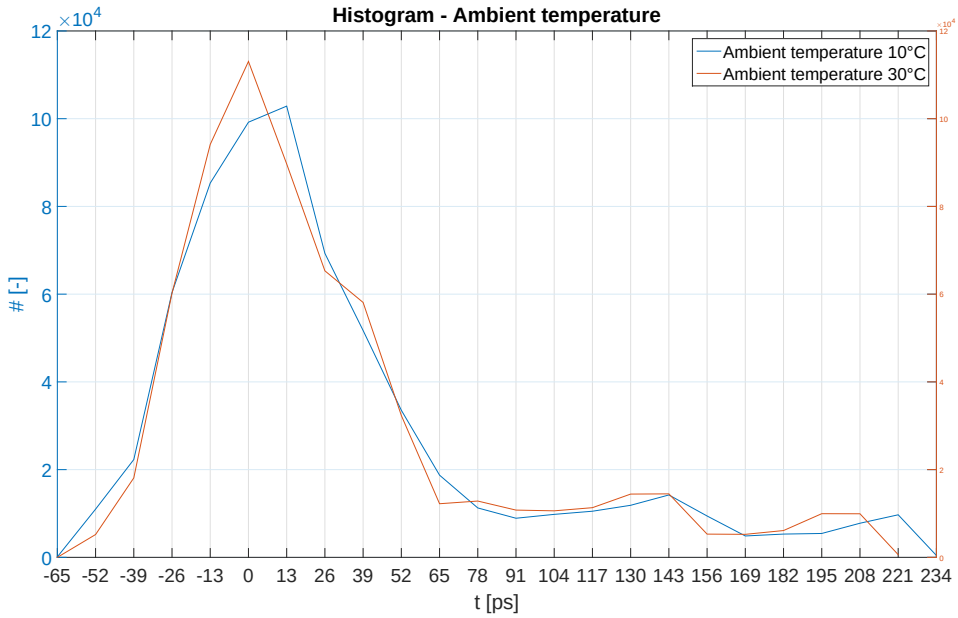


Figure 7.3: The effect of ambient temperature

Table 7.3: Statistical parameters for two ambient temperatures

Parameter	*Ambient temperature*	
	10°C	30°C
Mean	29.6542ps	29.0360ps
Standard deviation	59.0742ps	56.7426ps

As mentioned in Chapter 4, the TDC can be used for the propagation delay measurement. The measurement can be repeated and a moving average FIR filter can be applied.

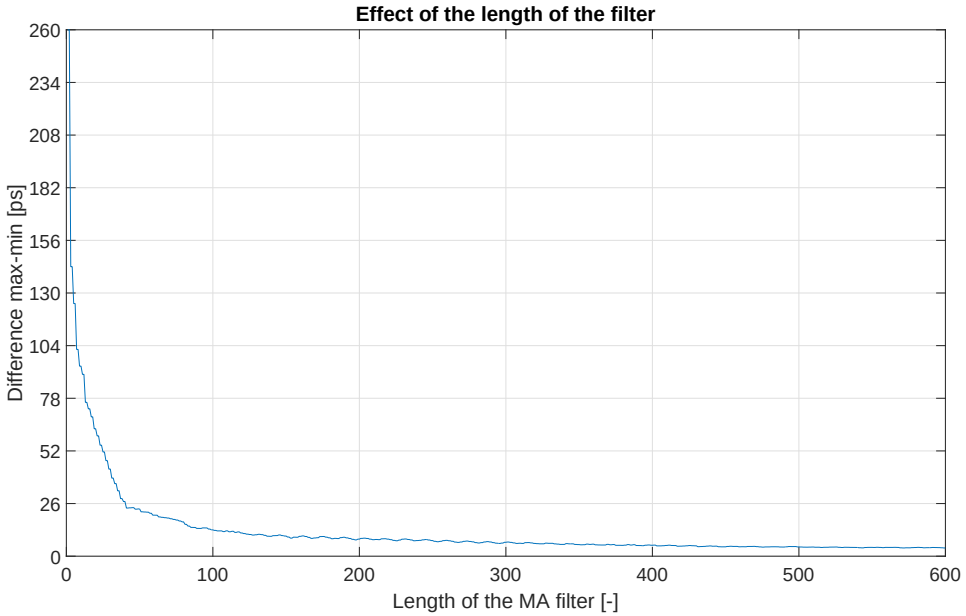


Figure 7.4: Effect of the length of the filter

Fig. 7.4 shows the effect of the length of the filter. The difference between the maximum and the minimum value decreases to 10-20ps, which is the resolution of the THS788.

Another measurement mentioned in the beginning of this part is the pulse width measurement. The time difference was taken between the rising and the falling edge of the pulse. The rising edge triggers the measurement and the measurement is ended at falling edge. The jitter of the generator used is higher than the resolution of the THS788, thus the measured jitter should be the same or less. The same test setup as in Fig. 7.1 is used for the pulse width measurement.

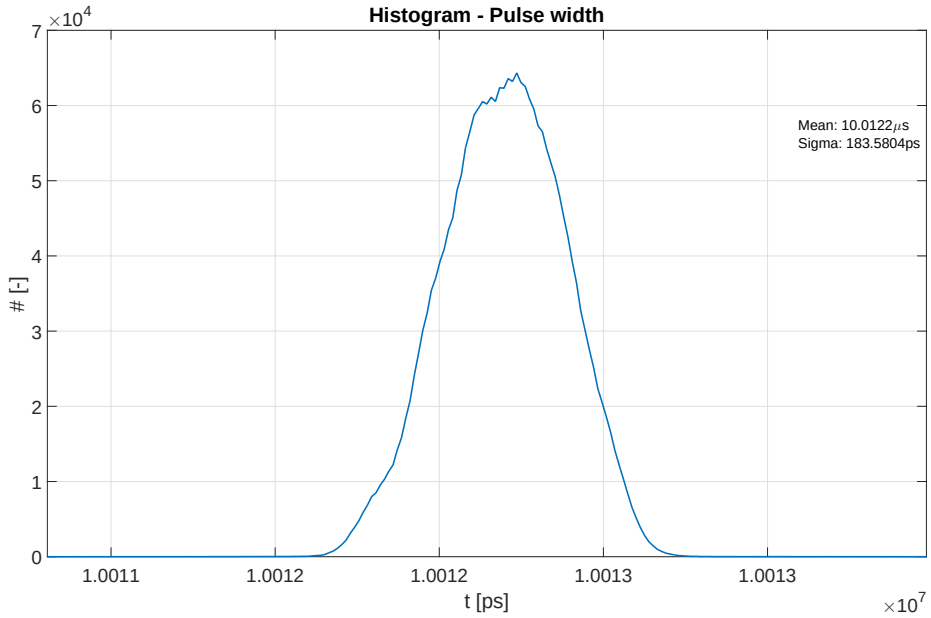


Figure 7.5: Pulse width measurement

According to the datasheet, the jitter is ±100ppm+500ps. The generated pulse was 10µs wide. It results in ±1.5ns jitter. The histogram is shown in Fig. 7.5. From Fig. 7.5, the jitter (worst-case) is ±1339ps. It corresponds to the datasheet of the generator.

7.2 TDC with the THS788 - USB3.0 with return channel

The improved device based on experience with TDC - USB2.0 was developed in order to obtain a higher data rate and add the return channel. The improvements and the description of upgrades are described in Chapter 5. The main differences are the communication via USB3.0 and the return channel which propagates the sync signal from the input to the output. It causes the need of calibration in order to equalize all inputs of TDC to zero.

The return channel itself causes a delay of the sync signal, in other words the measuring time differences of signals with no shift between them results in a negative time (time offset). The calibration is done by the offset measurement.

The next important measurement is a linearity. It means the comparison of the measured shift of a signal and the shift set on the generator (as a reference).

Then other types of measurements will be shown, such as the pulse width measurement or the propagation delay of a transmission line measurement.

7.2.1 Calibration

As already mentioned, the calibration is based on the measurement of the time offset on the inputs of TDC. For the offset measurement, signals with no time difference between them are necessary. This requires a generator with at least two outputs. The TDC measures the offset of the channel itself in such configuration. The condition of no time difference is very hard to achieve, thus it is better to calculate the offset from three measurements. But the configuration requires a generator with at least three outputs. The offset calculation describes the following equations and plots.

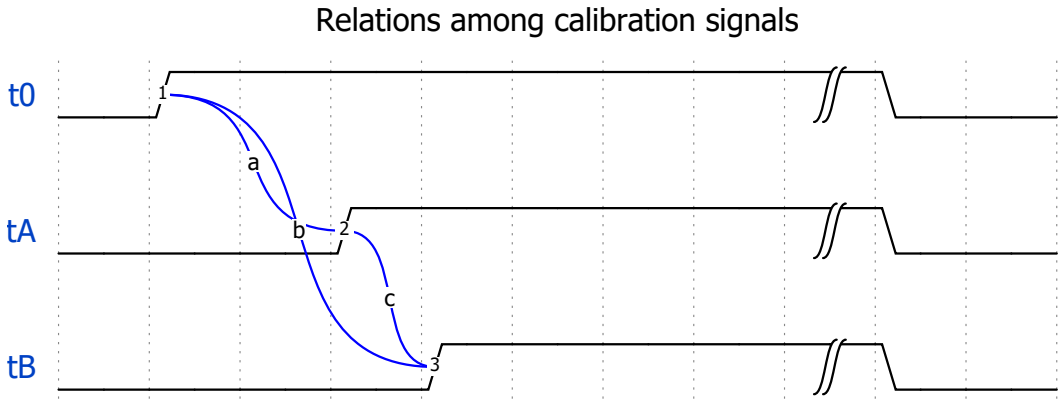


Figure 7.6: Calibration signals

The relations among the signals (generated by the generetor) are seen in Fig. 7.6. The shift between signal t_0 and t_A is a, the shift between t_0 and t_B is b and the shift between t_A and t_B is c. The measured values are t_1, t_2 and t_3. They consist of time a, b or c and offset (o_1).

$$t_1 = a + o_1 \tag{7.1}$$

$$t_2 = b + o_1 \tag{7.2}$$

$$t_3 = c + o_1 \tag{7.3}$$

We obtain the shifts (a, b, c) from formulas.

$$a = t_1 - o_1 \tag{7.4}$$

$$b = t_2 - o_1 \tag{7.5}$$

$$c = t_3 - o_1 = t_2 - o_1 - (t_1 - o_1) = t_2 - t_1 \tag{7.6}$$

We can calculate the offset from the following formulas.

$$t_3 - o_1 = t_2 - t_1 \tag{7.7}$$

$$o_1 = t_3 - t_2 + t_1 \tag{7.8}$$

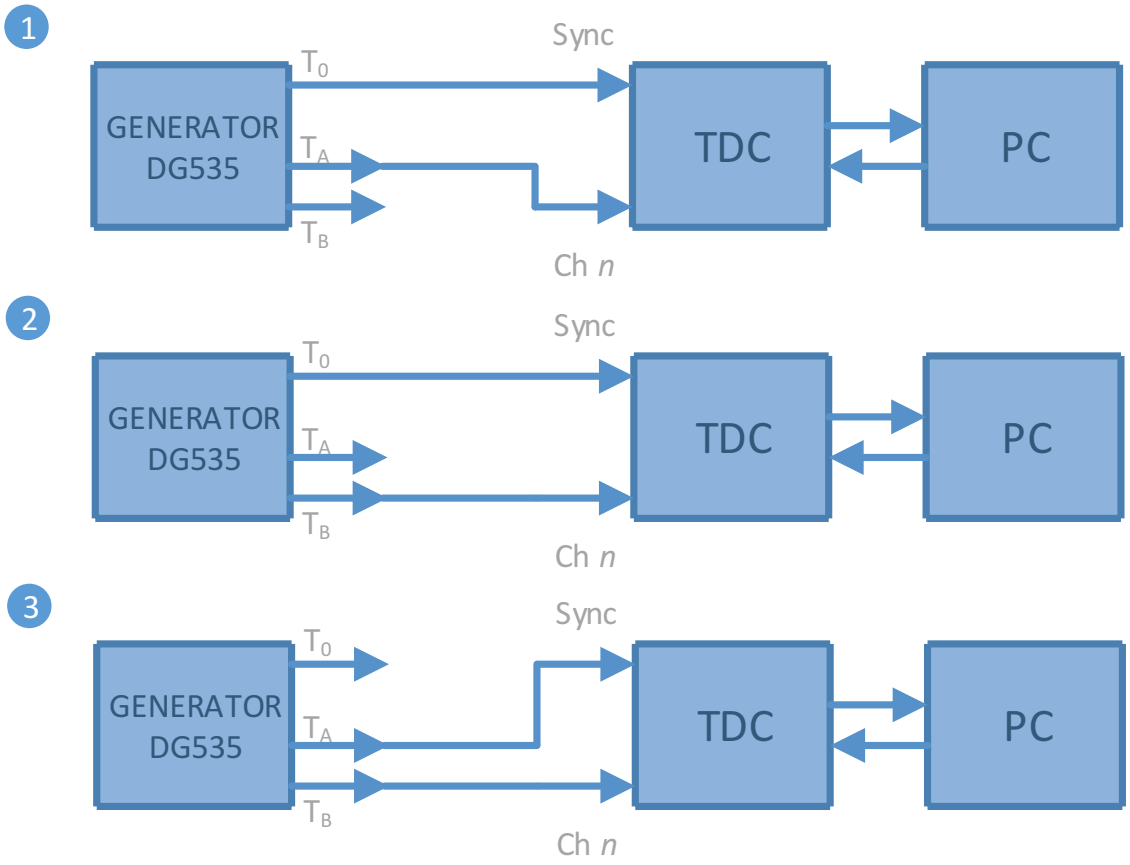


Figure 7.7: Calibration setup

The calculated value o_1 determines offset for the first channel. The other channels are calibrated in the same way with the same formulas. The calibration setup in steps is in Fig. 7.7. The label Ch_n means the chosen channel of the TDC and a calibration is done for the chosen channel in three steps.

The digital delay pulse generator is used for the calibration. The model is SRS DG535. The main parameters are shown in Tab. 7.4.

Table 7.4: Parameters of DG535

Parameter	Value
Number of channels	Trigger + 4
Amplitude level	Up to 4V
Delay resolution	5ps
Channel-to-channel jitter	50ps
Maximal internal trigger rate	1MHz
Accuracy	500ps (typ) + 1ppm (TCXO) × Time between outputs

Because of the jitter level, the three signal approach for the calibration (described previously) is used instead of two signals. Each time value is taken for approximately 200 000 samples. The histograms are plotted for each of them and statistical parameters are computed with probability density function fitting. The following results are related to channel 2 of the TDC. The histogram of the measured time interval t_1 is plotted in Fig. 7.8. You can see the mean value and the sigma of the measured data in Fig. 7.8.

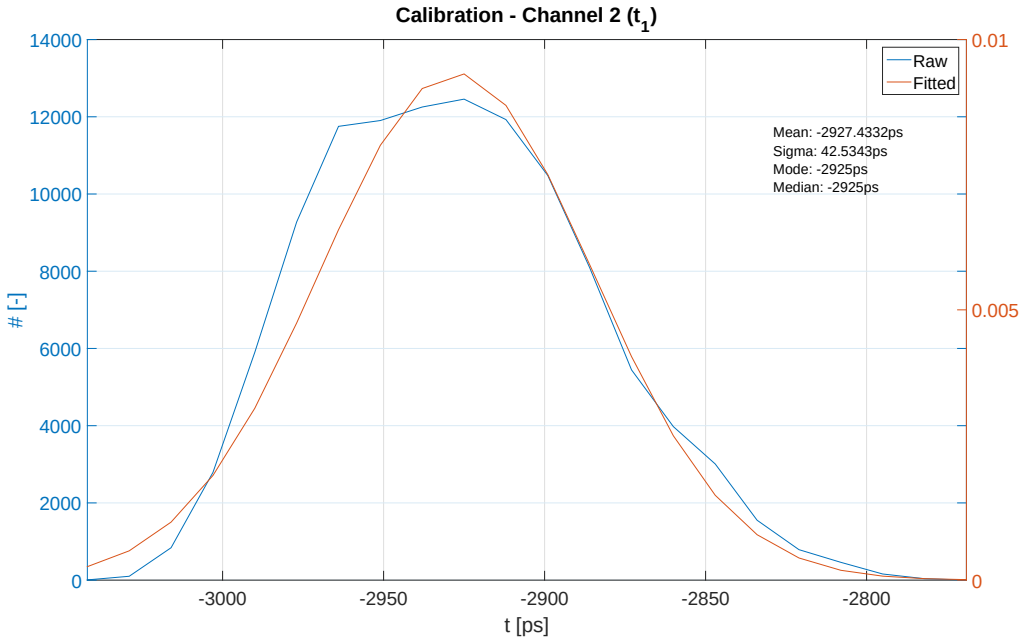


Figure 7.8: Time interval t_1

The measurement of time interval t_2 is shown in Fig. 7.9. The statistical data (mean value, sigma, mode, median) is also seen in the histogram.

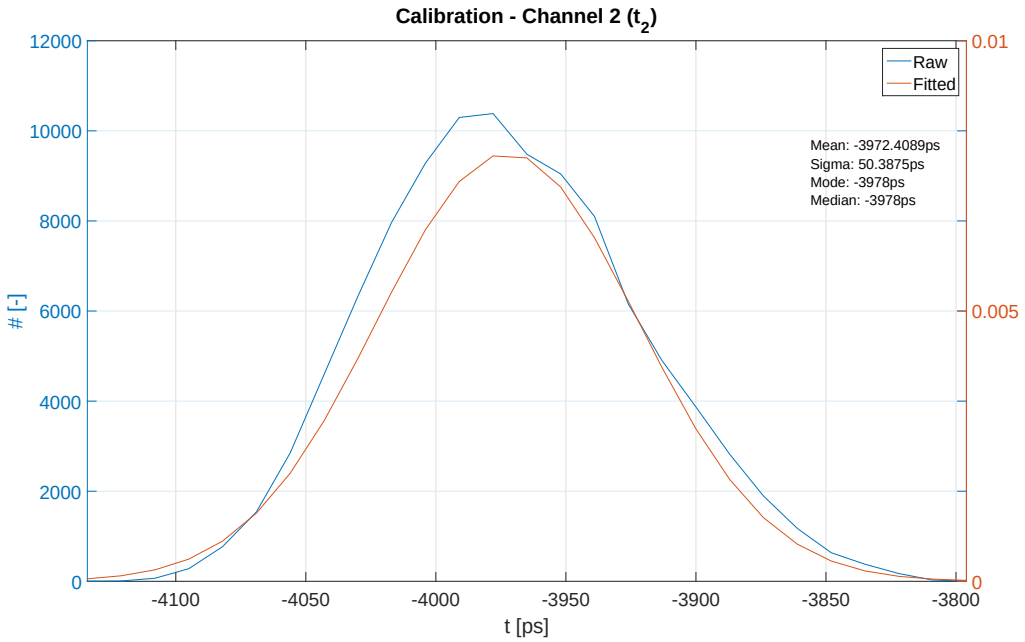


Figure 7.9: Time interval t_2

The last measured interval t_3 according to the formulas is plotted in Fig. 7.10.

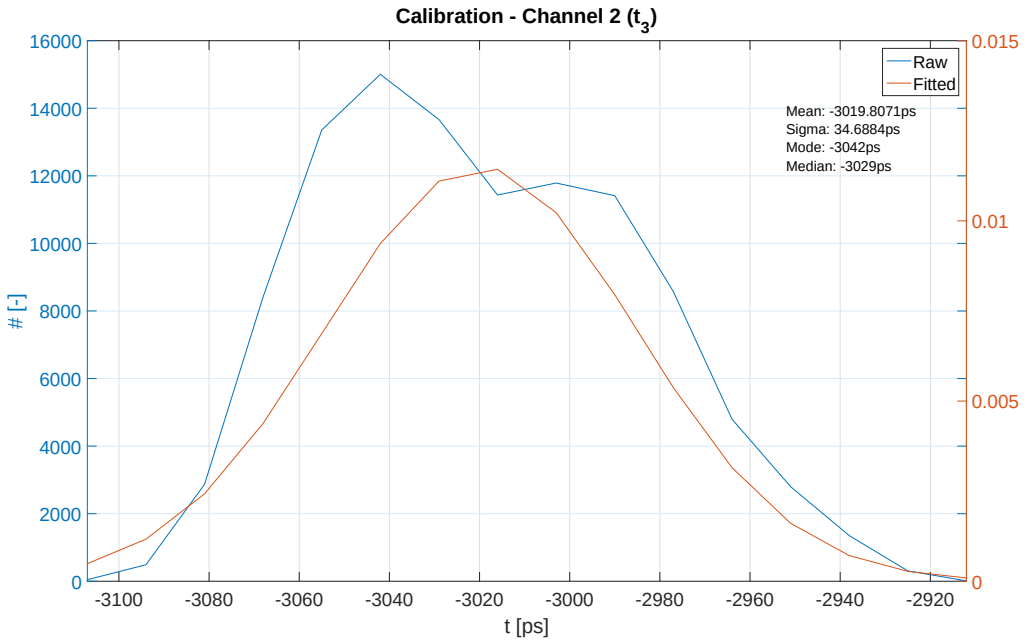


Figure 7.10: Time interval t_3

The calibrataion statistics of channel 2 are in Tab. 7.5 The table includes calculated offset according to formula 7.8 for mean value, mode and median.

Table 7.5: Calibration of channel 2

Value	t_1[ps]	t_2[ps]	t_3[ps]	Offset (o_2) [ps]
Mean	-2927.4332	-3972.4089	-3019.8071	-1974.8314
Mode	-2925	-3978	-3042	-1989
Median	-2925	-3978	-3029	-1976

The same calibration technique is applied for the rest of the channels. The results are shown in Tab. 7.6. Only mean values are mentioned in the table.

Table 7.6: Calibration of TDC

Channel (Mean)	t_1[ps]	t_2[ps]	t_3[ps]	Offset [ps]
Channel 1	-2934.6101	-3983.5136	-3030.3611	-1981.4576
Channel 2	-2927.4332	-3972.4089	-3019.8071	-1974.8314
Channel 3	-2811.1843	-3859.3037	-2907.2662	-1859.1468
Channel 4	-2743.9406	-3792.7918	-2838.5295	-1789.6783

Tab. 7.6 shows calibration data which has to be applied on the measured data in order to compensate for the error caused by the return channel. The calibration can be done offline or online. The offline calibration is performed on stored data. The online calibration is done using a control application (User version - mentioned in Subsection 5.4.2) in the tab named calibration. Then the stored data is already compensated for the offset and the current showed data are compensated in the software too.

A calibration is necessary for each TDC device. It is done for each device and the calibration data is compared. The next figure shows the histogram of time interval t_1 measured by channel 2 of another TDC.

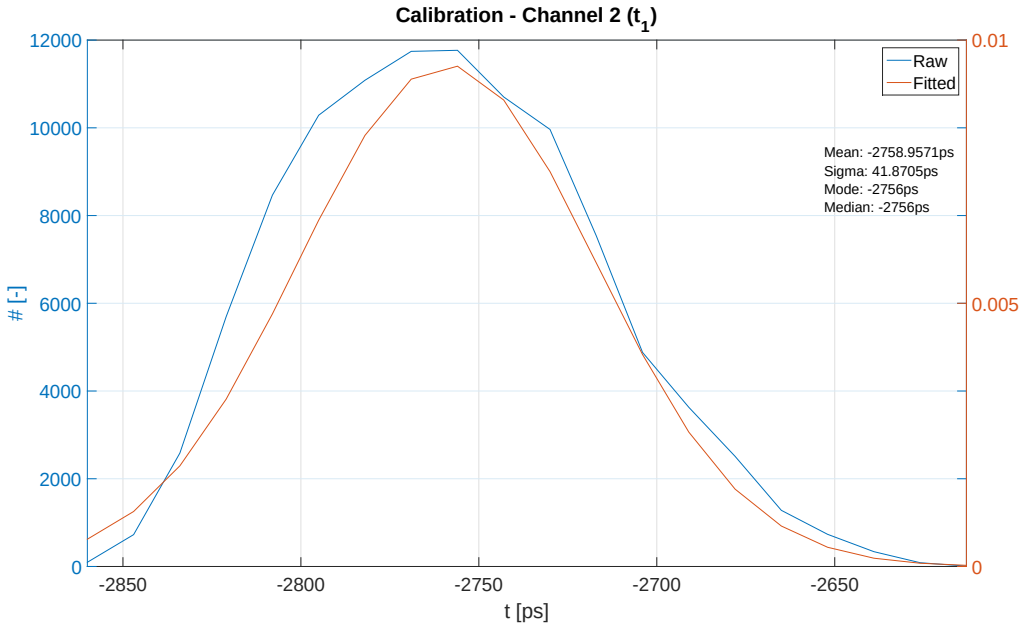


Figure 7.11: Time interval t_1

The time interval t_2 during the calibration of another TDC is in Fig. 7.12. The figure

contains the statistical data as well. The histogram of time interval t_3 is in Fig. 7.13.

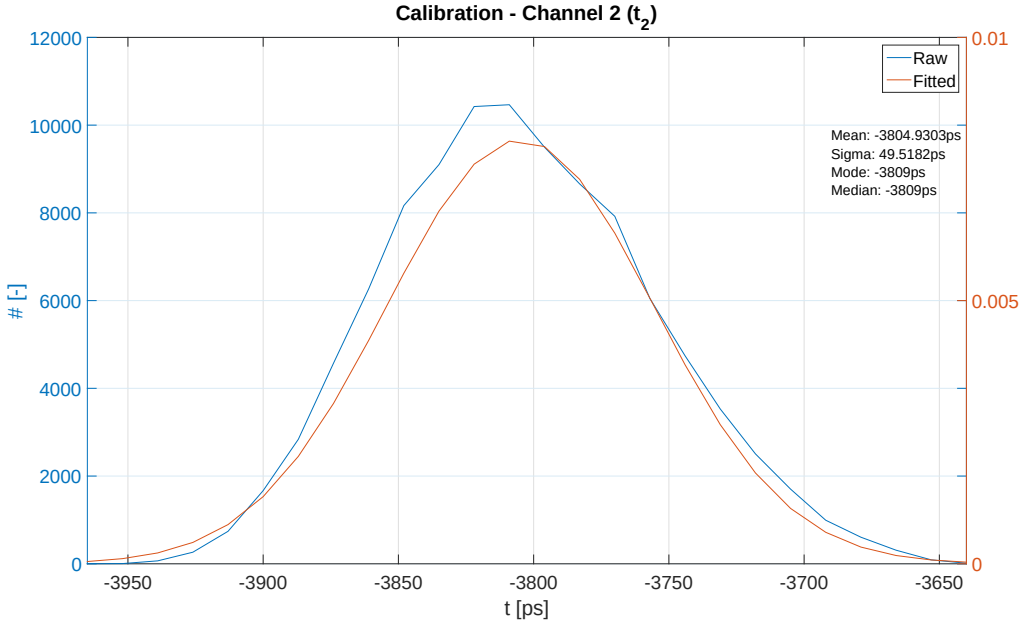


Figure 7.12: Time interval t_2

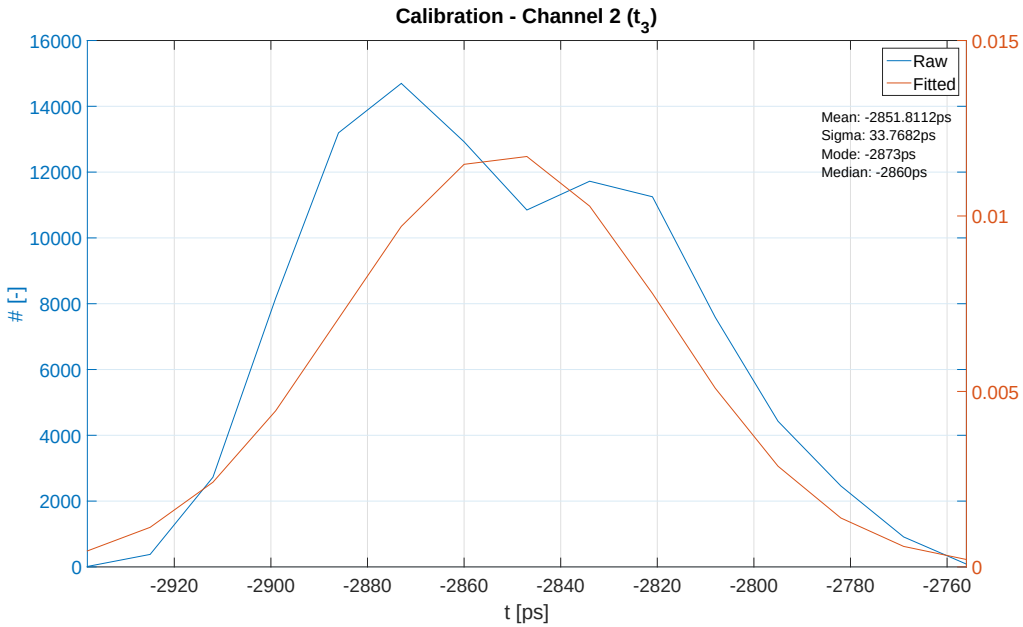


Figure 7.13: Time interval t_3

The processed data is shown in Tab. 7.7. There is calibration data for each channel of second TDC. From the comparison among channels and TDCs, you can see the differences which are caused by input drivers of the TDC device. The rest of the hardware (PCB, connectors, etc.) is the same. The only difference is the aforementioned input LVDS drivers which are common for two channels, also seen from the results. The difference between the calibration offset of channel 1 and channel 2 or channel 3 and channel 4 is less than

the difference between channel 1 and channels 3, 4 or channel 2 and channels 3, 4.

Table 7.7: Calibration of second TDC

Channel (Mean)	t_1[ps]	t_2[ps]	t_3[ps]	Offset [ps]
Channel 1	-2793.5062	-3840.5572	-2886.8227	-1839.7717
Channel 2	-2758.9571	-3804.9303	-2851.8112	-1805.8380
Channel 3	-2815.4269	-3863.1199	-2911.2033	-1863.5103
Channel 4	-2753.8571	-3801.2014	-2847.8682	-1800.5239

The differences in offsets of TDCs include propagation delays of LVDS drivers and an input clock buffer (return channel chip), which can vary. According to the calibration measurement of one TDC the variation can be up to 200ps. As already mentioned, the LVDS driver contains two channels. The channel-to-channel skew is 50ps in its typical value, it corresponds to the offset values. The switching parameters for the LVDS driver are in Tab. 7.8 for comparison with the calibration results.

Table 7.8: Switching parameters of LVDS driver

Parameter	*Typical (Maximal) value [ns]*
Propagation delay	1.3 (2)
Channel-to-channel skew	0.05 (0.5)
Part-to-part skew	- (1)

7.2.2 Linearity

The integral non-linearity (INL) of the TDC was measured. The generator DG535 from the SRS company is used for the INL measurement. The generator can delay the outputs with multiples of 5ps, as mentioned in Tab. 7.4. The output is delayed step by step by 5ps (T_0 - start, T_A - stop) and the delay is measured with a TDC. The same measurement was made repeatedly. The measurement setup is in Fig. 7.14.

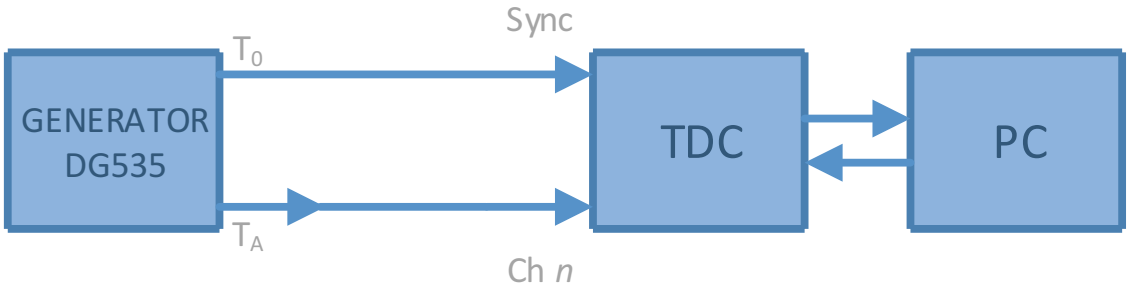


Figure 7.14: INL measurement setup

The results are plotted in Fig. 7.15 for channel 1 of the TDC. The measured data is in Tab. 7.9. There are four rows (3 measurements + average). Mean values from raw measured data are calculated. The data is focused on a relative shift between the start signal and shifted signal. The shift does not begin from zero because the first measurement starts at 5ps (error of the generator between channels).

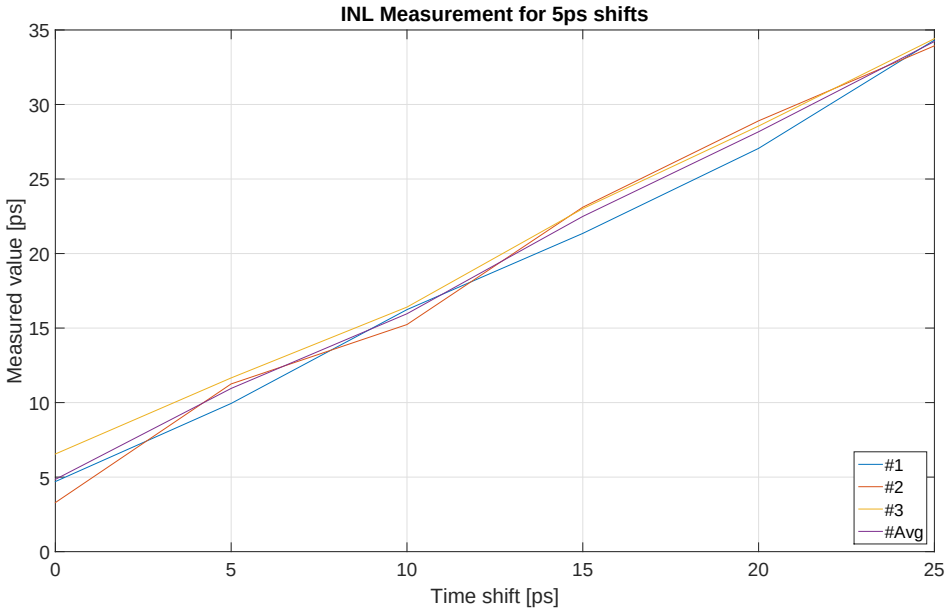


Figure 7.15: INL measurement for 5ps shifts

Table 7.9: INL measurement for 5ps shifts

Measurement	*1*	*2*	*3*	*4*	*5*	*6*
1 [ps]	4.7013	9.9436	16.2375	21.3511	27.0563	34.322
2 [ps]	3.2906	11.2529	15.2366	23.1081	28.9034	33.953
3 [ps]	6.5521	11.6559	16.4077	23.0102	28.5542	34.4151
Average [ps]	4.848	10.9508	15.9606	22.4898	28.1713	34.23003

From the data, the shifting of mean value is seen according to the generator settings. Moreover the first measurement is shown in histograms in Fig. 7.16.

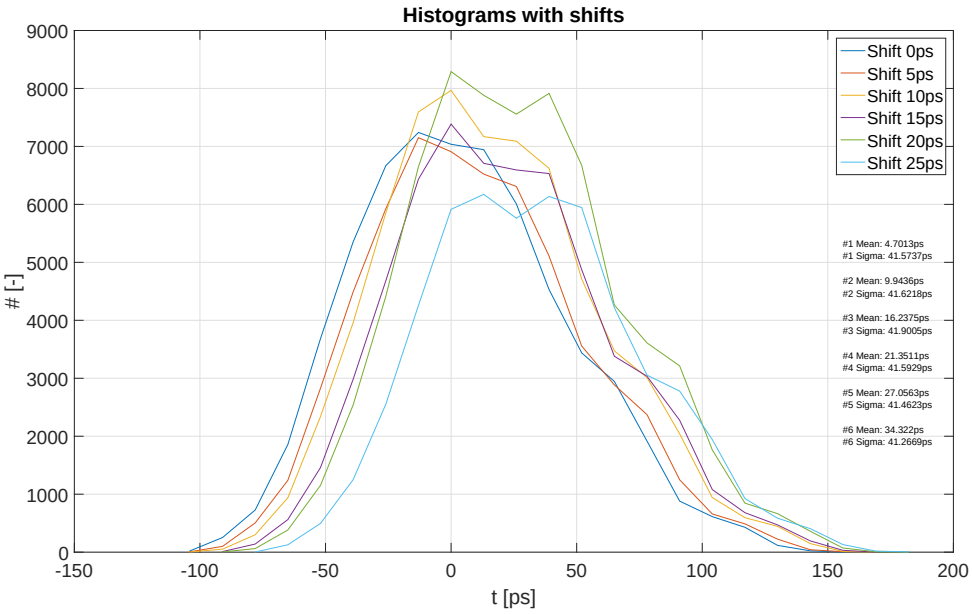


Figure 7.16: INL measurements - Histograms

You can see the shift of each histogram according to the 5ps shift showed in the legend. The figure also contains the sigma value of each measurement.

In addition, the measurement was made for delays of LSB multiples of the TDC resolution. It means delays of 65ps, 130ps, etc. In this measurement, the mean value, mode value and median value is shown in Tab. 7.10 and the data is plotted in Fig. 7.17.

Table 7.10: INL measurement for 65ps shifts

Shift [ps]	*0*	*65*	*130*	*195*	*260*
Mean	-2934.6	-2867.21	-2779.73	-2708.25	-2632.5
Mode	-2964	-2873	-2808	-2730	-2652
Median	-2938	-2873	-2782	-2717	-2639

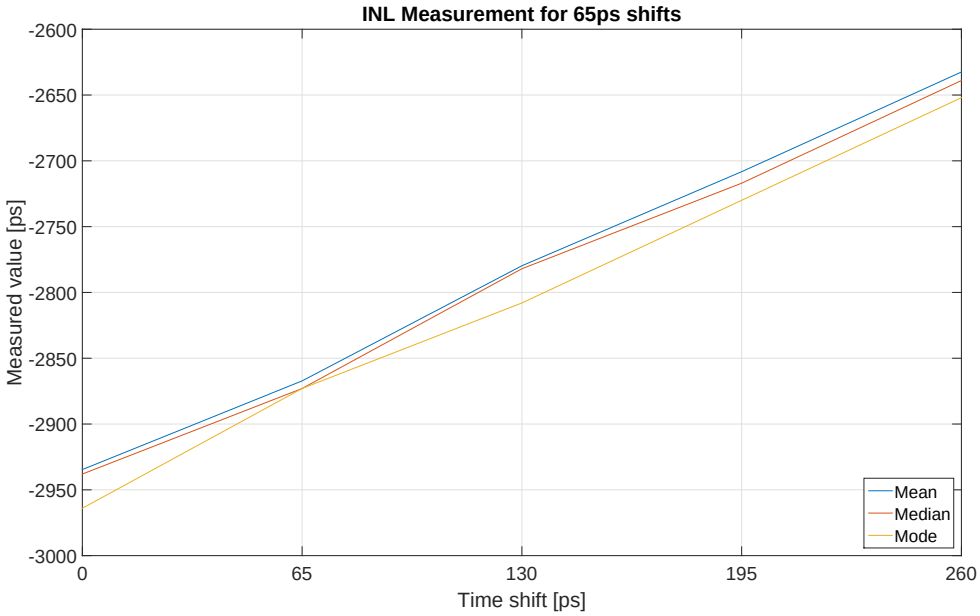


Figure 7.17: INL measurement for 65ps shifts

The values correspond to the delayed output of the generator. If the parameters of the generator are taken into account (jitter, etc.), the measured delay is at an error of a maximal value of one LSB. The measured trend of the curve is linear but the increment does not exactly correspond to the 5ps increment of the generator. It is a question if the real increment of the generator is 5ps or less. If it is, the real TDC resolution would probably be less.

7.2.3 Examples of measurement

The characterization of the TDC described above is an important thing which is necessary to know before the start of the measurement. The TDC can be used in several standalone applications. One of them was already mentioned in the measurement with TDC based on USB2.0 communication, a pulse width measurement. Another one is the propagation delay measurement of a transmission line, which uses the return channel.

Pulse width measurement

The pulse width measurement is based on the measurement between the rising edge and the falling edge of the signal or vice versa. In order to measure that, the signal has to be split into two signals. There are two approaches, an external splitter, such as the configuration in Fig. 7.1 or by using the return channel of the TDC. The first approach requires to using cables with the same length or cables of a known length (propagation delay). The second one requires the use of a cable with the known propagation delay due to the post-correction of the measured pulse width. The histogram of the pulse width generated from the DG535 generator with a generated 10ns wide pulse is in Fig. 7.18.

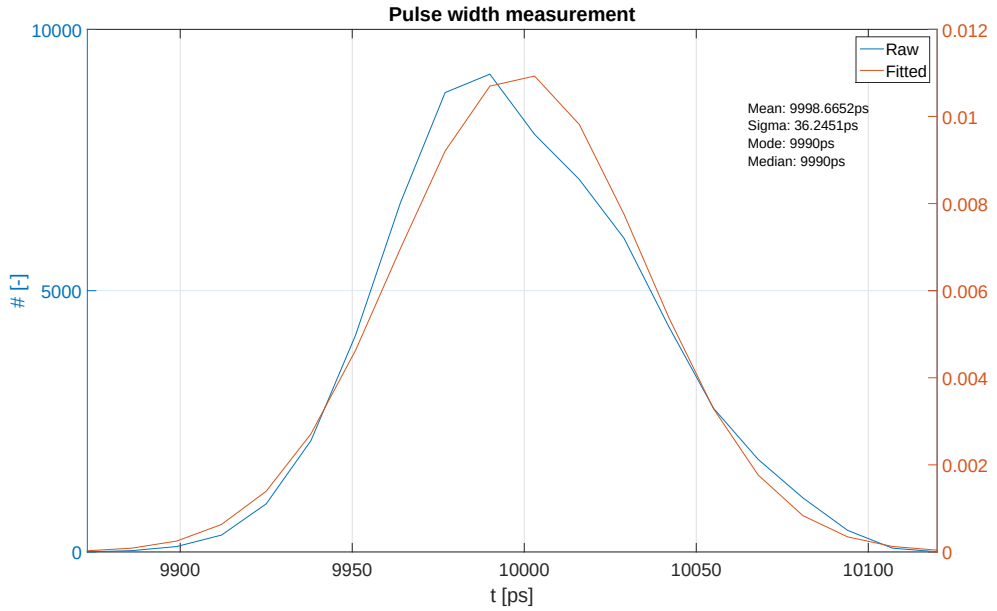


Figure 7.18: Histogram of the measured 10ns wide pulse

Propagation delay of a transmission line measurement

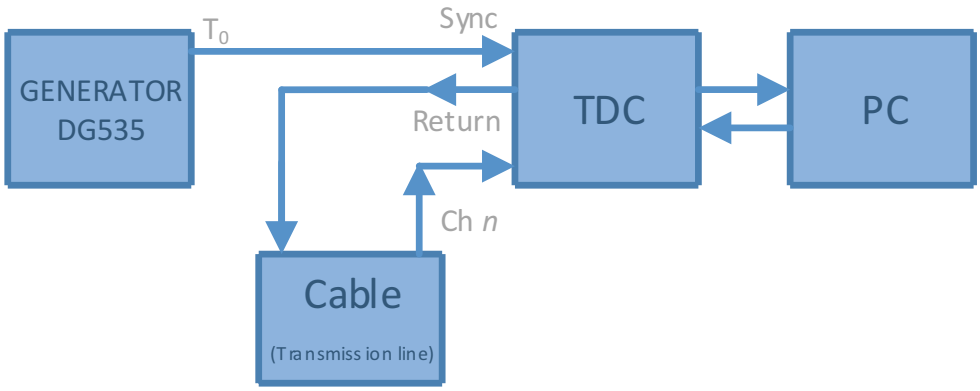


Figure 7.19: Setup for propagation delay measurement

The next advantage resulting from the return channel is the capability for the measurement of the propagation delay of a transmission line inserted between the return channel and

the input channel. The signal from the generator is fed only through the sync input of the TDC. The feature can be useful for a length characterization of unknown cables. The setup is in Fig. 7.19. The following figures show histograms for three cables of different lengths (approximately 0.5, 1.5m and 30m). The measured delay of the 30m long cable (Fig. 7.22) is 120ns which results in a velocity of propagation of 83% of the speed of light. According to the datasheet, the velocity of propagation is 84%.

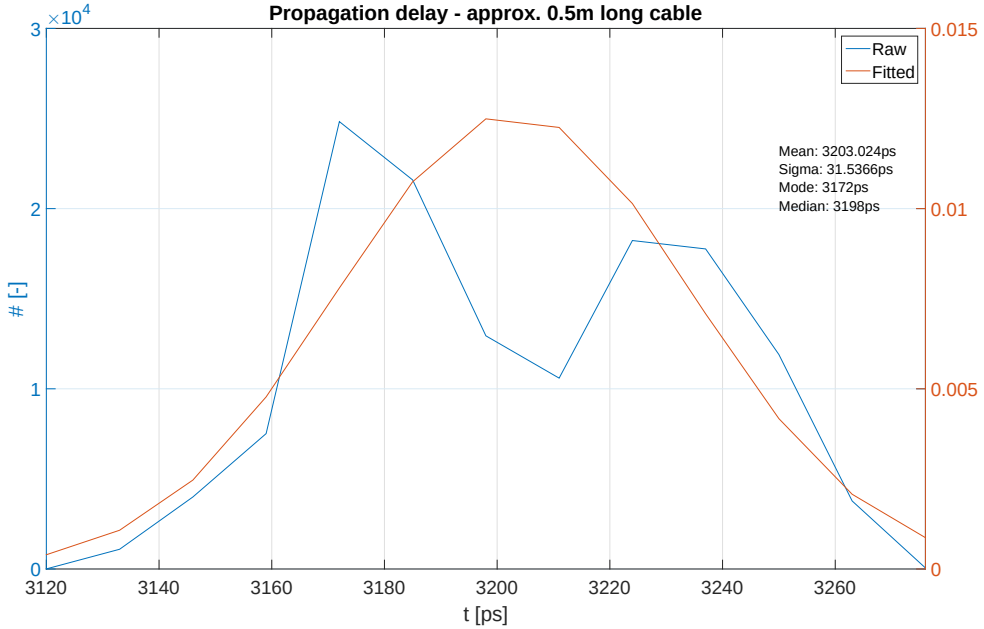


Figure 7.20: Propagation delay - approx. 0.5m long cable

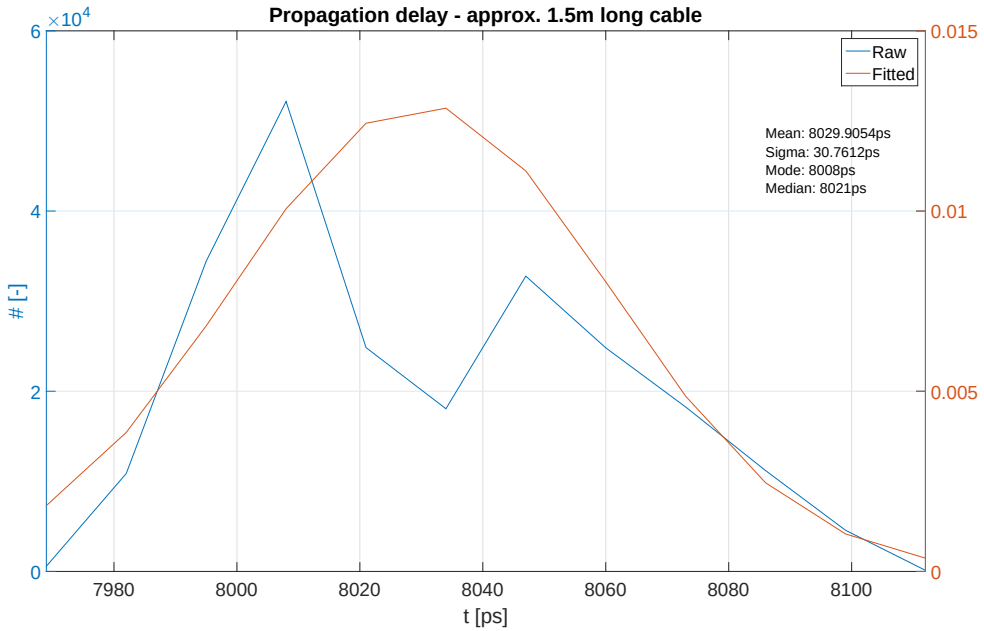


Figure 7.21: Propagation delay - approx. 1.5m long cable

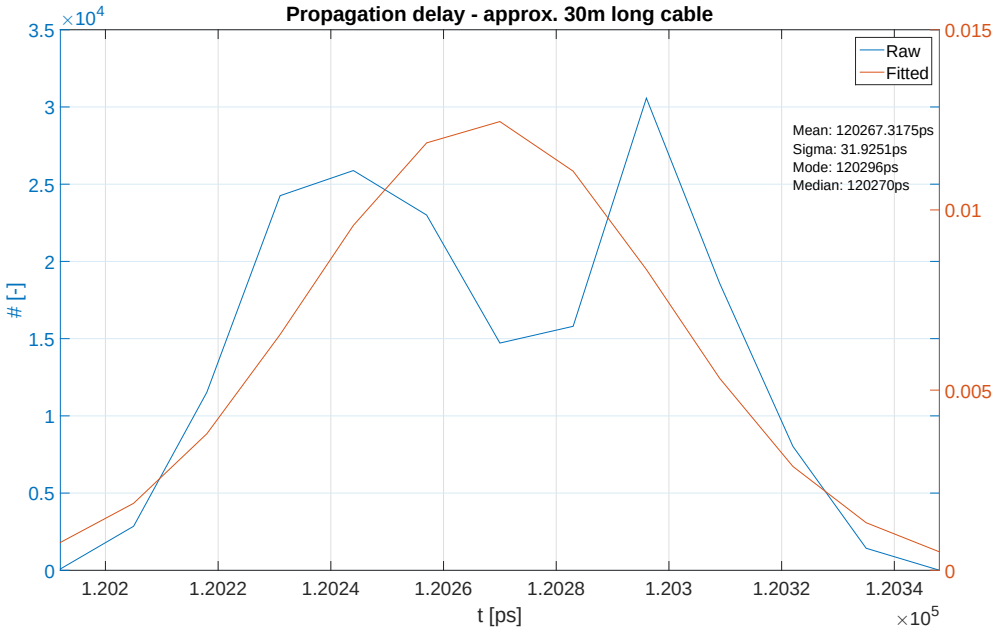


Figure 7.22: Propagation delay - approx. 30m long cable

You can see the drop in the histograms. The drop was probably caused by a measurement configuration which is the measurement between the rising edge and the rising edge of the same signal (only delayed). Other configurations did not cause a drop in the histogram.

Chapter 8

Clock distribution system

The clock distribution system is designed according to the principles mentioned in Chapter 4. The idea of the synchronization in the system is based on measuring the propagation delays of each transmission line (cables, interconnection in nodes, etc.) from the central unit to the nodes. The clock signal is distributed to all nodes, the clock signal is also used for the propagation delay measurement. In other words, the delay is measured at each period of the clock signal (more details in the following section). The next sections describe the designed system and its experimental setup with the corresponding measurements.

8.1 Description of the system

As mentioned, the system measures the propagation delay of each transmission line to all nodes. A system with 2 nodes is shown in Fig. 8.1. Each node includes its own time measurement unit (TDC) as a timestamping device.

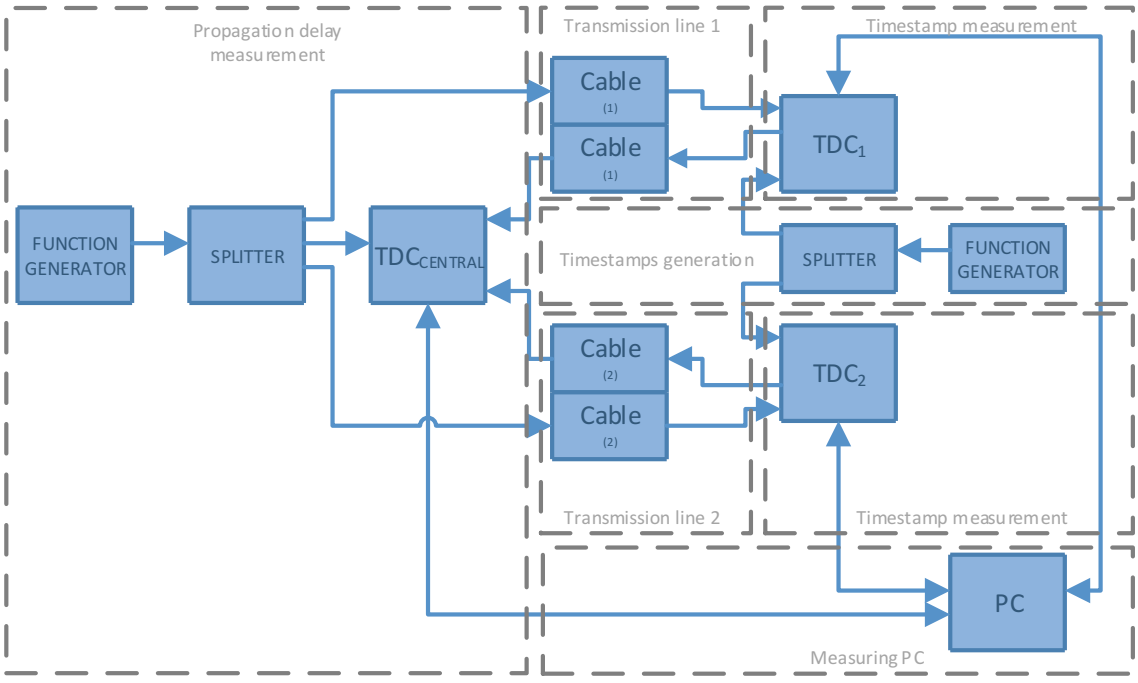


Figure 8.1: Block diagram of the setup with 2 nodes

The propagation delay measurement uses the clock generator in the central unit, which feeds all nodes of the system including the main time measurement unit (in the central unit). The measured propagation delay is used for offline corrections of the timestamps obtained from the nodes. The block diagram consists of parts according to their function. The main time measurement unit ($TDC_{CENTRAL}$) ensures the propagation delay measurement. The interconnection between the central unit and nodes is established from cables, the forward and the backward path to the same node uses identical cables (transmission line 1 or transmission line 2). The local timestamp measurement is made by TDC_1 or TDC_2. For test purposes, the timestamp generation was provided with a function generator and a splitter. The event occurs (Timestamp generation in Fig. 8.1) at the same moment in the TDCs due to the use of the same interconnection between the splitter and TDCs. All TDCs in the setup are connected to the measuring computer via USB. The computer controls all settings of TDCs and it logs the measured data. In principle, additional nodes can be added by adding a transmission line and a corresponding TDC. The general block diagram is in Fig. 8.2. One main time measurement unit can operate up to 4 nodes, but the next 4 nodes can be operated by adding one more TDC as a propagation delay measuring device (grey TDC block in Fig. 8.2). The timestamps are generated as events which are produced by detectors (or other devices that are needed to synchronize), the timestamp measurement is highlighted with a gray dashed line in Fig. 8.2.

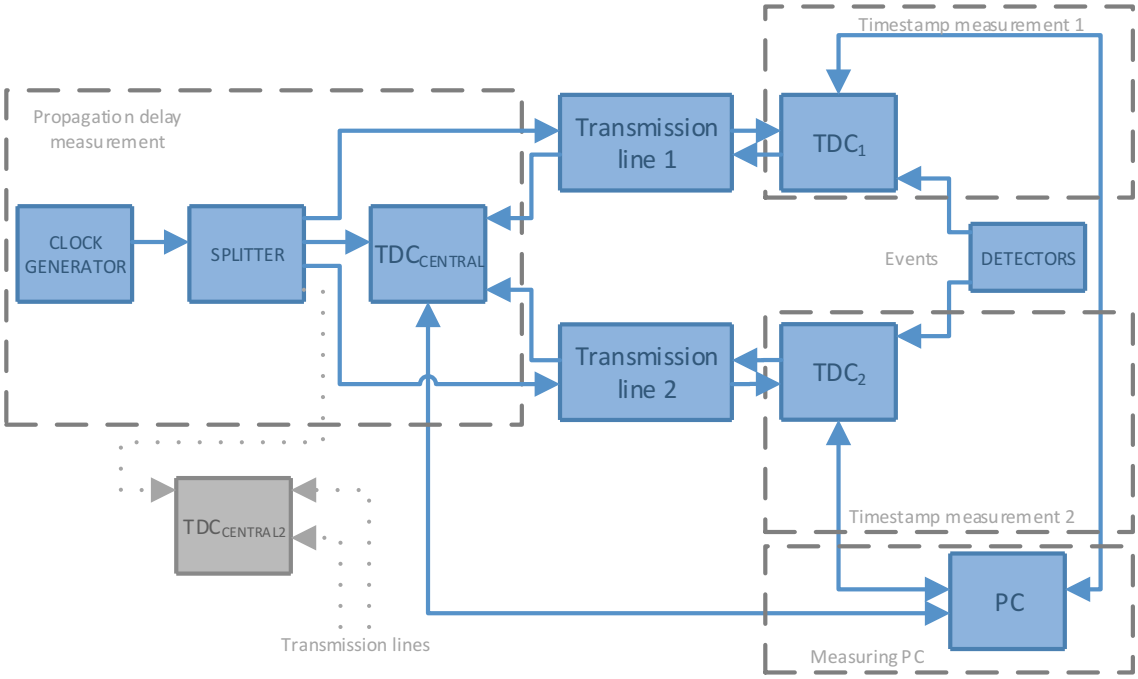


Figure 8.2: General block diagram of the system with synchronization

The period of the clock generator for propagation delay measurement has to be chosen according to the longest transmission line. The period has to be longer than the propagation delay. Otherwise the measured time interval will have a phase difference during one period of the generated signal.

8.2 Correction algorithm

Suppose a system with an asynchronous 200MHz clock in each node, i.e. the system described in the previous chapter which does not have a common clock signal. The central unit and each node in the system have their own clock generator with the same nominal frequency. The oscillator is used as a clock generator. The parameters of the oscillator are in Tab. 8.1.

Table 8.1: Parameters of the oscillator

Parameter	*Value*
Nominal frequency (f)	200MHz
Jitter	<0.9ps
Frequency stability (f_s)	±50ppm
Aging (15years)	±7ppm
Frequency change due to ΔV_{CC}	±3ppm/V

Because of the standalone oscillators, the devices are asynchronous to each other and the frequency used for time measurement can be slightly different. Basically, the time measurement is based on a counting of the periods of the clock signal. The error between timestamps from two TDC devices linearly increases according to the frequency difference. In general, the bigger the difference, the bigger the error. The maximal error can be computed for a period of 1s. The error in the frequency (Δf) is computed from the parameters of the oscillator.

$$\triangle f = \pm \frac{f}{10^6} \cdot f_s \tag{8.1}$$

Now, the values are put into the formula.

$$\triangle f = \pm \frac{200 \cdot 10^6}{10^6} \cdot 50 \tag{8.2}$$

$$\triangle f = \pm 10kHz \tag{8.3}$$

The maximal frequency (f_1) and the minimal frequency (f_2) is obtained.

$$f_1 = f + \triangle f \tag{8.4}$$

$$f_1 = 200.01 \cdot 10^6 Hz \tag{8.5}$$

$$f_2 = f - \triangle f \tag{8.6}$$

$$f_2 = 199.99 \cdot 10^6 Hz \tag{8.7}$$

The count of clock signal periods of the first TDC is

$$N_1 = \frac{1}{T_1} \tag{8.8}$$

where T_1 is

$$T_1 = \frac{1}{\frac{f_1}{x}} \tag{8.9}$$

and f_1 is the frequency of the oscillator and x is the multiplication factor for TDC resolution.

$$N_1 = \frac{f_1}{x} \tag{8.10}$$

The same approach is applied for the second TDC.

$$N_2 = \frac{f_2}{x} \tag{8.11}$$

For the TDC with a 13ps resolution, the x factor is computed as follows.

$$x = f \cdot T_{LSB} \tag{8.12}$$

$$x = 200 \cdot 10^{60} \cdot 13 \cdot 10^{-12} = 2.6 \cdot 10^{-3} \tag{8.13}$$

The error is calculated with the following formula.

$$\triangle t = t_1 - t_2 \tag{8.14}$$

$$\triangle t = T_{LSB} \cdot N_1 - T_{LSB} \cdot N_2 = T_{LSB} \cdot (N_1 - N_2) = T_{LSB} \cdot \left(\frac{f_1}{x} - \frac{f_2}{x} \right) \tag{8.15}$$

$$\triangle t = T_{LSB} \cdot \left(\frac{f_1}{x} - \frac{f_2}{x} \right) = \frac{T_{LSB}}{x} \cdot (f_1 - f_2) \tag{8.16}$$

$$\triangle t = \frac{T_{LSB}}{f \cdot T_{LSB}} \cdot (f_1 - f_2) = \frac{1}{f} \cdot (f_1 - f_2) \tag{8.17}$$

$$\triangle t = \frac{1}{200 \cdot 10^6} \cdot \left(200.01 \cdot 10^6 - 199.99 \cdot 10^6 \right) = 1 \cdot 10^{-4} s = 100 \mu s \tag{8.18}$$

The maximal error in the time measurement between 2 TDCs is 100μs during a 1s measurement. The maximal error for the whole measurement range of the TDC used is calculated with the following equation.

$$\triangle t_{max} = \triangle t \cdot 2^{N-1} \cdot T_{LSB} \tag{8.19}$$

$$\triangle t_{max} = 1 \cdot 10^{-4} \cdot 2^{40-1} \cdot 13 \cdot 10^{-12} = 7.14682558 \cdot 10^{-4} s \tag{8.20}$$

The maximal error during the whole measurement can be up to approximately 714µs. The increasing error at its maximum is drawn in Fig. 8.3 in the whole range of the measurement.

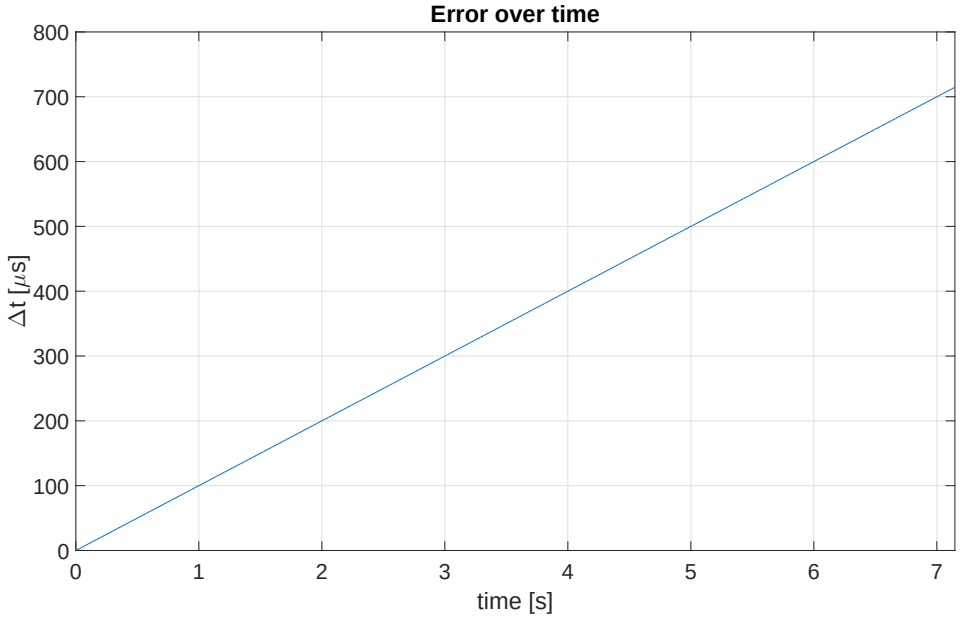


Figure 8.3: Increasing error over time

The error has a linear trend. If the trend is known, it is possible to correct the timestamps in one TDC device in relation with another TDC device. The trend is determined by the ratio of the frequencies of the oscillator in the first TDC and the second TDC. Ratio k is calculated according to the following formula for oscillator frequencies f_1 and f_2.

$$k = \frac{f_2 - f_1}{f_2} \tag{8.21}$$

The problem is how to determine the unknown frequencies. The ratio can be expressed with counts of LSB (N_1 and N_2). Suppose the difference between the timestamps from the TDCs is zero (formula 8.22).

$$\triangle t = t_1 - t_2 = 0 \tag{8.22}$$

$$t_1 = N_1 \cdot T_{LSB} \tag{8.23}$$

$$N_1 \cdot \frac{1}{\frac{f_1}{x}} - N_2 \cdot \frac{1}{\frac{f_2}{x}} = 0 \tag{8.24}$$

$$\frac{N_1}{f_1} = \frac{N_2}{f_2} \tag{8.25}$$

The f_1 is also determined by ratio k (formula 8.21).

$$f_1 = f_2 - k \cdot f_2 \tag{8.26}$$

Formula 8.26 is put into formula 8.25.

$$\frac{N_1}{f_2 - k \cdot f_2} = \frac{N_2}{f_2} \tag{8.27}$$

$$N_1 = N_2 \cdot (1 - k) \tag{8.28}$$

$$k = \frac{N_2 - N_1}{N_2} \tag{8.29}$$

Formula 8.23 is put into formula 8.29.

$$k = \frac{t_2 - t_1}{t_2} \tag{8.30}$$

Ratio k ratio can be determined by timestamps t_1 and t_2. In that case, a setup with zero difference has to be established. It is possible with the same cables used in the interconnection of the system. The setup is used for a calibration which is necessary for synchronization. The k ratio is calculated according to formula 8.30. After the calculation of the k ratio, the timestamps can be corrected. The following formula is applied for the correction.

$$t_1 = t_1 - k \cdot t_1 \tag{8.31}$$

The next figure shows a block diagram of the calibration setup. The nodes are connected via the same cables as mentioned before. The start and stop signals are generated using two independent function generators.

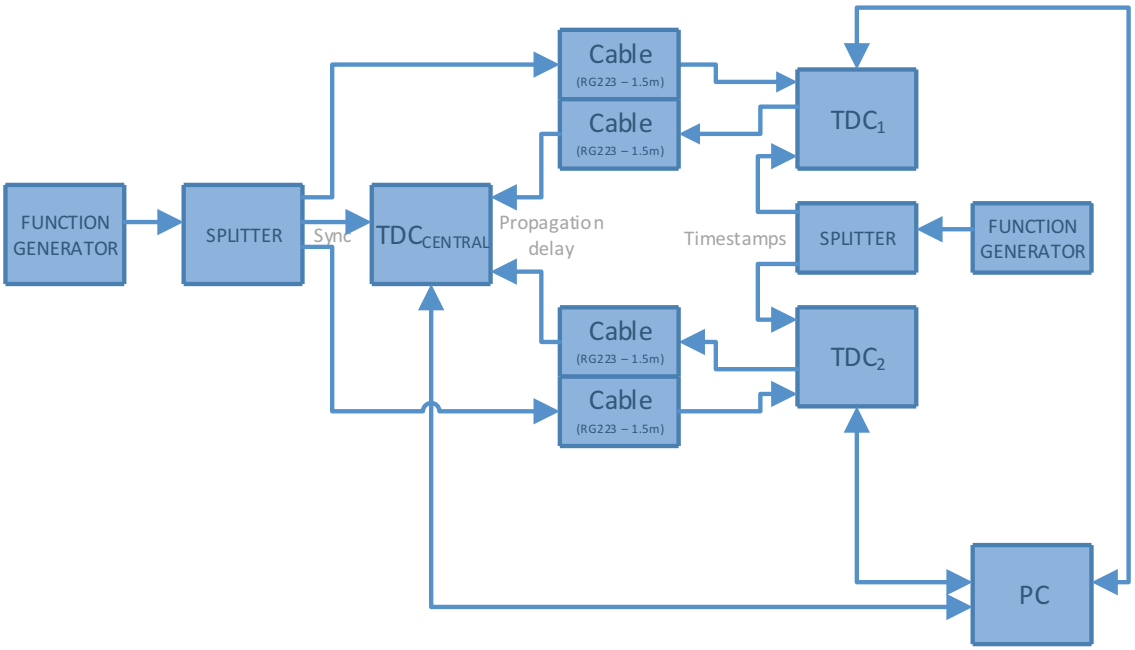


Figure 8.4: Calibration setup

A photo of the calibration setup is in Fig. 8.5. The main part are highlighted in the

photo as TDCs, generators and splitter.

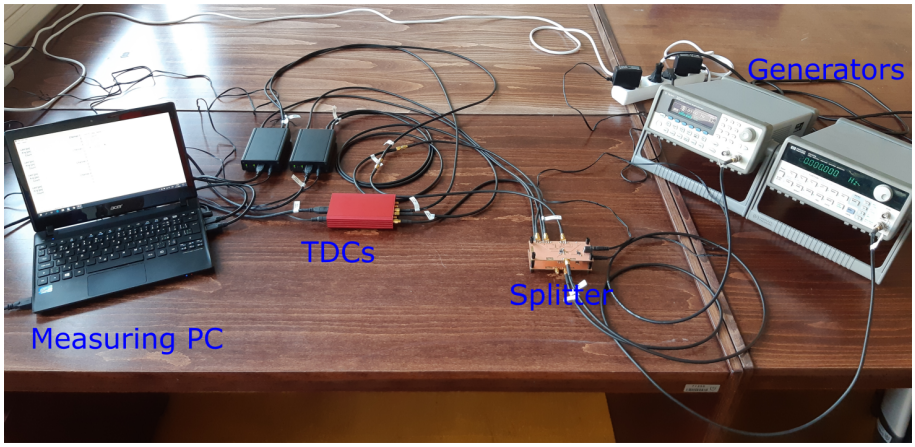


Figure 8.5: Photo of the calibration setup

The calibration measurements were made for three different settings (different frequencies of the timestamp generator - stop signal for TDC), specifically for 20Hz, 25Hz and 30Hz. The results are plotted as a density function (histogram) in the following figures.

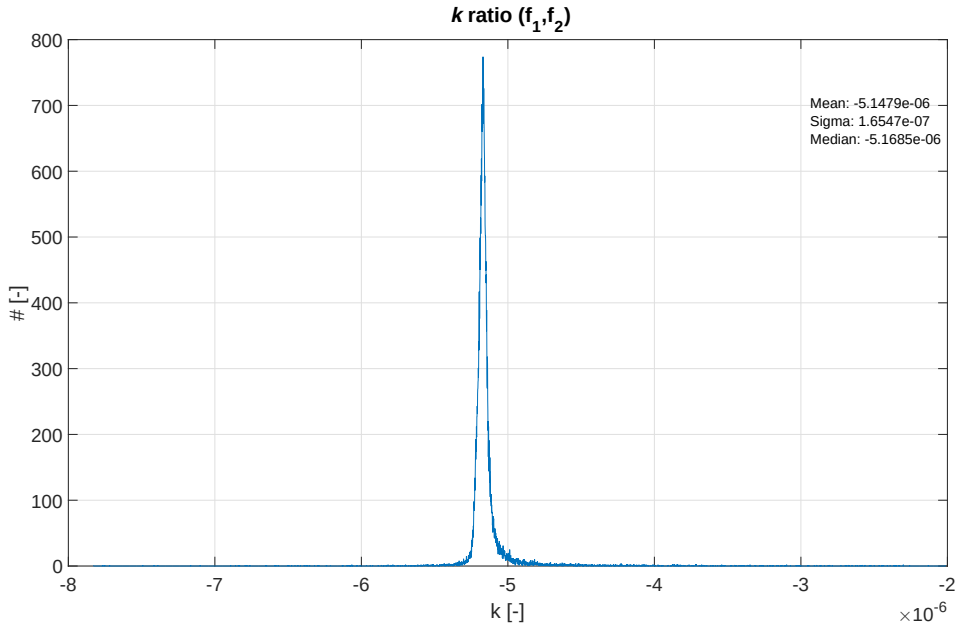


Figure 8.6: k ratio - timestamp generation at 20Hz

The mean values are also in Tab. 8.2. The error is seen from the results. The difference in timestamps from two TDC devices can be up to approximately 5μs in 1s of measurement. It means, the error of the LSB of TDC is approximately 67as.

Table 8.2: k ratio

Frequency of timestamp generation	*20Hz*	25Hz	30Hz
k (mean)	$-5.1479.10^{-6}$	$-5.1174.10^{-6}$	$-5.127.10^{-6}$
k (median)	$-5.1685.10^{-6}$	$-5.1398.10^{-6}$	$-5.1489.10^{-6}$

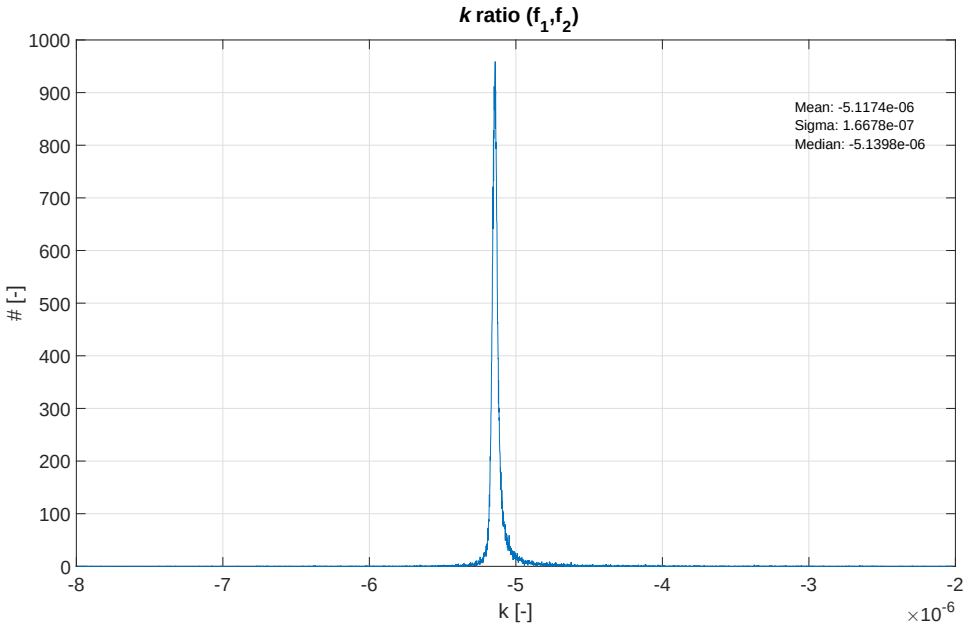


Figure 8.7: k ratio - timestamp generation at 25Hz

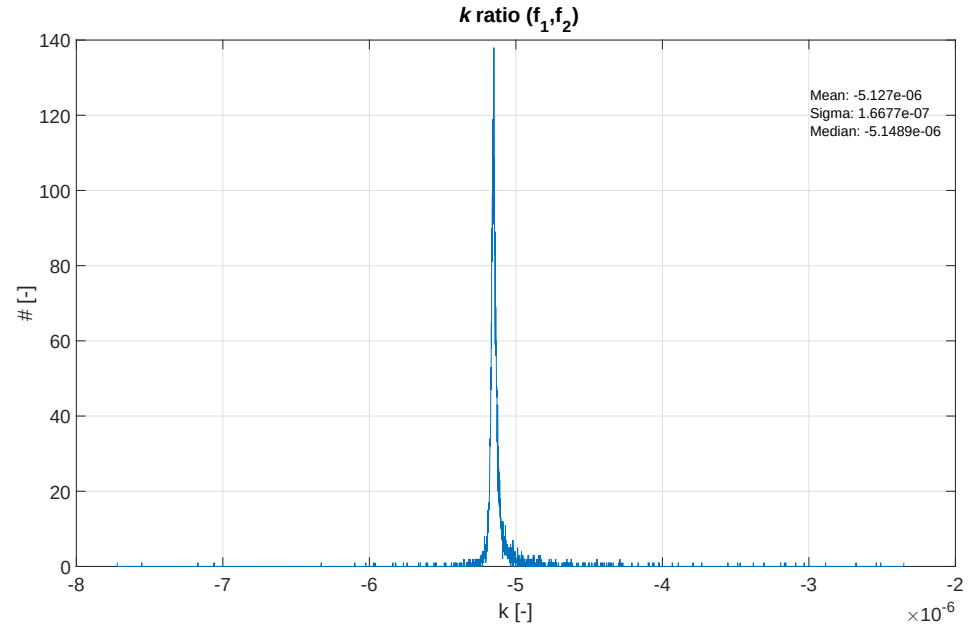


Figure 8.8: k ratio - timestamp generation at 30Hz

The calculated value of ratio k is relevant only for the measured TDC. In the setup with more TDC devices, all TDCs have to be calibrated and one TDC has to be common for all measurements. The oscillator in the common TDC is a reference for the other TDCs and all timestamps are corrected with this reference.

8.3 Measurements

8.3.1 Setup with the same transmission lines to nodes

This setup is similar to the calibration setup which is shown in Fig. 8.4. The difference in timestamps from both nodes should be zero in this setup. As the first result from the measurement, the difference was computed from raw data, i.e. without the correction algorithm described in the previous part, however the propagation delay correction is included. Fig. 8.9 shows the histogram of raw data, Fig. 8.10 shows raw data over time.

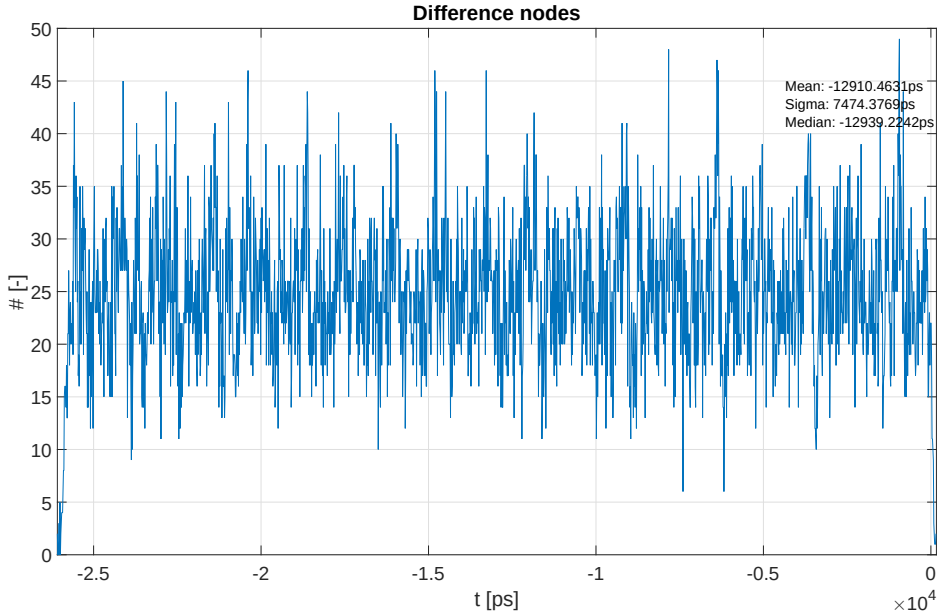


Figure 8.9: Histogram of difference in timestamps without correction

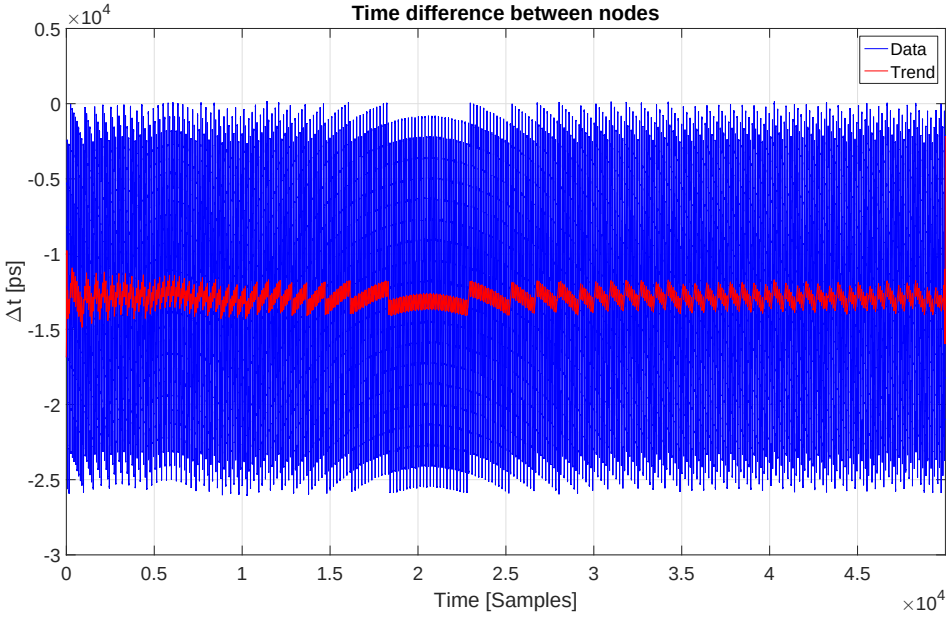


Figure 8.10: Difference in timestamps over time without correction

The need for the correction algorithm is seen from Fig. 8.10. The trend corresponds to Fig. 8.3 (Error in time). As mentioned, the propagation delay correction is included in the results. The propagation delays of transmission lines are plotted in the following histograms (Fig. 8.11 and Fig. 8.12) for cable A (to TDC_1) and cable B (to TDC_2). The difference is less than 30ps according to the measurement of cables used. The sigma of the measurement is approximately 15ps.

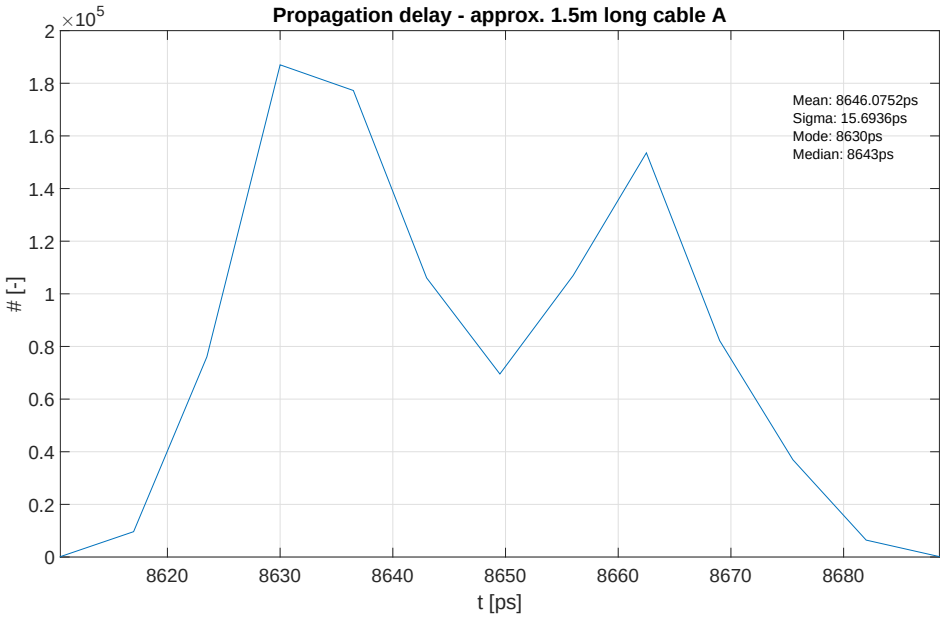


Figure 8.11: Histogram - propagation delay of cable A

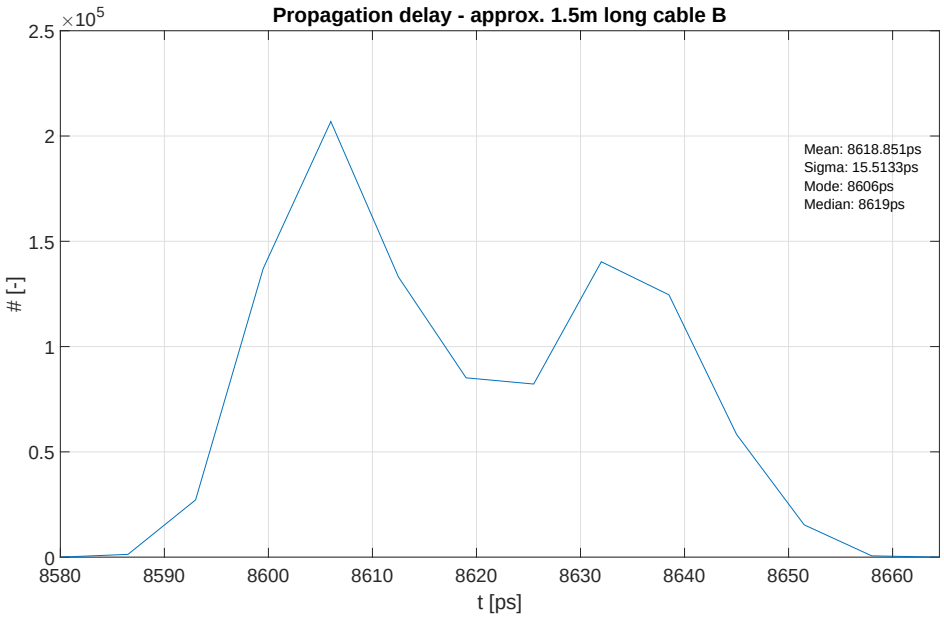


Figure 8.12: Histogram - propagation delay of cable B

The timestamps were generated by the function generator with various frequencies.

Three sets of data were taken for generating frequency of 20Hz, 25Hz and 30Hz. Fig. 8.9 and Fig. 8.10 show the data for a frequency of 20Hz. The following figures show the results for the other two frequencies of the generating timestamps.

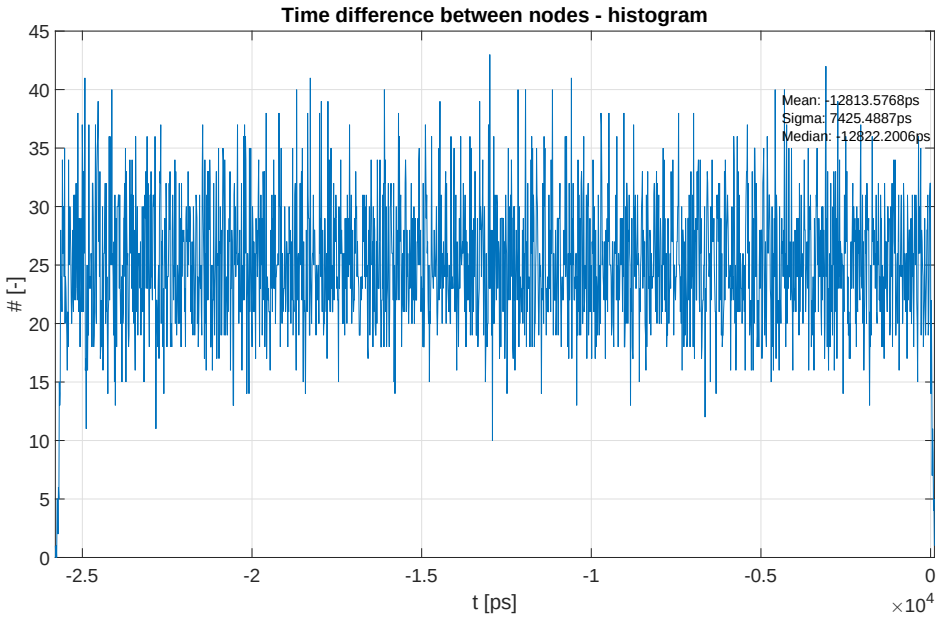


Figure 8.13: Histogram of difference in timestamps without correction (25Hz)

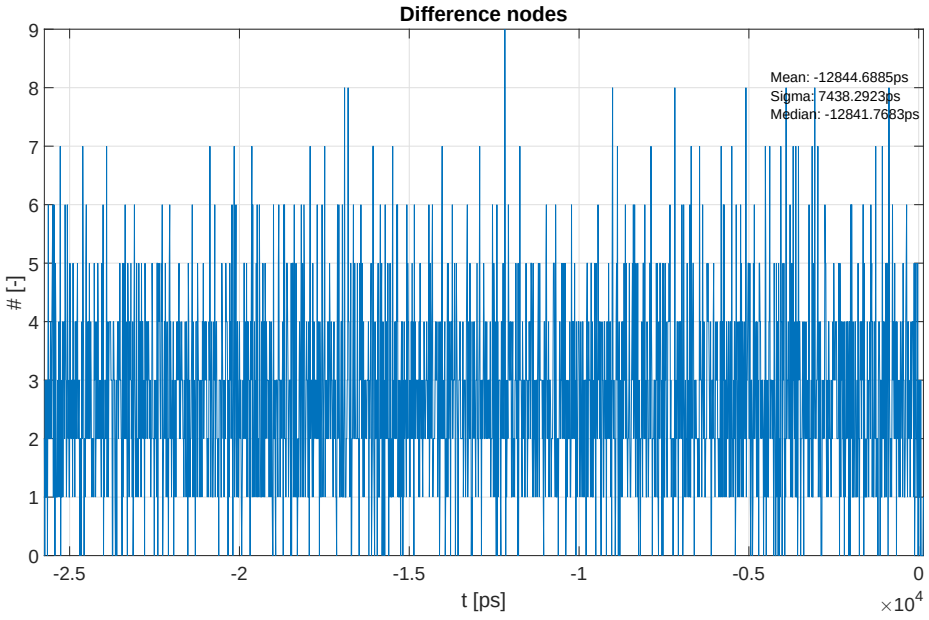


Figure 8.14: Histogram of difference in timestamps without correction (30Hz)

The difference among the histograms for all frequencies of generating timestamps is negligible. The correction algorithm described in the previous part is applied to the results according to the computed k ratio. The histogram of difference in timestamps for the first set of timestamps (20Hz) is plotted in Fig. 8.15. Fig. 8.16 shows the trend of the change

of the difference over time. The measurement after the power up is seen in Fig. 8.16, the measurement is stabilized after a while (a few minutes), when the device and housing are heated themselves.

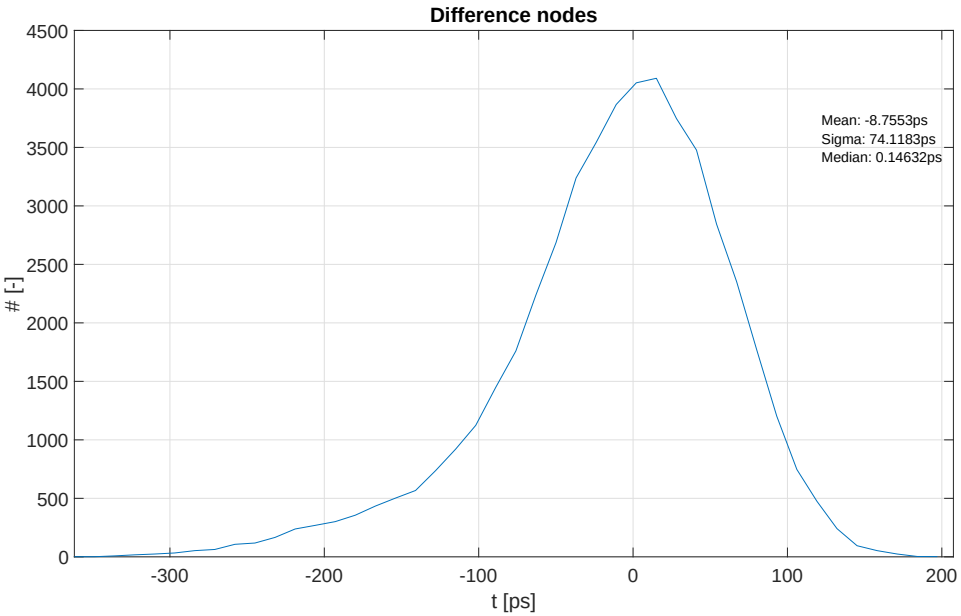


Figure 8.15: Histogram of difference in timestamps with correction

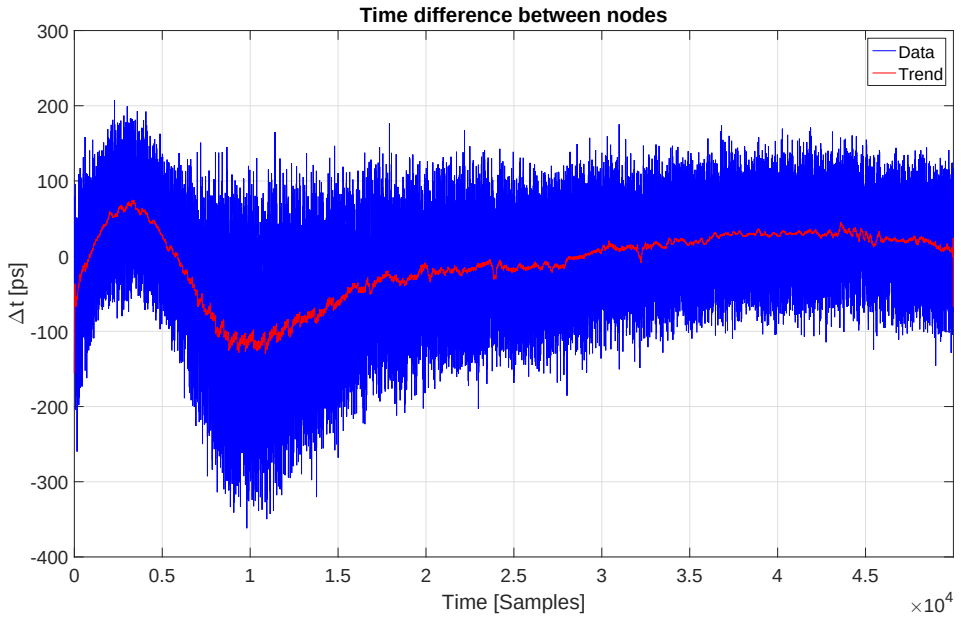


Figure 8.16: Difference in timestamps over time with correction

The other figures show the same results for the other frequencies. The mean value of the time difference are in Tab. 8.3. All values are in the span of one LSB of the TDC device.

Table 8.3: Time differences after correction

Frequency of timestamp generation	*20Hz*	25Hz	30Hz
Mean value [ps]	-8.7553	-1.6801	-0.0668

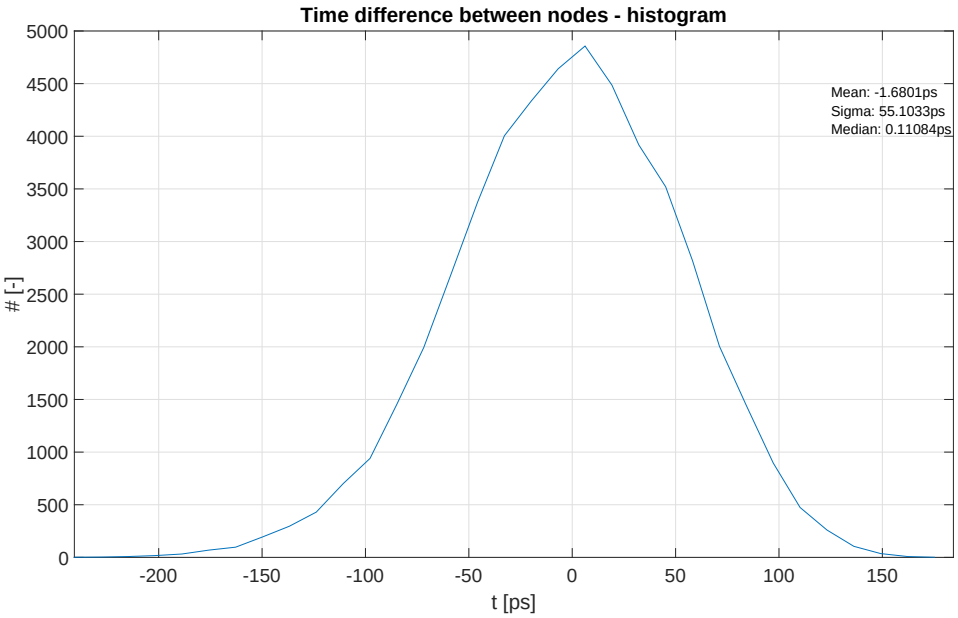


Figure 8.17: Histogram of difference in timestamps with correction (25Hz)

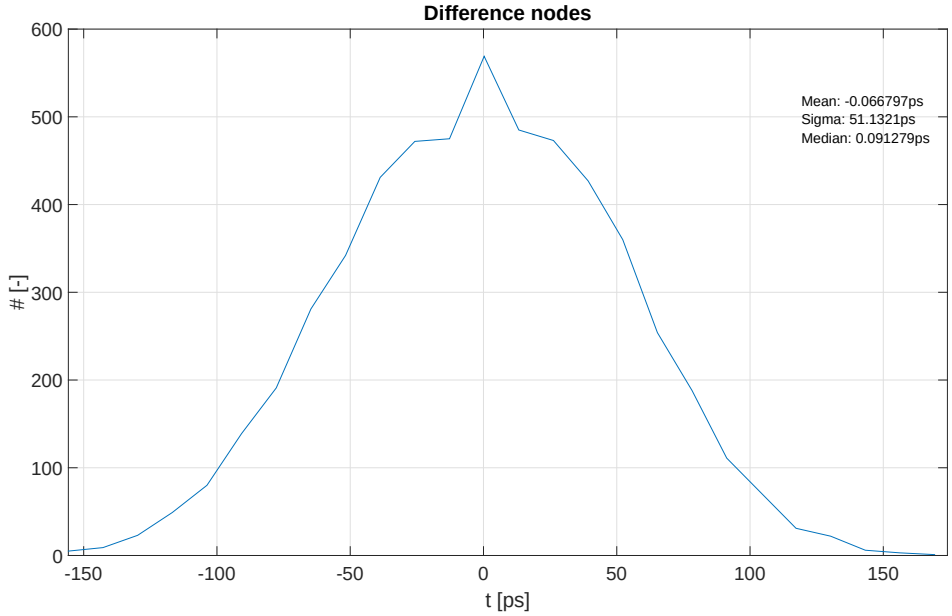


Figure 8.18: Histogram of difference in timestamps with correction (30Hz)

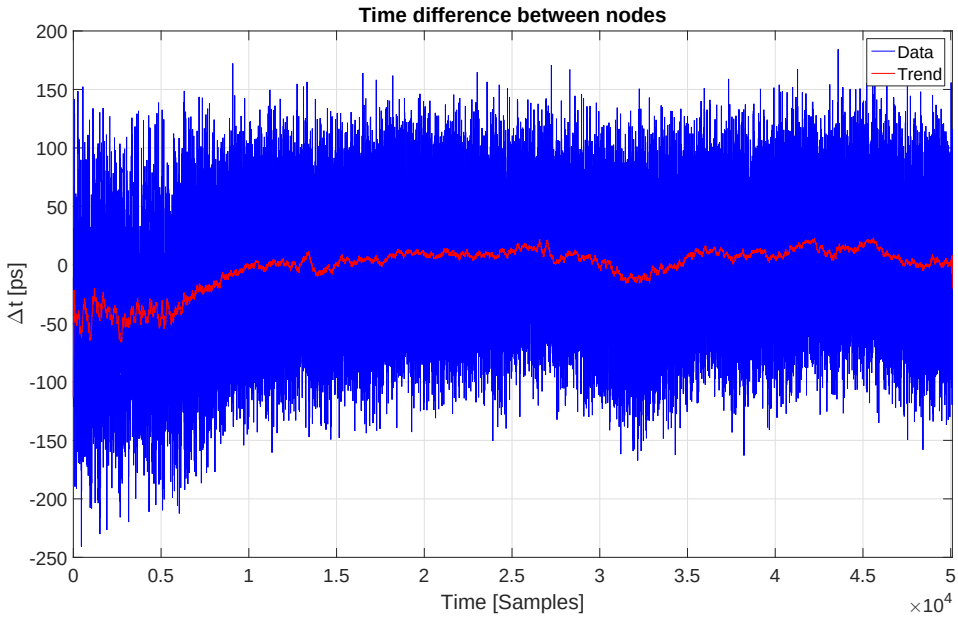


Figure 8.19: Difference in timestamps over time with correction (25Hz)

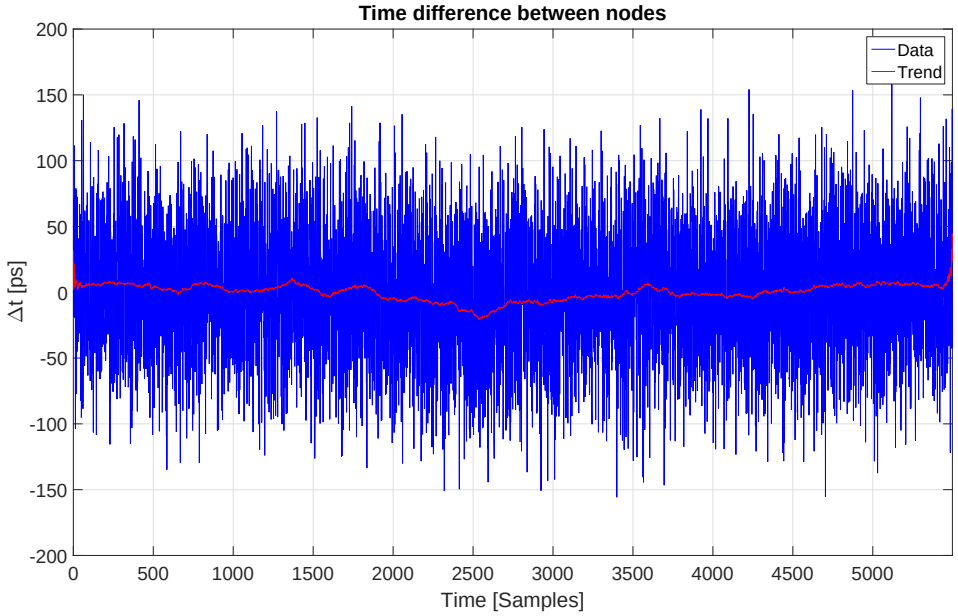


Figure 8.20: Difference in timestamps over time with correction (30Hz)

8.3.2 Setup with the different transmission lines to nodes

The second setup is focused on using different transmission lines, which demonstrate the measurement in a real application. The setup consists of two transmission lines, a short one and a long one. The long transmission line is approximately 30m long and it is established from a Belden 9913 cable, which is chosen for its high velocity of propagation (84%). Its main parameters are in Tab. 8.4 according to the datasheet [1]. The block diagram with cable types is in Fig. 8.21.

Table 8.4: Parameters of the Belden 9913 cable

Parameter	*Value*
Nominal characteristic impedance	50Ω
Nominal inductance	0.059 µH/ft
Nom. capacitance conductor to shield	24.6 pF/ft
Nominal velocity of propagation (VP)	84%
Conductor size	AWG 10

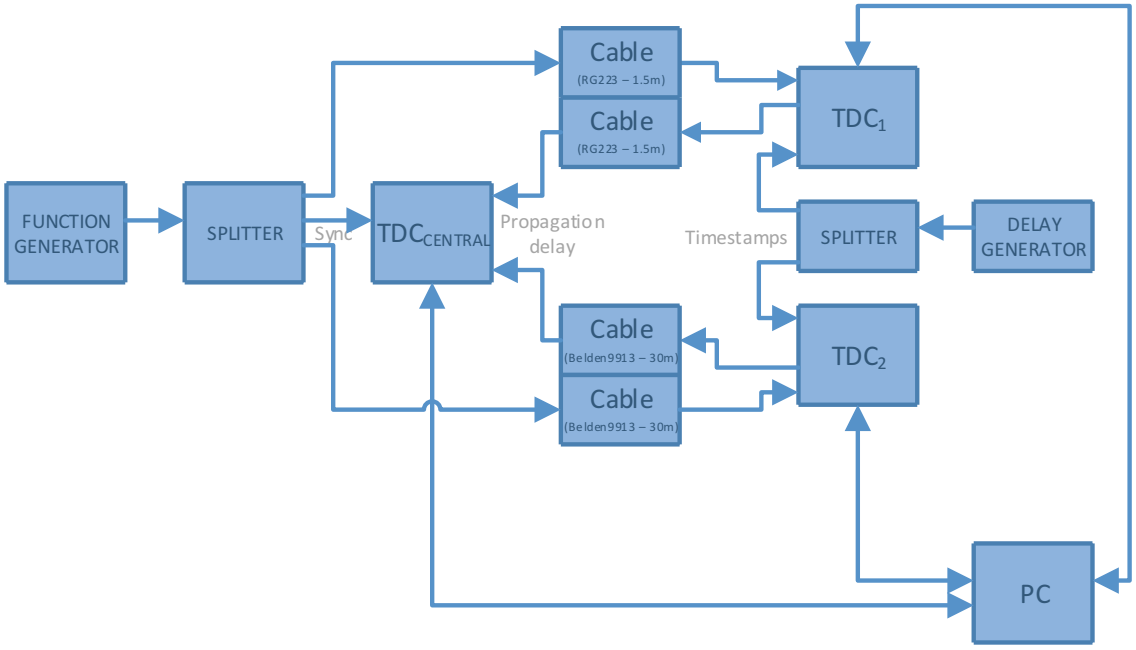


Figure 8.21: Block diagram of the setup with different transmission lines

Similar to the previous setup, measurements are made for various frequencies of generating timestamps. In the setup, the digital delay generator (described in Chapter 7) is used as the timestamp generator instead of the function generator used in the calibration setup and the setup with the same transmission lines. It allows to shift (delay) one output and to have a non-zero difference between timestamps. The k ratio computed in Section 8.2 is applied for the data taken from the TDC devices after the propagation delay correction. The difference between timestamps for the first set of results is plotted in Fig. 8.22 as a histogram. The trend of the calculated difference is in Fig. 8.23.

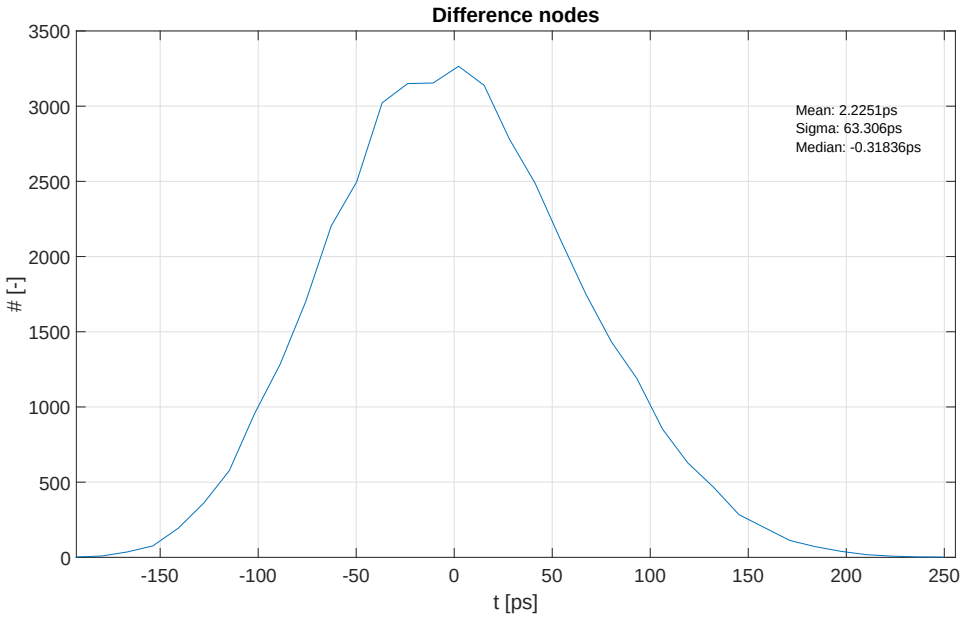


Figure 8.22: Histogram of difference in timestamps

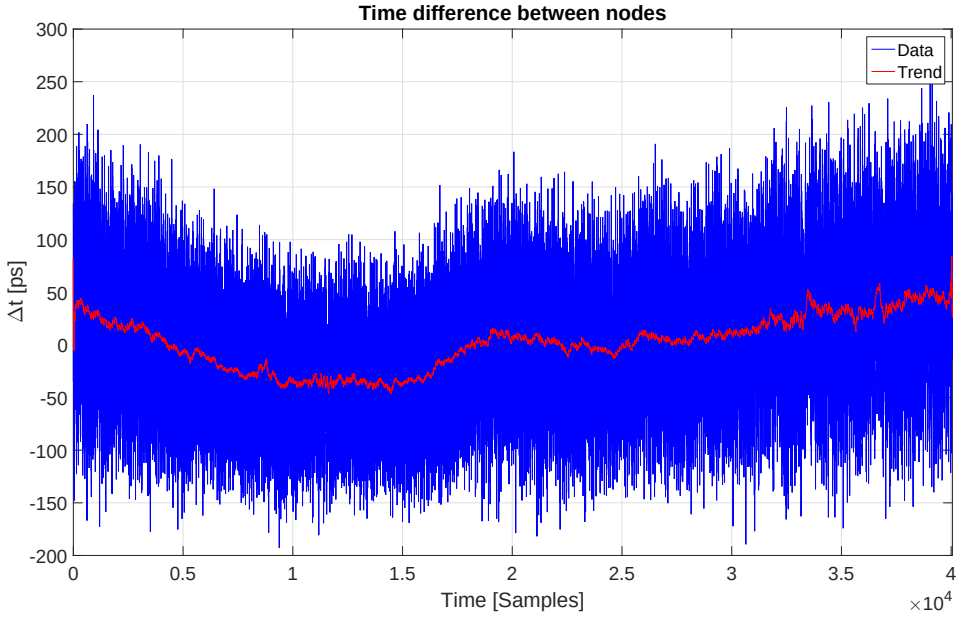


Figure 8.23: Difference in timestamps over time

The shown results are for timestamps generated at the same moment. The next measurement shifts one output about 200ps. The result is drawn in the following figures with the same representation as the previous measurement.

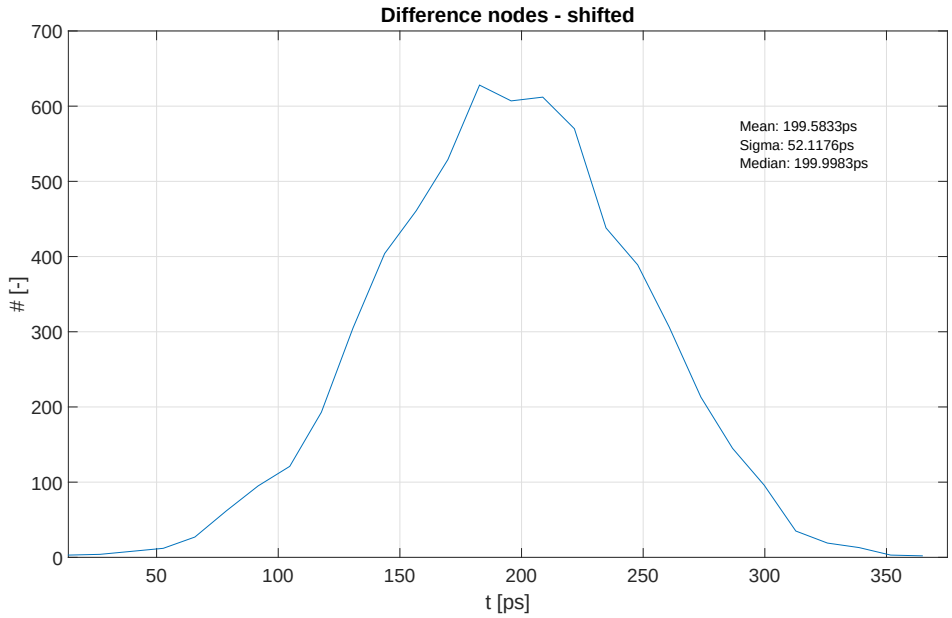


Figure 8.24: Histogram of difference in shifted timestamps

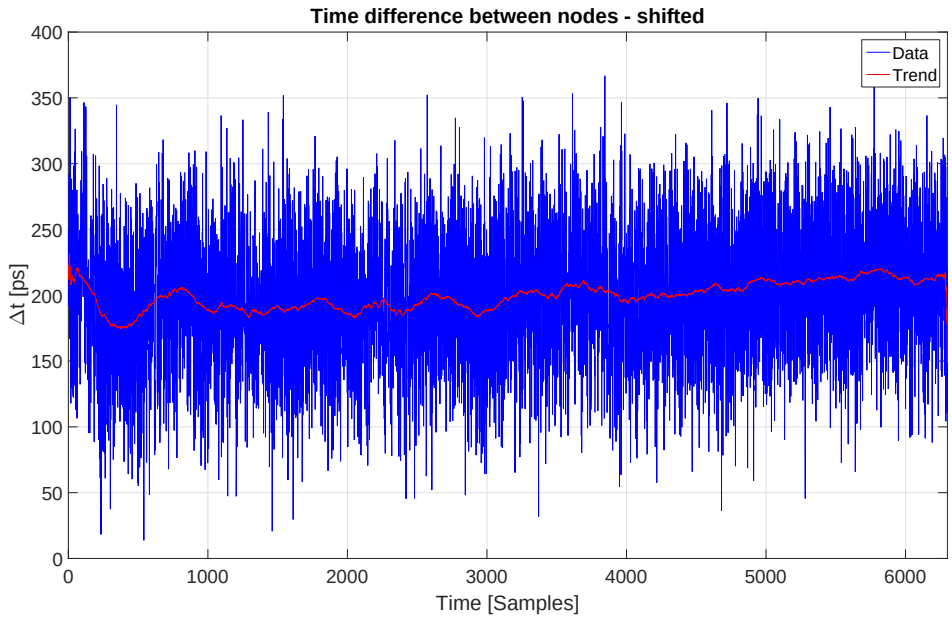


Figure 8.25: Difference in shifted timestamps over time

A shift of 200ps results in a 200ps difference between timestamps from two nodes which is seen in the histogram (Fig. 8.24). The trend (difference in time) is plotted in Fig. 8.25.

The setup allows checking the linearity of the measurement, it is similar to the linearity described in Subsection 7.2.2. The measurements were made for LSB multiples, which means delaying timestamps of 65ps, 130ps, etc. in one TDC. Tab. 8.5 shows the mean values of the measured shifts and the result is drawn in Fig. 8.26.

Table 8.5: Linearity measurement for 65ps shift

Shift [ps]	*0*	*65*	*130*	*195*
Mean	0	64.2702	129.2619	206.9320
Median	-0.6883	63.6254	128.3080	207.1029

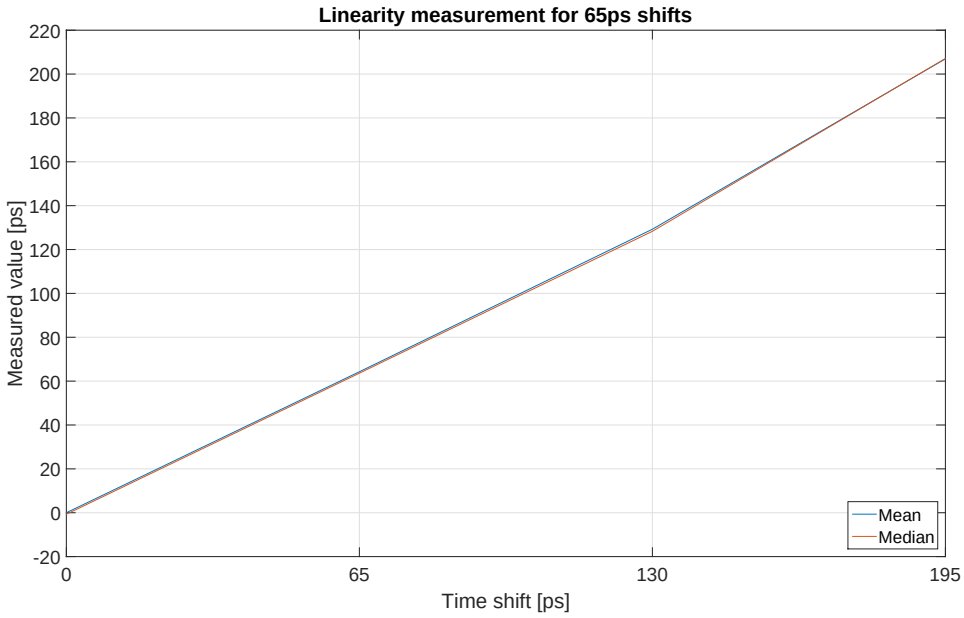


Figure 8.26: Linearity measurement for 65ps shift

8.4 Measurements in real applications

A difference exists in the setup for measurements in real applications and the setup for testing in Section 8.3. The nodes are at different places and it is not possible to use only one measuring PC. Each TDC device at node requires a measuring PC or any other device capable of communication based on USB3.0. The important measurement for synchronization is the propagation delay measurement. The propagation delay can vary due to the temperature, etc. Thus the temperature is also logged into the file during the measurement. The measured propagation delay can be divided into several periods which correspond to the measured temperature, quantity or time period. Then the timestamps are corrected to the relevant period of the measured propagation delay.

The data is sent via USB3.0 as raw data (channel, timestamp, temperature). Thus the further processing of data can be done, i.e. dividing into periods (mentioned above), averaging, etc. It makes it possible to join the processing with other scripts for other devices which require synchronization or timestamps.

Chapter 9

Other usage of time measurement unit

The Time-to-Digital Converter described in Chapter 5 has already been used in several projects. The first one is focused on the synchronization of particle detectors in different places [29]. Another one deals with a particle telescope [28].

9.1 Timepix3 synchronization

The principle described in the previous chapters is used in a simplified form for the synchronization of four pixel detectors in the ATLAS experiment at CERN. The Timepix3 was chosen as the pixel detector. A brief summary of the Timepix3 chip follows.

9.1.1 Timepix3 detector

The Timepix3 [31] detector is the last in the generation of the Medipix/Timepix series of pixel detectors. It was developed within the Medipix3 Collaboration [26] at CERN. The detector is assembled from two parts, one of them is the readout ASIC chip and the second one is the active sensor layer. Both parts are connected together by bump bonding. Various materials can make the active sensor layer, such as Si, CdTe, GaAs. The 130nm CMOS technology is used for the ASIC chip. The chip implements 65 536 channels based on 256×256 pixel matrix. The pixel pitch is 55μm. The Timepix3 simultaneously allows the Time-over-Threshold (ToT) measurement and the Time-of-Arrival (ToA) of a detected particle measurement. The time resolution is improved to 1.5625ns. It is derived from 40MHz clock generator (coarse ToA measurement) and a 640MHz ring oscillator (fine ToA measurement). Two approaches are implemented in the Timepix3 as readout process, the frame-based mode and the data-driven mode. All pixels, except the pixels with zero value, are read out in the frame-based mode. The maximal frame rate is approximately 1 300 frames per second. Only hit pixels are sent out in the data-driven mode. The advantage of such an approach is only that hit pixels are dead for approximately 475ns.

9.1.2 Katherine readout for Timepix3

The Katherine readout [30] is an Ethernet Embedded Readout Interface for the Timepix3. The readout is supposed to control one Timepix3 detector, which is assembled on the CERN chipboard for Timepix3 or a compatible chipboard with a Very High Density Cable Interconnect (VHDCI) 68-pin connector. The Katherine readout is designed as an embedded computer with the interface for Timepix3. The dimensions of the readout in the housing are 100mm in length, 80mm in width and 28mm in height. The connectors are placed on the front and rear panels. The maximal performance (it means hits per data rate) of the device is given by the bandwidth of the used Gigabit Ethernet interface and it corresponds to approximately 16Mhitps (Mpixps) in the data-driven readout mode. The readout is optimized for remote controlling, which allows a long cable connection between the readout and the detector.

Figure 9.1: Katherine readout for Timepix3

The Ethernet interface makes it possible to place the measuring computer up to 100m away from the readout without additional electronics. This feature is valuable for a measurement in radiation fields where the readout device electronics might suffer radiation damage. The chipboard can be connected directly to the device and in addition there is a possibility of using extending VHDCI cables for distances up to 10m or special cable extenders (designed specially for a Katherine readout) for distances at a range from 10–120m, but the use of longer cabling reduces the maximal hit rate due to the decreasing communication speed between the detector and the readout. Tab. 9.1 shows the maximal hit rate in dependency on the cable length.

The readout contains a high voltage power supply for the sensor bias in both polarities up to 300V. The bias voltage is provided with the LEMO connector on the front panel

of the readout. Katherine offers a General Purpose Input/Output (GPIO) connector with four general-purpose signals. The signals are dedicated to the integration of the Katherine readout into measurement setups, where the triggering or synchronization of clocks is necessary.

Table 9.1: Hit rate vs. cable length

Distance [m]	Cable	Data rate [MBps]	Hit rate [Mhitps]
3	VHDCI Extending cable	2×640	16
10	VHDCI Extending cable	4×160	10
20	Ethernet CAT7	2×640	16
100	Ethernet CAT7	4×80	5

9.1.3 Synchronization

As previously mentioned, four Timepix3 detectors are in ATLAS experiment at CERN. The detectors are in a configuration of two sandwiches. One sandwich is situated on the central barrel in ATLAS's cavern and another one is placed on the wall in the cavern. The length of the interconnection cables between detectors and the rack room, where the readout electronics are installed, is approximately 50m for the sandwich on the central barrel and 80m for the sandwich on the wall. The detectors in the sandwich on the central barrel are 4.6m away from the interaction point in ATLAS's cavern. The ATLAS detector system placed in the cavern is shown in Fig. 9.2 [17]. The interaction point is in the middle of the detector system.

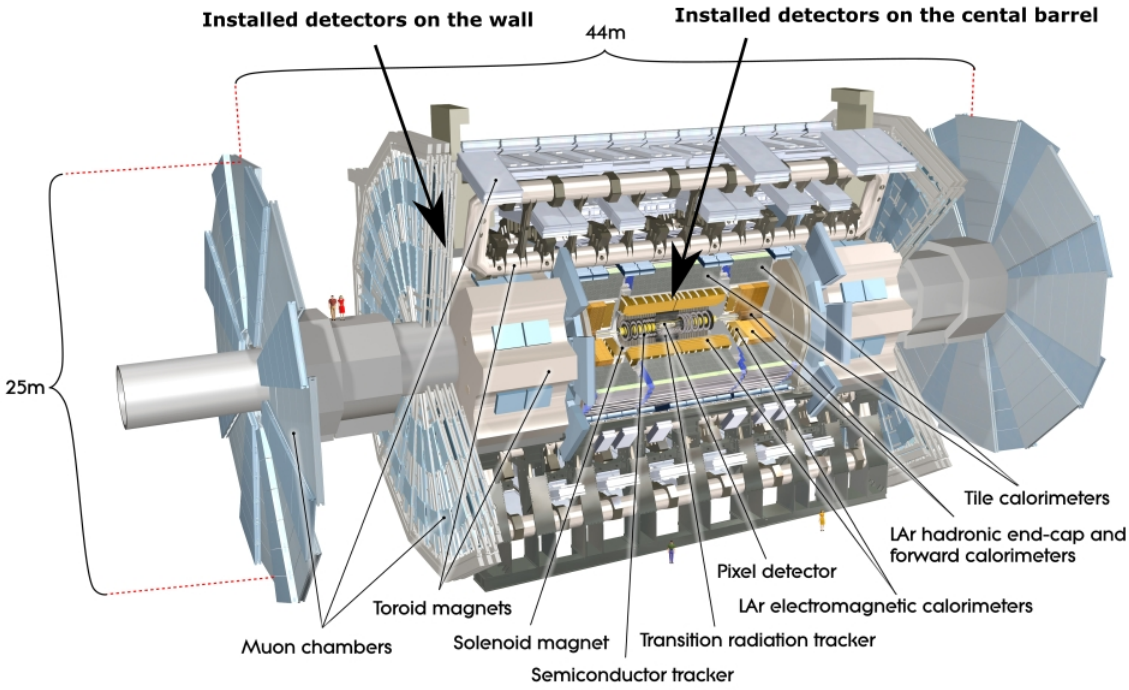


Figure 9.2: Image of the ATLAS detector [17]

The detectors are connected together through the Katherine readouts. Each readout

provides the information of the beginning of the measurement in the detector itself. The start of the measurement from each detector propagates into the TDC, which is used as a synchronization device. The TDC measures time differences (time shifts) at the beginning of the measurement in the detectors. Then the time differences are used for offline correction of timestamps from each Timepix3 detector. The described time measurement is only half of the synchronization. It covers time shifts (delays, phase differences, etc.) among Timepix3 detectors. The other half is time differences in interconnections between the detector and the readout. Each detector has its own cable interconnection with the readout. The interconnections have various lengths, which causes different propagation delays. These delays are also necessary to include in the offline correction of timestamps. Thus the chipboard and the readout have a special feedback path which is intended for the propagation delay measurement of the path between the detector and the readout. It is based on the principle mentioned in previous chapters. The feedback path is connected to the TDC device which determines the propagation delay of each path. In principle, the propagation delay measurement of the path can be made continuously, but it is not necessary because the conditions (such as temperature) can be considered as stable. Thus the measurement is made only at the beginning, it means after the installation of setup. However, it is possible to make it upon the request of a user. The propagation delays and the time differences at the beginning of the measurements are combined together into one value for each detector and the value is used for the offline correction of the timestamps.

9.1.4 Experimental results

The first important measurement for the synchronization is the propagation delay measurement. The measurement was made after the installation of the detectors and the readout electronics. The setup can be seen in the following figure (Fig. 9.3). Only 2 units are shown in Fig. 9.3, in reality there are four units. The measuring line is connected to the TDC through the RJ45 extender for the Katherine readout which is designed for long distance connection using ethernet cables.

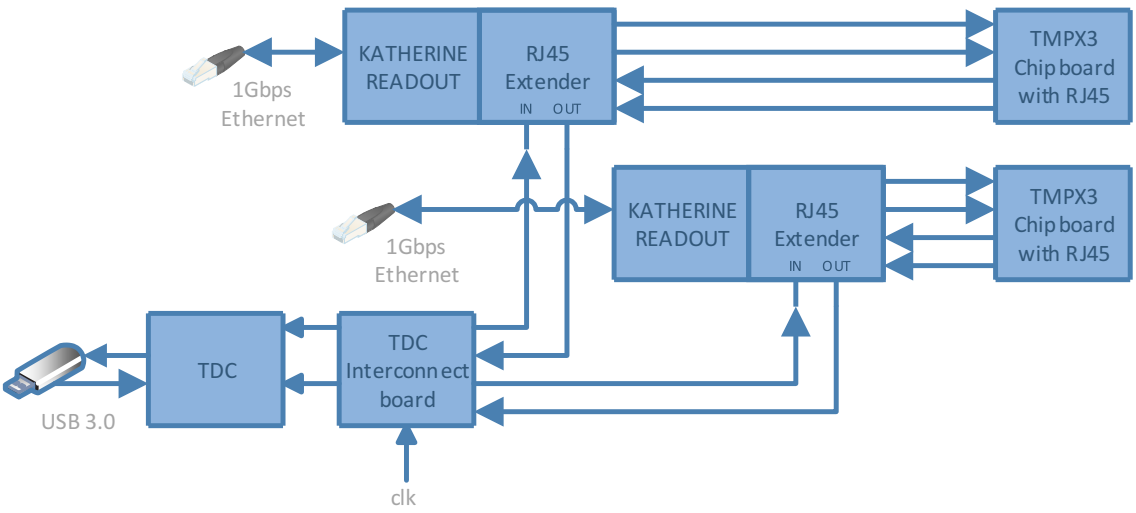


Figure 9.3: Setup for propagation delay measurement with feedback path

The measured data is processed by Matlab script and you can see results for the path between the readout and the detector on the central barrel in Fig. 9.4 and for the path between the readout and the detector on the wall in the cavern in Fig. 9.5.

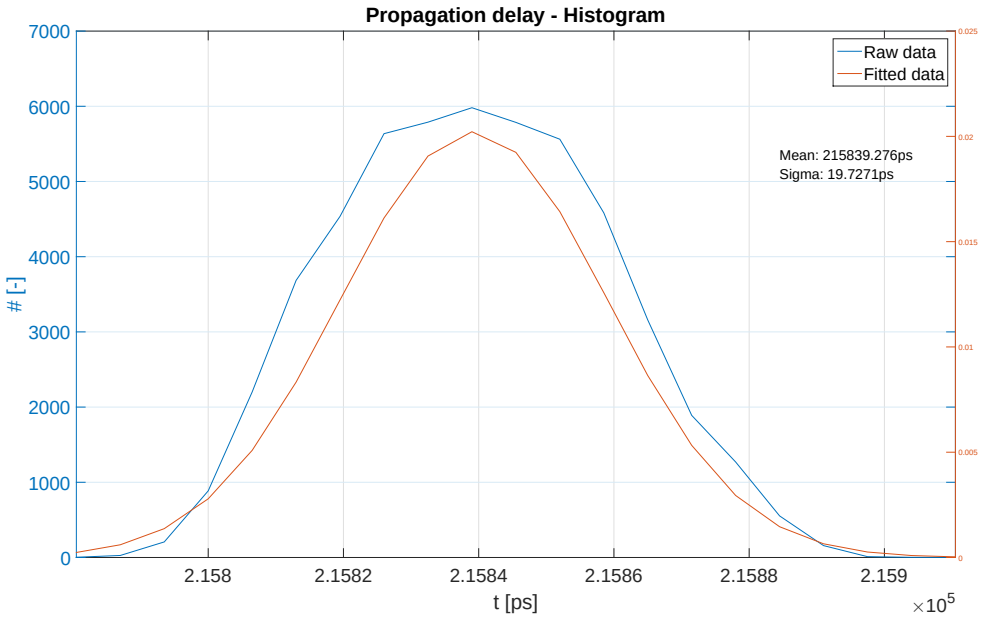


Figure 9.4: Propagation delay of cable to the detector on the central barrel

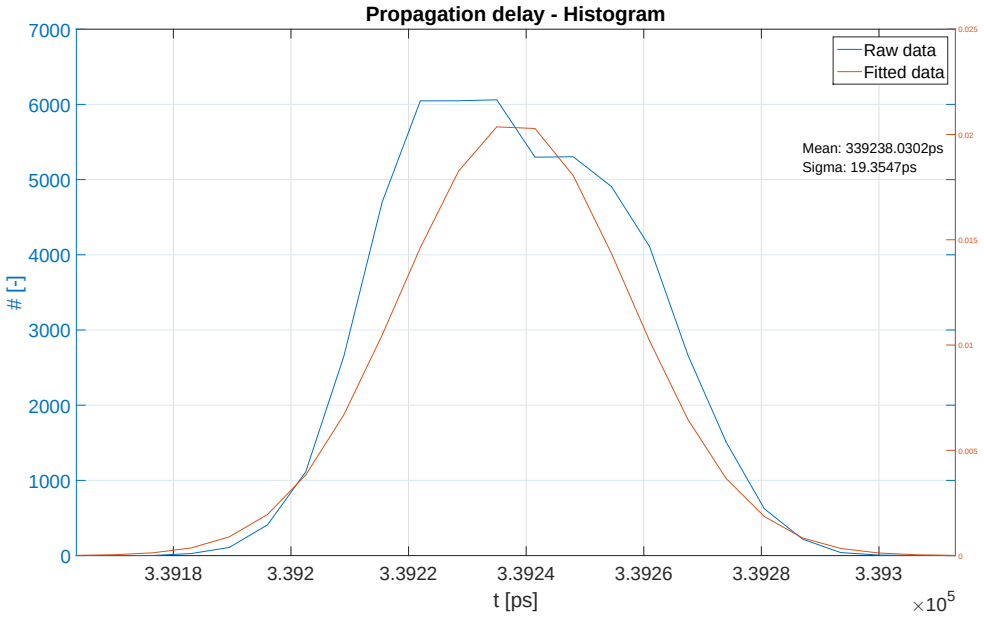


Figure 9.5: Propagation delay of cable to the detector on the wall

The mean value of a propagation delay of 215839.276ps (Fig. 9.4) corresponds to a cable length of approximately 50m. The velocity of propagation is between 77% and 78%. The mean value of a propagation delay of 339238.0302ps (Fig 9.5) corresponds to a cable length of approximately 80m. The velocity of propagation is the same as previously

mentioned. The propagation delays are used with the time differences of beginnings of the measurement for the offline correction as mentioned in the synchronization description. The time coincidence in the detectors in the sandwich on the central barrel is zoomed on one cluster in Fig. 9.6. One bin corresponds to an LSB resolution of 1.56ns. There is no difference in timestamps with a resolution of 1.56 and the offline synchronization.

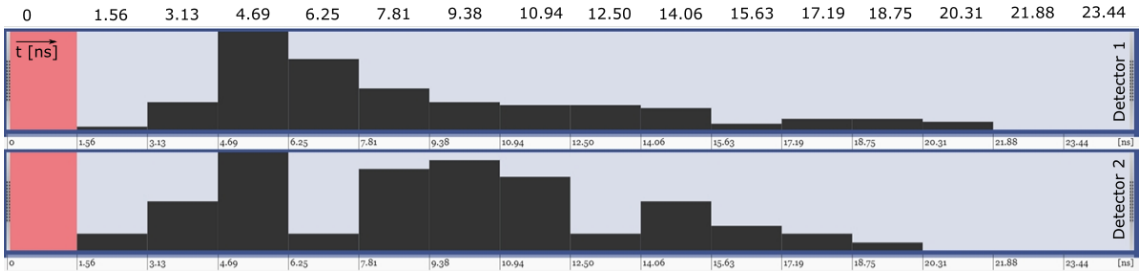


Figure 9.6: Time coincidence of the detectors on the central barrel

The following figure (Fig. 9.7) shows time coincidence between the detector on the central barrel and the detector on the wall in the cavern. There is a 62.5ns difference after the correction. The measured difference corresponds to the distance between the sandwich on the central barrel and on the wall in the cavern.

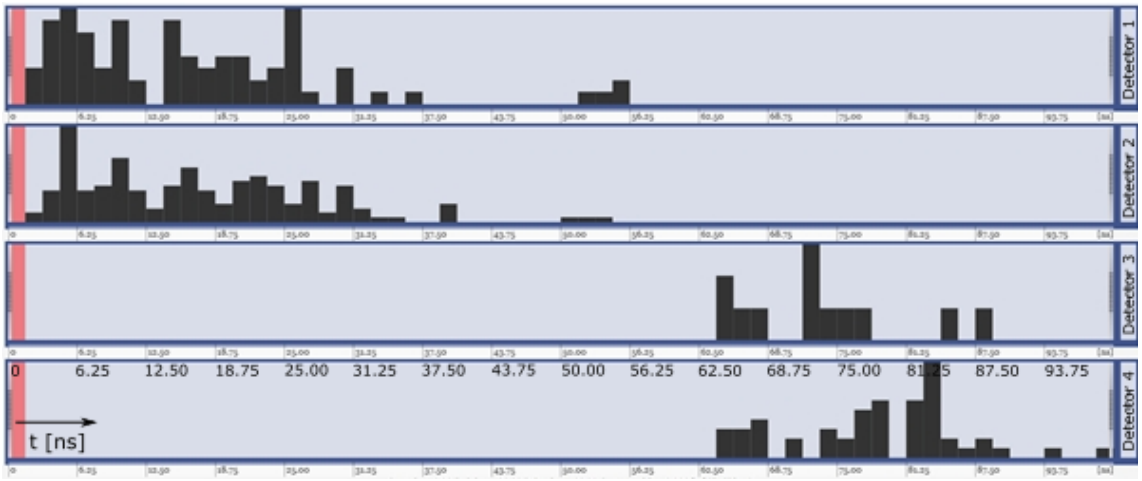


Figure 9.7: Time coincidences of the detectors on the central barrel and on the wall

From the measurements during the beam splashes, the error is observed between -LSB and +LSB of time resolution of the Timepix3 detector, which is 1.56ns. Without synchronization, particles caused by the same event can not be distinguished. The timestamps in the detectors will not correspond to the time-of-flight of the particles.

9.2 Particle telescope with Timepix3

9.2.1 Introduction in particle telescope

Timepix detectors [32] have already been used in different applications [27] including particle tracking. The latest generation of the Timepix detectors allows a simultaneous measurement of time and the energy in each of the 65 536 pixels, the time resolution is improved

to 1.5625ns and a data-driven readout scheme is implemented. With the assumption of a separation of the detectors (tens of cm), the time-of-flight measurement (velocity of charged particles) can be made because of the time resolution (1.5625ns). The Timepix3 ASIC has increased complexity and improved time resolution, thus the clock synchronization requires higher demands. The advanced techniques are necessary for synchronizing several nodes in order to implement a distributed system. When more clock sources with the same frequency are used in the system, they have to be considered as asynchronous. Uncertainties in propagation delay are produced with clock domain crossings because of resynchronization. These uncertainties and propagation delays of signals through cables or on printed circuit boards have to be taken into account regarding the time resolution of the Timepix3. The following subchapters describe the features of the Timepix3 detector and the Katherine readout in a configuration where synchronization is needed, and show the results of a test beam measurement performed at Super-Proton-Synchrotron (SPS) at CERN in a 40 GeV/c pion beam.

9.2.2 Hardware concept

The particle telescope is based on Katherine readouts for the Timepix3 detector. The usage and the principle are described in details in [28]. The system has fewer demands on the time resolution. Thus the synchronization of all nodes is not necessary with the assumption of known delays of used cables and phase differences among signals. These delays and phase differences can be measured in each node of the system. The principle for three synchronized detectors is shown in Fig. 9.8 [28].

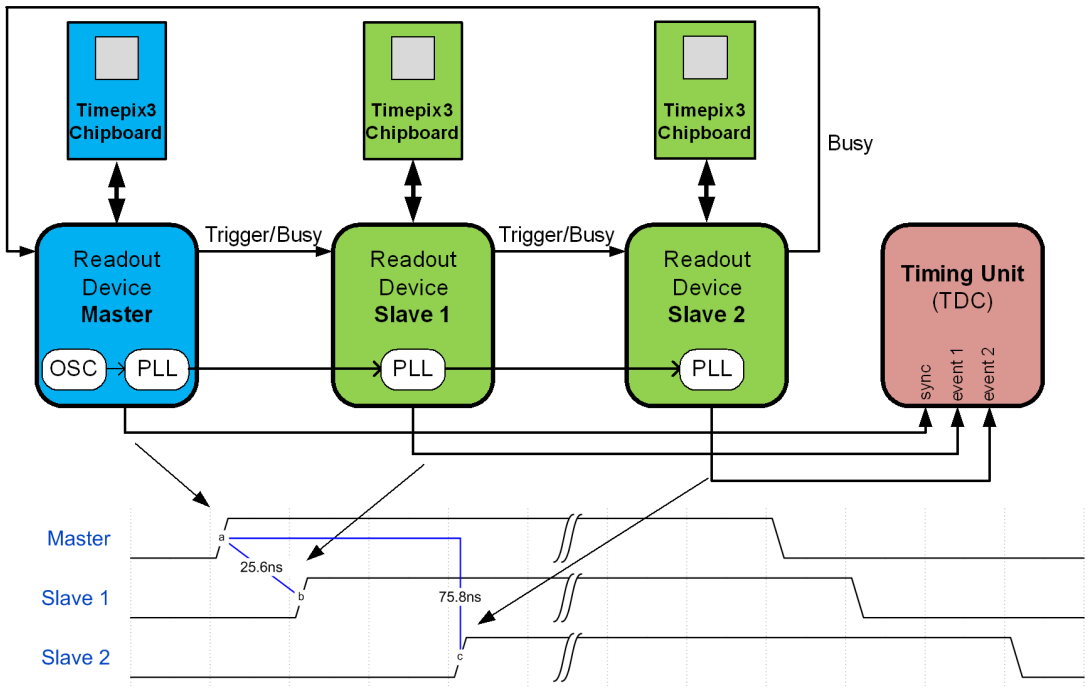


Figure 9.8: Block diagram of offset compensation of detectors

In Fig 9.8, you can see three Katherine readouts in the loop trigger chain. One of the readouts is selected as the master device and the other two readouts are slave devices. The start and the end of the measurement, which are determined by the shutter signal (trigger signal), are propagated through the loop trigger chain. The trigger chain uses the LVDS standard for signaling. The master device is able to recognize a busy or not busy state from propagating the shutter signal through the loop trigger chain. Each device provides the resynchronization of the shutter signal to the local clock domain. Due to the resynchronization of shutter signals, the detectors are opened at different moments caused by delays among detectors. In such mechanisms, the synchronization uncertainty is one clock period. The setup uses only one source of the clock signal, which is generated by the master device's oscillator. Then the clock signal is distributed to the slave devices, in which the clock signal is recovered by a Phase Locked Loop (PLL). PLLs are also sources of phase shifts.

The propagation delays of shutters, which consist of phase differences of the clock signal and detectors triggering, are measured by the time measurement unit (TDC). The TDC is described in Chapter 5. Each readout produces a copy of the shutter signal and the time differences among the signals are determined after the start of the measurement. The TDC is capable of compensation up to 5 Katherine devices. In such a configuration, one device acts as the master (feeds the sync input of TDC) and the other devices act as slaves (feed the event inputs). It is possible to increase the number of synchronized devices by using additional TDCs, one additional TDC adds 4 more event inputs for the Timepix3 readouts. The TDCs are connected together via the synchronization output channel (see Section 5.4, return channel).

9.2.3 Experimental results

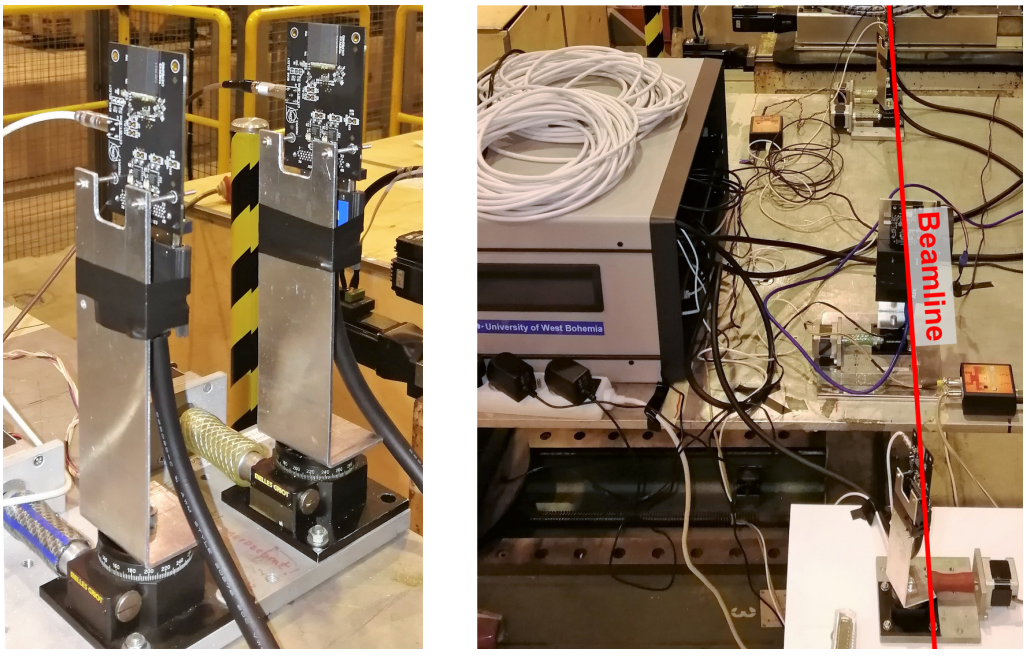


Figure 9.9: Photos of measurement setup

From the point of view of the time measurement in the setup, a systematic inaccuracy of the time-of-flight value below 1 ns was found. The inaccuracy is below the time resolution of the Timepix3, but it can effect the results in short distances. During the measurement, an effort was made to better understanding the inaccuracy. As such, 10 000 short measurements were made and the time differences in released shutters were measured by the time-to-digital converter. The results are presented in Fig. 9.10, Fig. 9.10 also shows the standard deviation of approximately 115ps. The results prove to not be the origin of the 1ns inaccuracy because the standard deviation is lower than the time resolution of the Timepix3.

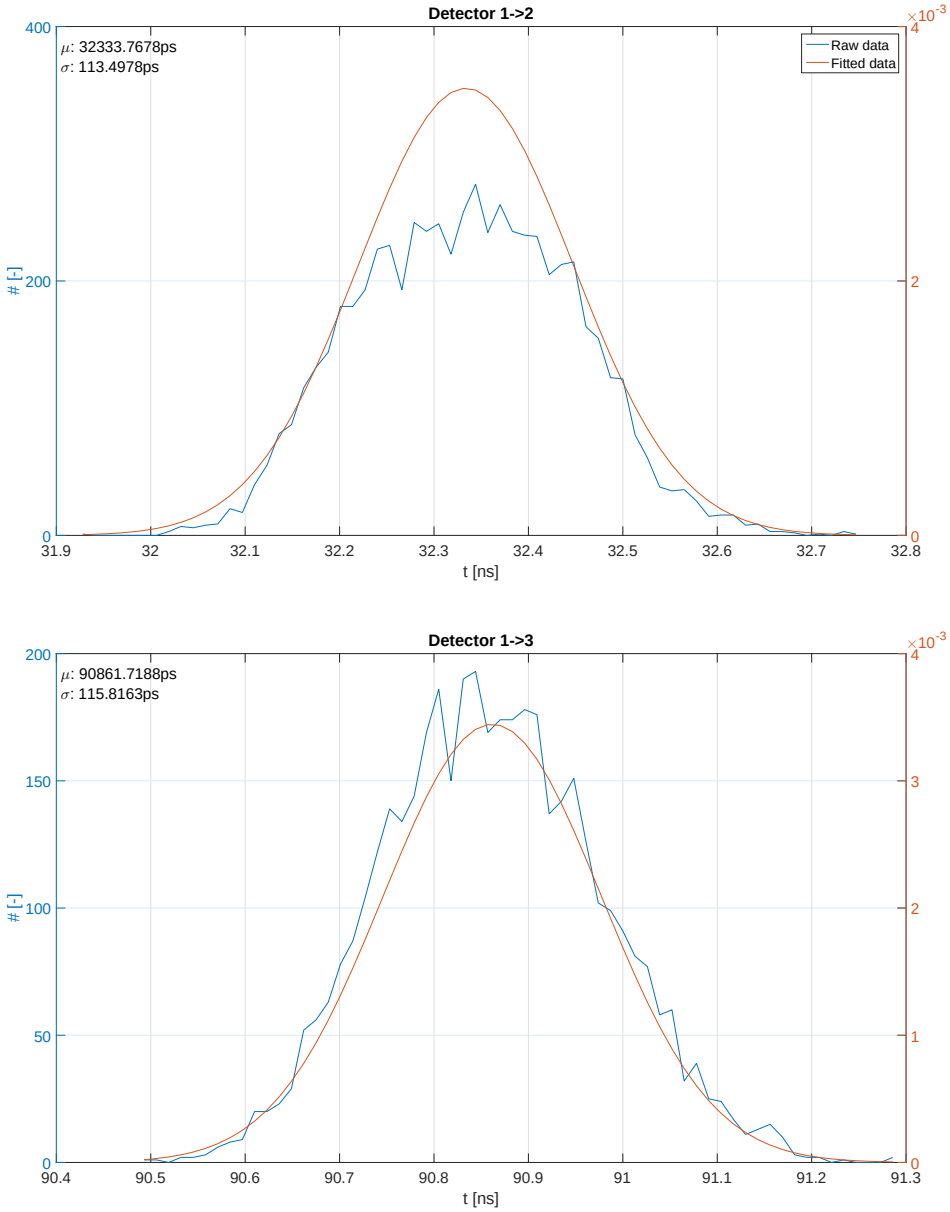


Figure 9.10: Time differences in released shutters

The TDC unit has proven itself during the measurement as a useful device in such an application as the particle telescope with Timepix3 detectors.

Chapter 10

Conclusions

The thesis deals with systems for the time measurement and the synchronization among these systems with very high resolution in the order of picoseconds. The systems with such time resolution are a current problem in particle physics experiments, as mentioned in Motivation of the thesis.

The important thing in the system is the signal distribution which is described in Chapter 4. Two approaches of signal distrubution are described (electrical and optical). The designed systems in the thesis only use electrical transmission. The thesis deals with time measurement and the time measurement is focused on the measurement in time domain. The main part of the designed system is the time-to-digital converter, which is introduced in Chapter 5. The basic description of how the TDC is designed and its parameters are shown in this chapter. The control software as a desktop application was programmed for TDC. The software makes it possible to set the TDC for chosen measurements and to log data into the file for further processing. A short summary of possible error in the measurement is in Chapter 6 including the calculations.

Chapter 7 is focused on measurements with the designed TDC. The chapter provides basic functionality measurements, calibration and examples of TDC usage in measurements as stand alone applications. Calibration is necessary for the equalization of the inputs, i.e. the time offset for each channel is obtained. All relations between signals and corresponding histograms have proved the calibration method. The next important parameter of the measurement is its linearity. The linearity has been checked by the delay generator and results showing the linearity have been plotted. Stand alone applications of TDCs have been introduced and they are a part of the designed system with synchronization.

The following chapter described the whole system for time measurement and its synchronization in the order of picoseconds. A block diagram of the system hase been shown and explained. In the subchapter, the correction algorithm was introduced. It is necessary because each device has its own clock source. The subchapter offered the correction algorithm to remove the effects of different clock sources. A better solution is avoiding different clock domains and trying to use only one clock source, but it may result in several complications. One of them is an extra path dedicated for the clock signal in the system. Then the system was tested and results proving the successful synchronization were discussed.

The last chapter was dedicated to the usage of the designed devices. The experiments

were introduced and they are explained from the point of view of time measurement including results focused on time measurement.

Using the time domain for the time measurement brings several features. A short list of features of the designed system in the time domain follows:

- Cheap in comparison with measurement in frequency domain (vector network analyzer is needed in frequency domain)
- Only electrical transmission lines (no additional expensive converters to optical transmission)
- Limited distances (tested up to 100m with LVDS signaling, 40m with CMOS signaling)
- No common clock source (suitable for existing systems with limited interconnections, the correction algorithm is needed)
- TDC is used for the synchronization of all nodes and the same device is used for timestamping in nodes (no need of vector network analyzer for node synchronization nor any other device for timestamping)

To summarize all results, the system for time measurement in the time domain has been designed. The system measures timestamps in several places at various distances. These timestamps are synchronized to each other. All of these measurements have been made in order of picoseconds and it is seen in several histograms showed in the corresponding chapters. The work, which has been done, has successfully fulfilled the intentions and goals following from the Introduction and Motivation. Furthermore, the designed TDC and principles of synchronization have already been used in several experiments, such as Timepix3 synchronization in ATLAS cavern at CERN. The usage confirms the relevance of the topic of the thesis.

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