Universal balancing method of flying capacitor converters

Jiří Brychcín
Research and Innovation Centre for Electrical Engineering (RICE)
University of West Bohemia
Pilsen, Czech Republic
brychj@fel.zcu.cz

Tomáš Košan
Research and Innovation Centre for Electrical Engineering (RICE)
University of West Bohemia
Pilsen, Czech Republic
kosan@fel.zcu.cz

Zdeněk Peroutka
Research and Innovation Centre for Electrical Engineering (RICE)
University of West Bohemia
Pilsen, Czech Republic
peroutka@ieee.org

***Abstract*—This paper describes novel method of balancing of multi-level flying capacitor converters. The proposed balancing block is placed behind PWM modulator instead of balancing table and it is independent on type of modulator nor number of levels. The method was simulated in ModelSIM and PLECS/Simulink and implemented in VHDL to FPGA. Function of the proposed algorithm was verified on the real seven level flying capacitor converter with three phase asynchronous machine.**

Keywords—modulator, balancing, model, simulation, implementation, multilevel, flying, capacitor

I. INTRODUCTION

There are a lot of methods how to modulate and to balance the flying capacitor converter. Basic types of modulators are phase-shifted PWM (PSPWM), phase-disposition PWM (PDPWM), space vector PWM, together with modulators based on prediction and fuzzy logic. All these methods must be able to balance voltage on flying capacitors to achieve proper function of converter.

The most common methods for balancing voltage on flying capacitors are those with PI controllers of voltage [1], which change modulation signal or carrier signal for each transistor. They are usually followed by PSPWM modulator which has auto-balancing capability. This method is perfect for easy change of number of levels, but algorithm must be able to detect load mode (generator or motor). This problem was solved in [2], in this paper authors deal with modified PSPWM with PI controllers and they used direction of the load current in balancing block to achieve proper balancing. Another method for balancing of 4L converter is in [3], where there is proposed 4L PDPWM modulator with balancing table placed behind the modulator. There is problem with balancing table that is composed of combinatoric logic and is usable only for four level FLC converter. Any change in number of levels means redesign of balancing table. Other methods do not use triangular carrier signal, which is replaced by: space vector PWM in [4], predictive control in [5], fuzzy logic controller in [6]. These methods can be difficult to implement and can consume high amount of computation time. Also for different number of levels there is necessary to alter core algorithm and add or remove extended switching states. These problems are solved in proposed balancing algorithm based on mathematical model of FLC.

All of methods mentioned above has its advantages and disadvantages and our proposed balancing method for flying capacitor-based converters is simple and efficient replacement for them. Main advantage (universality) of our method is its independency on modulator type. This method is easy reconfigurable for required account of levels.

II. MATHEMATICAL MODEL OF 7L FLC CONVERTER

The power circuit of the 7L FLC is shown in Fig. 1. It was used to derive a mathematical model. There are Tx transistors and complementary transistors Tx'. Following text assumes that the positive phase current flows out of the converter to the load.

If the T_{XN} transistor is on and its neighbor T_{XN-1} transistor is off, the phase current will flow through the C_{XN} capacitor and positive amplitude will discharge capacitor, negative amplitude will charge the capacitor and the T_{XN} adds to the phase voltage value of voltage of this capacitor. If the T_{XN} transistor is off and T_{XN-1} transistor is on, the phase current will flow through the capacitor and positive amplitude of phase current will charge the C_{XN} capacitor, negative amplitude will discharge the capacitor and the T_{XN}' adds to the phase voltage negative value of this capacitor voltage. If the T_{XN} and T_{XN-1} are both on or off, the capacitor current will be zero because it is clamped and value of the capacitor between these transistors will not influence the phase voltage. Phase voltage and polarity of flying capacitors currents were obtained in mathematical model and the phase current is calculated from known RL parameters of the load. The knowledge of phase current is necessary to determine capacitor currents, which are used for calculation of voltage of the flying capacitors. The diagram of the mathematical model of 7L FLC is shown in Fig. 2.

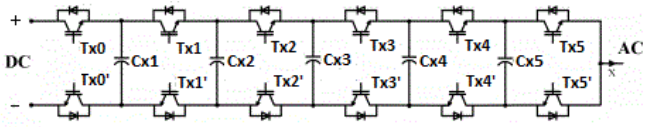

Fig. 1. Power circuit of one phase of 7L FLC

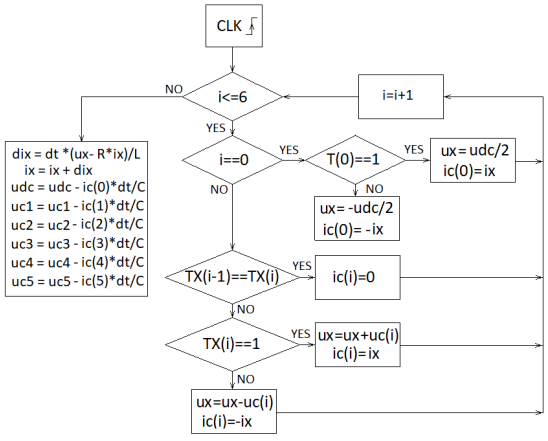

Fig. 2. Mathematical model of one phase of 7L FLC

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III. BALANCING METHOD

The balancing method is derived from mathematical model of 7L FLC converter, which is shown in Fig. 2. The balancing algorithm function can be divided to two steps: 1) predictor and 2) corrector. The predictor chooses the optimal switching combination according measured and required values of flying capacitors and according to the output current polarity. switching combination is chosen independently of outputs of modulator. The second step is correction of predicted switching combination. It is necessary because the output level of the balancing block has to be the same as required level, i.e. it must match output of the modulator in term of output voltage. This method uses the fact, that sum of states of upper T_X transistors is level of output voltage. The corrector algorithm reads states of transistors in for cycle and changes the state of transistors to achieve correct value of level on output. When equality of the input and output levels is achieved, then the corrected switching combination is written to the outputs. A block diagram of the predictor is shown in Fig. 3 and corrector in Fig. 4, where *ix* is phase current, *i* and *x* are pointers of array, *Ucw* is array of required values of flying capacitors voltage, *Uc* is array of values of flying capacitors voltage, *T* is array of input signals from modulator, *TX* is array of outputs used for balancing. The *TX* array is written to the outputs at the end of corrector algorithm run.

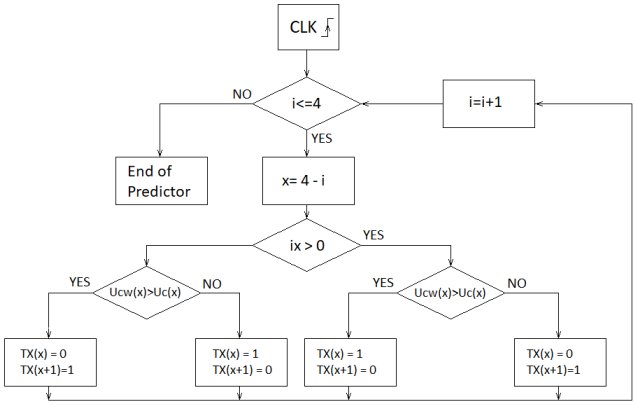

Fig. 3. Diagram of predictor function

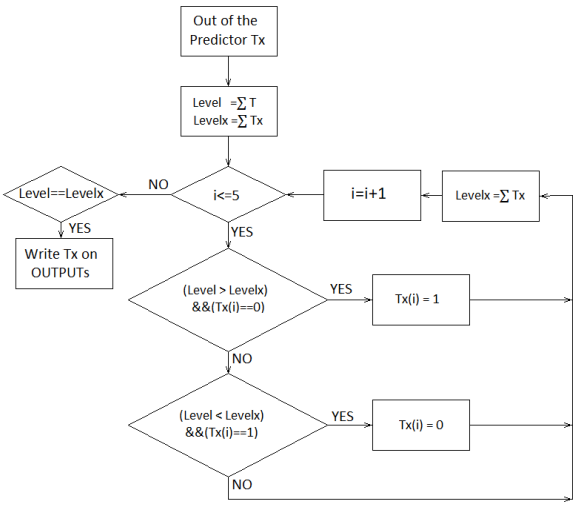

Fig. 4. Diagram of corrector function

IV. VHDL SIMULATION IN MODELSIM

VHDL simulation in ModelSIM of 7L FLC converter was performed to verify correct function of proposed balancing algorithm. The structure of VHDL entities is shown in Fig. 5. There is three phase sinus generator, followed by PWM modulator. It generates 6 output signals per each phase. These signals are then connected to the balancing entities, which choose optimal switching combination according to balancing method algorithm described in Section III. Output signals of the balancing entities are connected to the mathematical model of 7L FLC converter. The 7L FLC model is composed of three entities, one phase model of 7L FLC converter is used per each phase. Their outputs are values of flying capacitors and output phase voltages, which are calculated according to phase currents and switching combination. The mathematical model entities contain comparators, which compare whether the required values of flying capacitors are higher or lower than calculated value of flying capacitor. The outputs of comparators are connected to the balancing entities. Phase currents are calculated by last block which simulates three phase R-L load. The calculated currents are connected to the balancing and mathematical model entities. The model runs at clock frequency of 10MHz and the values of the voltage and currents are read by balancing entities only once per switching period of modulator. This is necessary to have the same output switching frequency as modulator frequency.

Simulation results are shown in Fig. 6, Fig. 7, Fig. 8 and Fig. 9. In Fig. 6 there is steady state of 3 phase converter voltage and first phase current for R=2Ω and L=20mH. In Fig. 7 there is shown first phase converter voltage and first phase current during transition change of resistance, that was decreased from 120Ω to 2Ω in time 25ms and in Fig. 8 is shown increase of resistance in time 75ms back to 120Ω, inductance was constant L=20mH. Fig. 9 shows balancing of FLC during transition of resistance in time 25ms and 75ms. Simulation parameters are shown in TABLE I.

TABLE I. SIMULATON PARAMETERS

Udc	600V
fs switching frequency	15kHz
Cx flying capacitors	100µF
L inductance of load	20mH
R resistance of load	2Ω and 120Ω

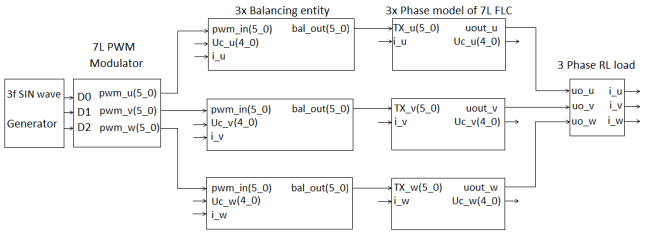

Fig. 5. Structure of implementation in VHDL

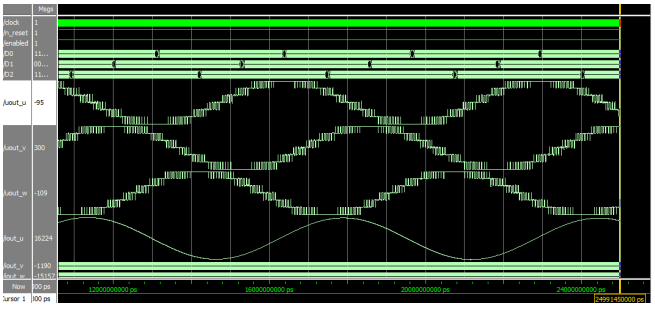

Fig. 6. 7L FLC converter 3 phase voltage and phase current - steady state for R=2Ω L=20mH

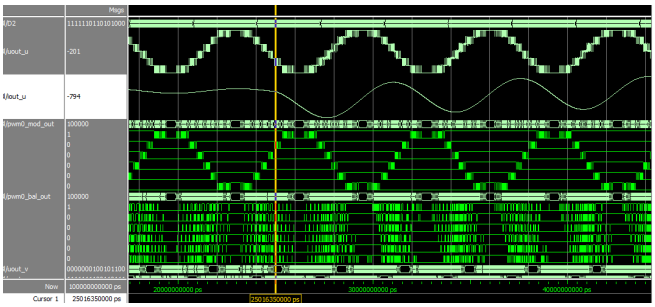

Fig. 7. Phase voltage, phase current and states of outputs of the modulator and of ouputs ofthe balancing block during transition decrease of resistance in time 25ms

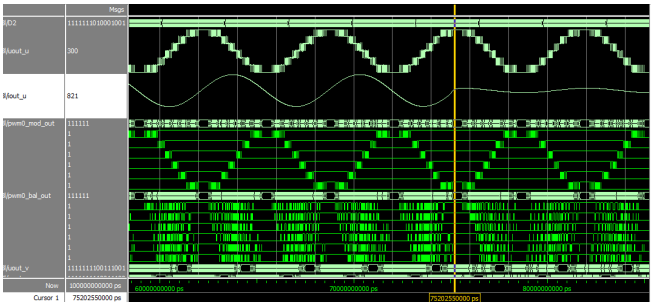

Fig. 8. Phase voltage, phase current and state of outputs of the modulator and of ouputs ofthe balancing block during transition increase of resistance int time 75ms

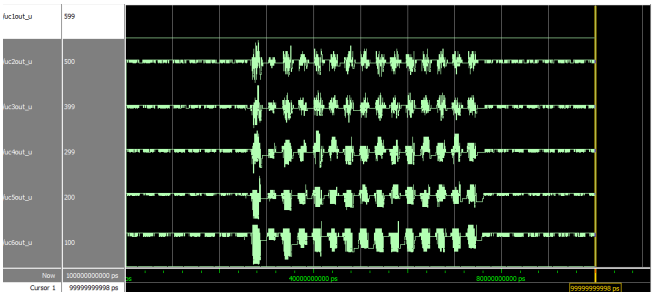

Fig. 9. Balancing of flying capacitors in transition change of resistance

V. SIMULATION IN PLECS/SIMULINK

For the verification of the 7L FLC balancing in VHDL, the simulation in PLECS was done for the same parameters as in ModelSIM simulation. Simulation results for steady state are in Fig. 10, transient change of resistance and balancing of flying capacitors are shown in Fig. 11. Simulation parameters are shown in TABLE I. Simulation was performed by 150Hz output frequency and full amplitude of modulation signal. The maximum ripple of voltage of flying capacitors is 20V p-p. From both simulations results the proper function of balancing method is verified.

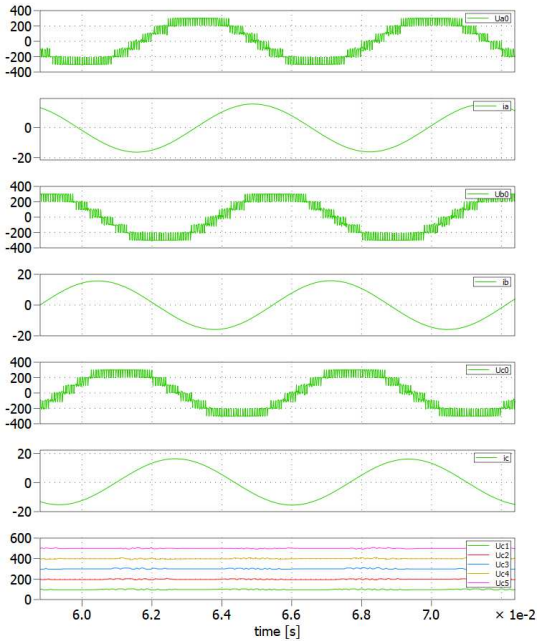

Fig. 10. 7LFLC phase converter voltage, phasecurrents and voltage of flying capacitors in steady state for R=2Ω, L=20mH

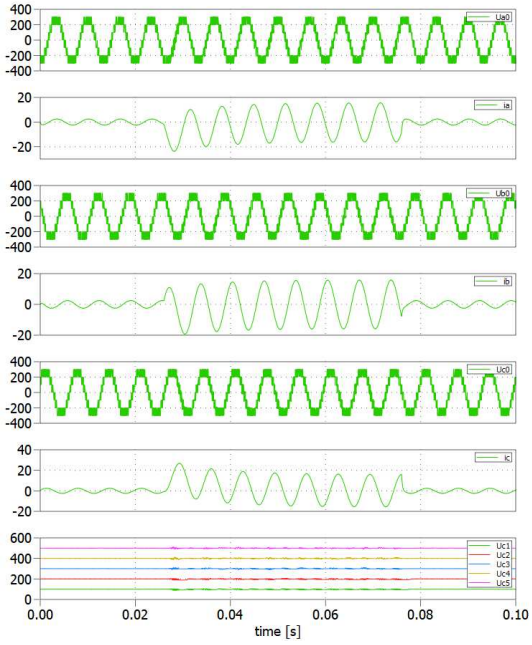

Fig. 11. 7LFLC phase converter voltage, phasecurrents and voltage of flying capacitors in transient change of resistance in time 25ms and 75ms

VI. EXPERIMENTAL RESULTS

For verification proposed balancing algorithm, the experiments were performed on real hardware. The hardware consists of control unit MLC interface and modular three phase 7L-FLC converter (Fig. 12). The FLC converter is loaded with three phase asynchronous machine. The MLC interface is hardware development kit with MCU module and FPGA on main board. It is equipped with DSC TMS320F28335 and FPGA EP3C40 together with AD, DA converters and up to 48 PWM outputs for multi-level converters control. The DSC is calculating three phase modulation signals and transfers them to the FPGA design. The proposed balancing algorithm is implemented in FPGA together with PD-PWM based modulator. The converter parameters are shown in TABLE II. Experimental results are

shown in Fig. 13 and Fig. 14. Fig. 13 shows steady state for 5Hz output frequency and output voltage amplitude 0.25. Maximum voltage ripple is 10V p-p. Fig. 14 shows steady state for 50 Hz output frequency and output voltage amplitude 1.0. Maximum voltage ripple is 10V p-p. Both results show acceptable behavior of proposed balancing algorithm.

TABLE II. FLC CONVERTER AND MOTOR PARAMETERS

Udc	60V
fs switching frequency	40kHz
Cx flying capacitors	40μF
Rs stator resistance	1.86Ω
Rr rotor resistance	1.53Ω
Lss stator stray inductance	5.3mH
Lrs rotor stray inductance	4.3mH
Lm main inductance	33mH
J moment of inertia	0.01kgm^2

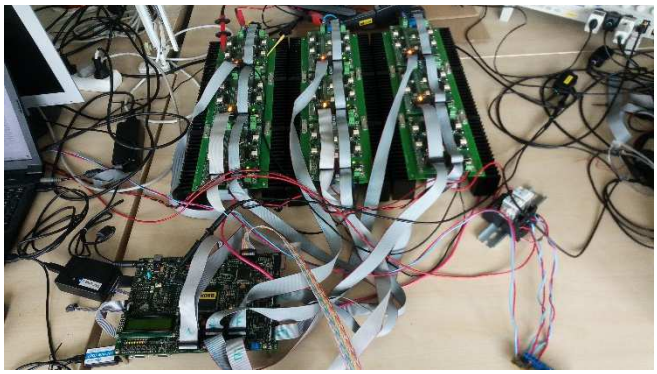

Fig. 12. MLC interface with 3 phase 7L- FLC converter

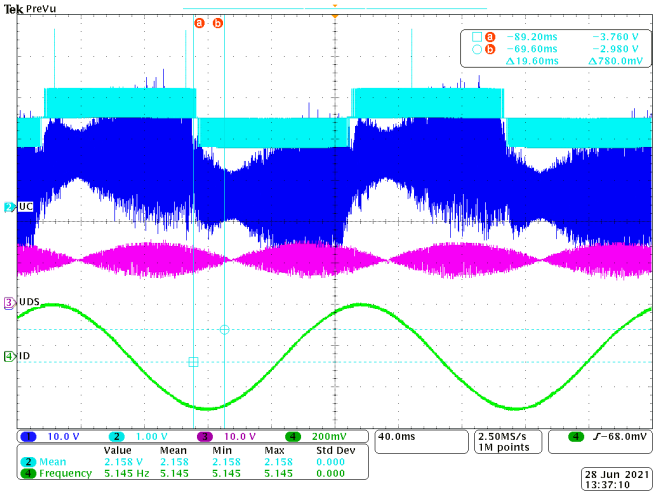

Fig. 13. Measured results for 5Hz frequency :CH1 (blue) phase converter voltage [10V/div], CH2 (cyan) required level of the converter, CH3 (magenta) voltage of flying capacitor Cx5[10V/div], CH4 (green) phase current [2A/div]

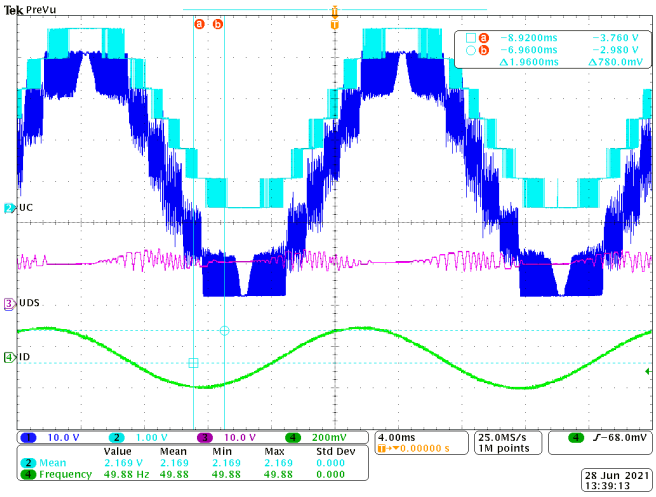

Fig. 14. Measured results for 50Hz frequency :CH1 (blue) phase converter voltage [10V/div], CH2 (cyan) required level of the converter, CH3 (magenta) voltage of flying capacitor Cx5[10V/div], CH4 (green) phase current [2AV/div]

VII. CONCLUSION

This paper describes proposed algorithm of balancing multilevel FLC converters. The balancing algorithm was simulated on 3 phase seven level FLC converter in ModelSIM and PLECS with identical results. Behavior of balancing algorithm was verified on the real three phase 7L-FLC converter with three phase asynchronous machine. The performed experiments show proper function of balancing algorithm in steady-state. Next step will be performing experiments in dynamic states and full DC-link voltage.

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