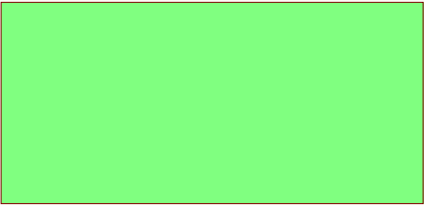
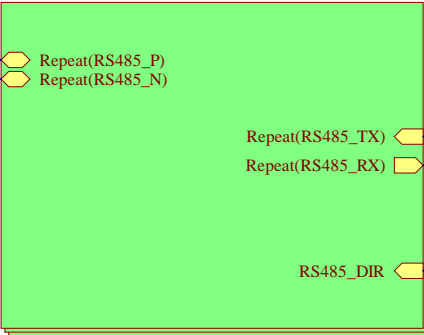


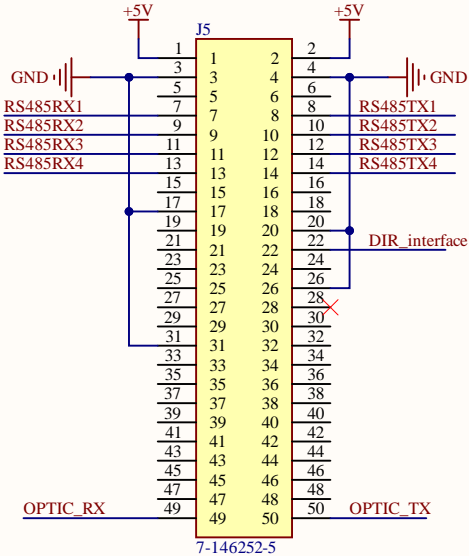
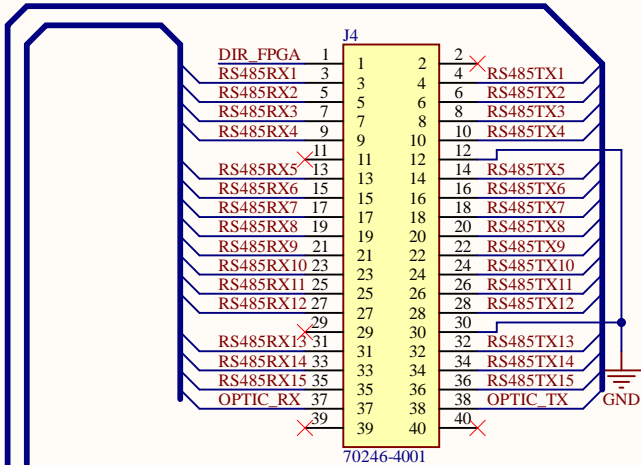
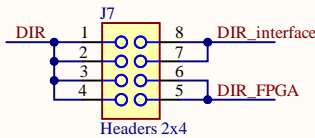
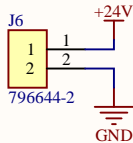
Designator  
Power.SchDoc



Repeat(RS\_1,15)  
RS485.SchDoc



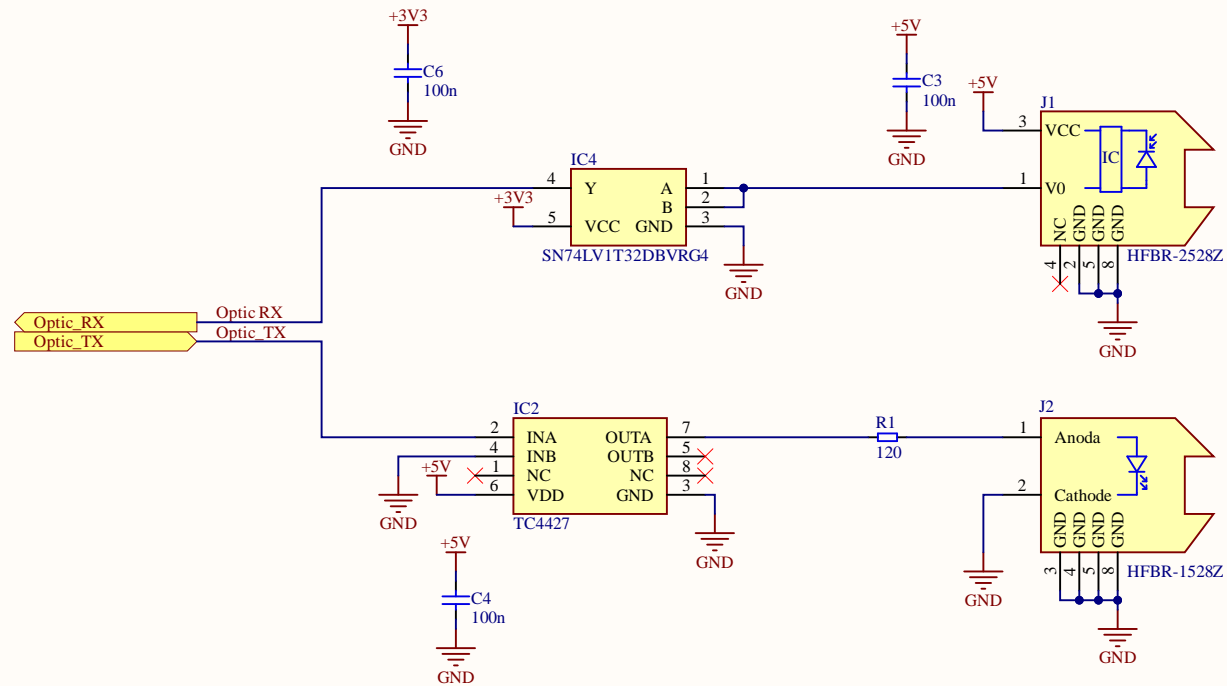
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# Diplomová práce

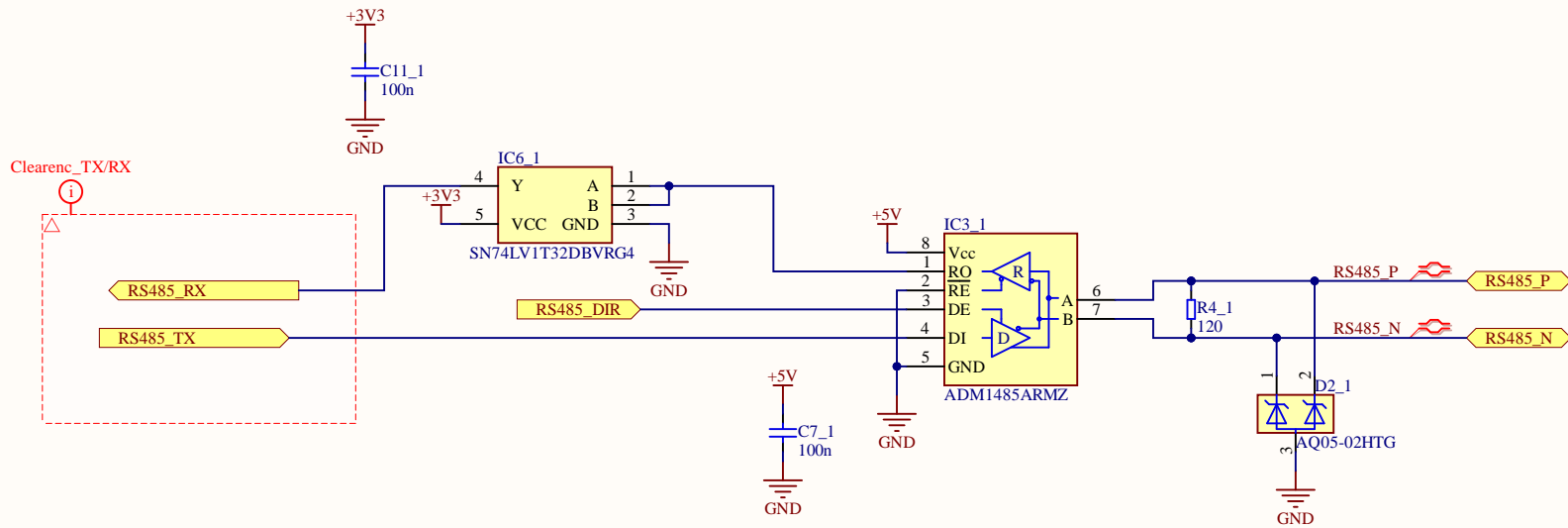
Size: A4	Date: 24.05.2022	Title: Interface k FPGA	
Author: David Bartůněk	Subtitle: RS485/FPGA	Variant: [No Variations]	
Checked by: David Bartůněk	Nr.: 1	Revision:	
Approved by:	Type: Digital	Sheet 1 of 4	
	File: Main.SchDoc		





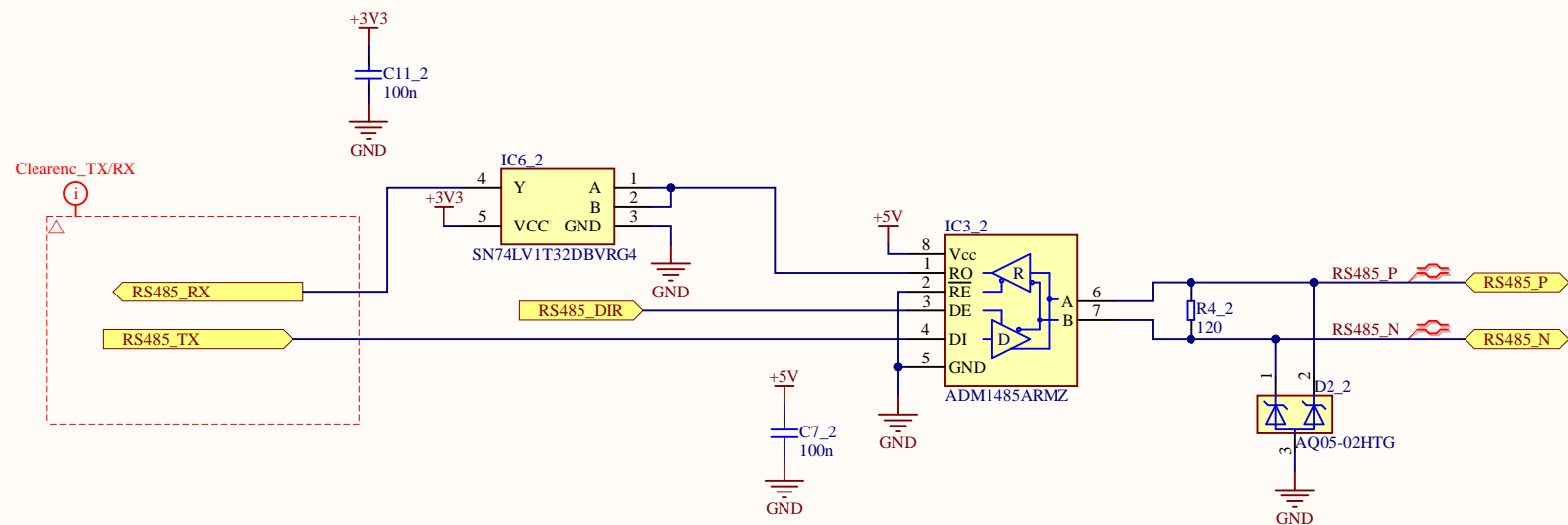
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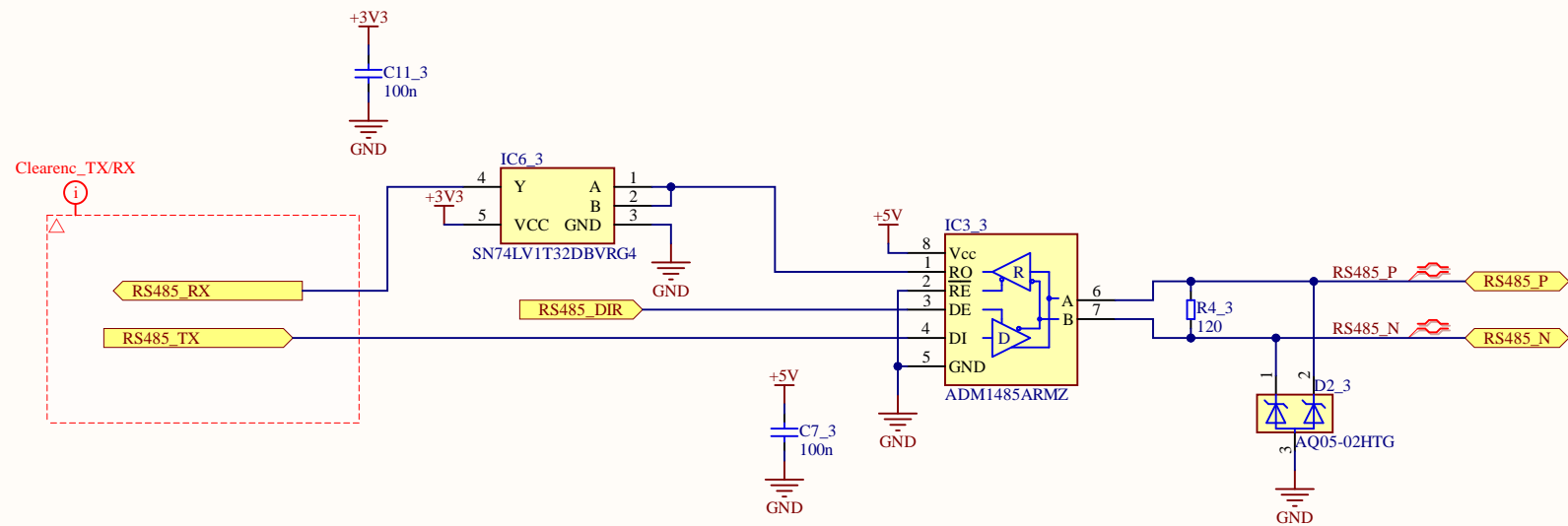
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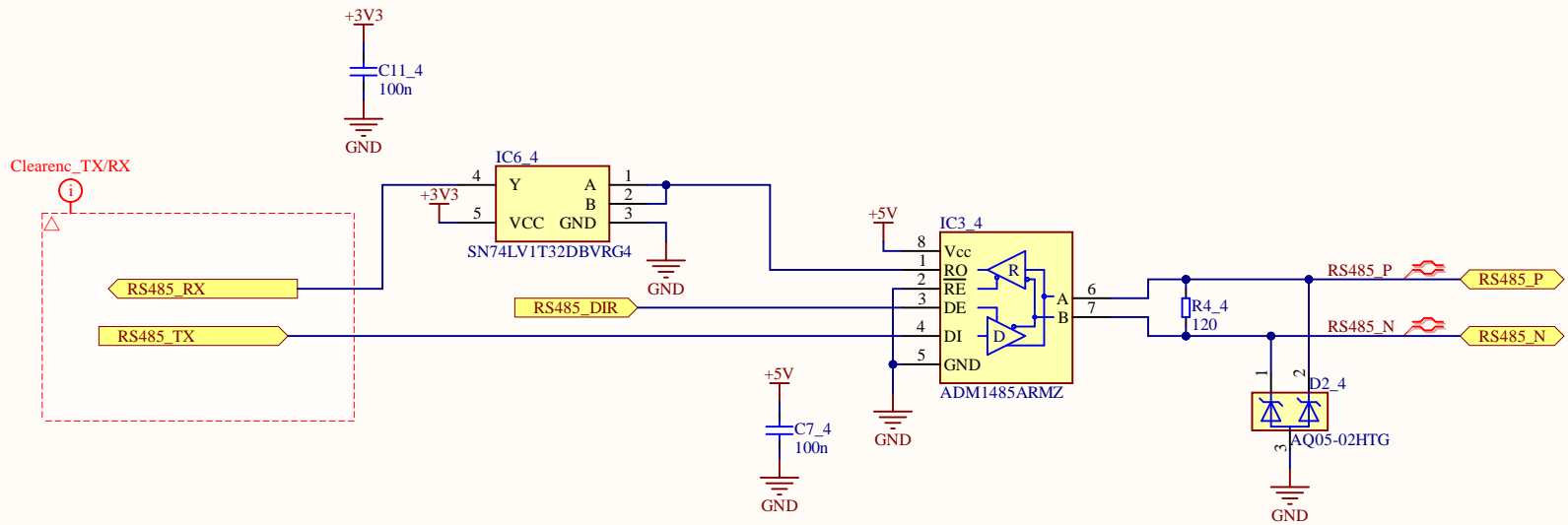
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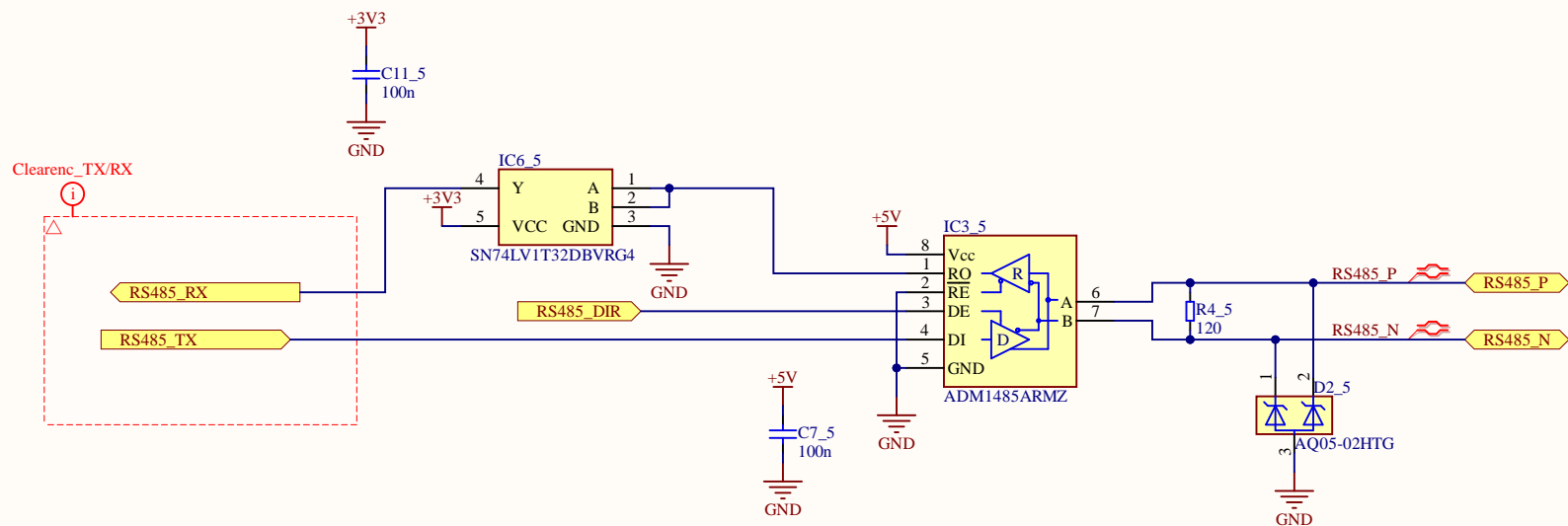
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		File: RS485.SchDoc	



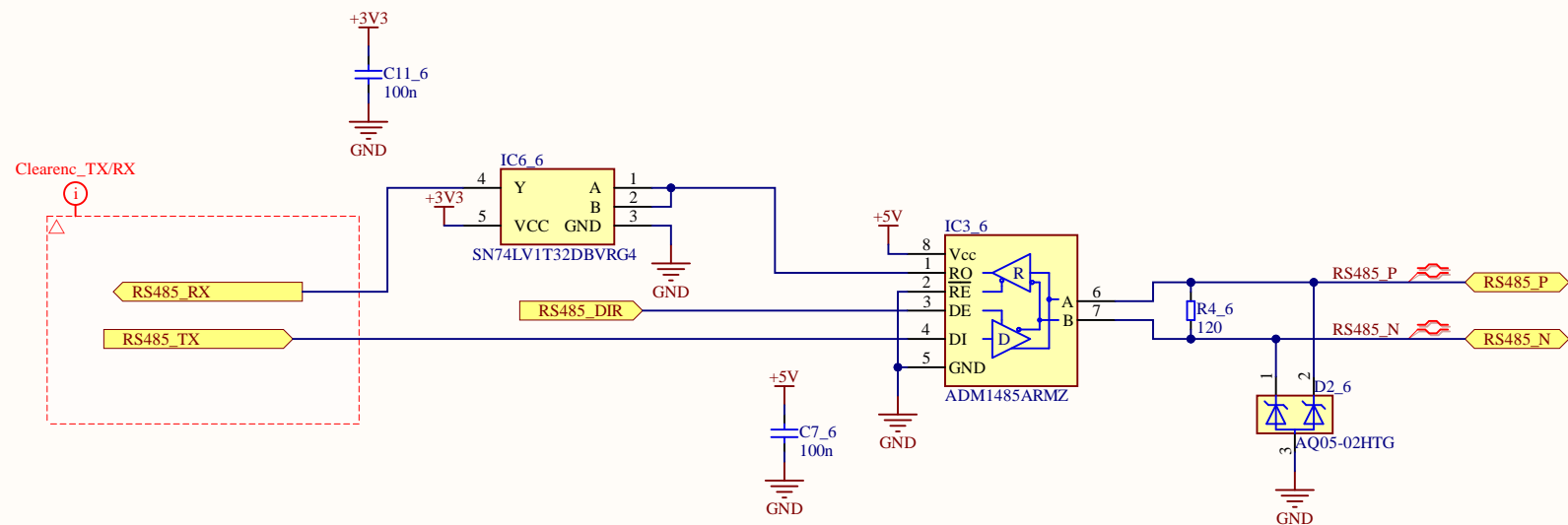
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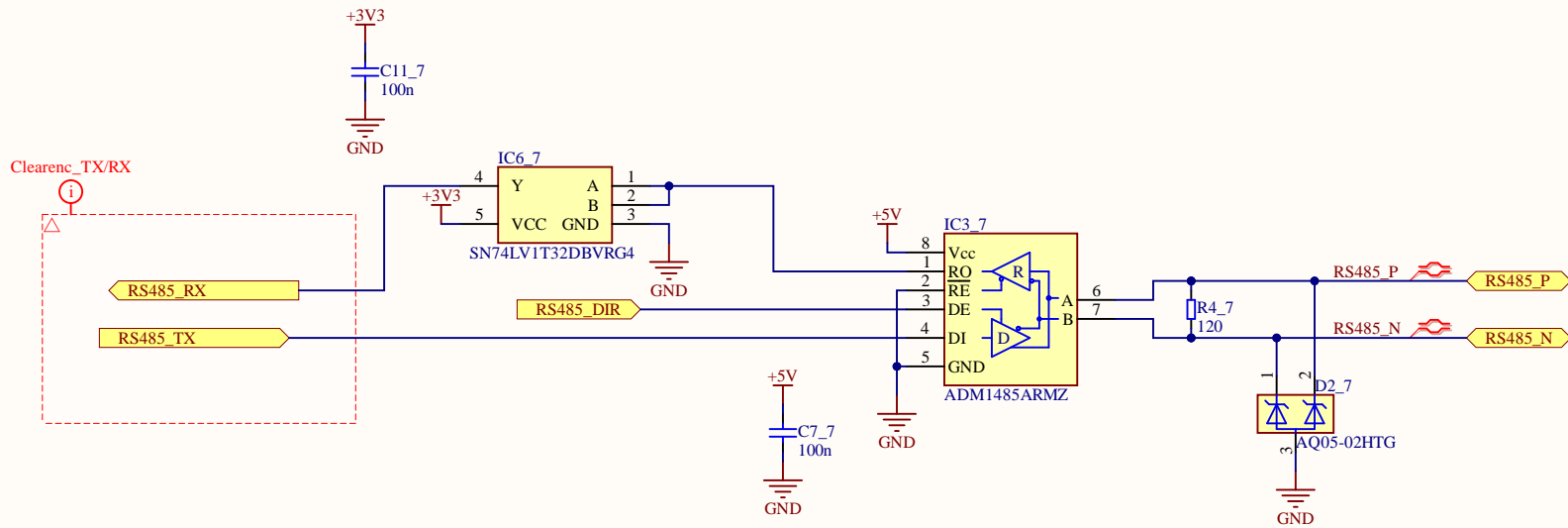
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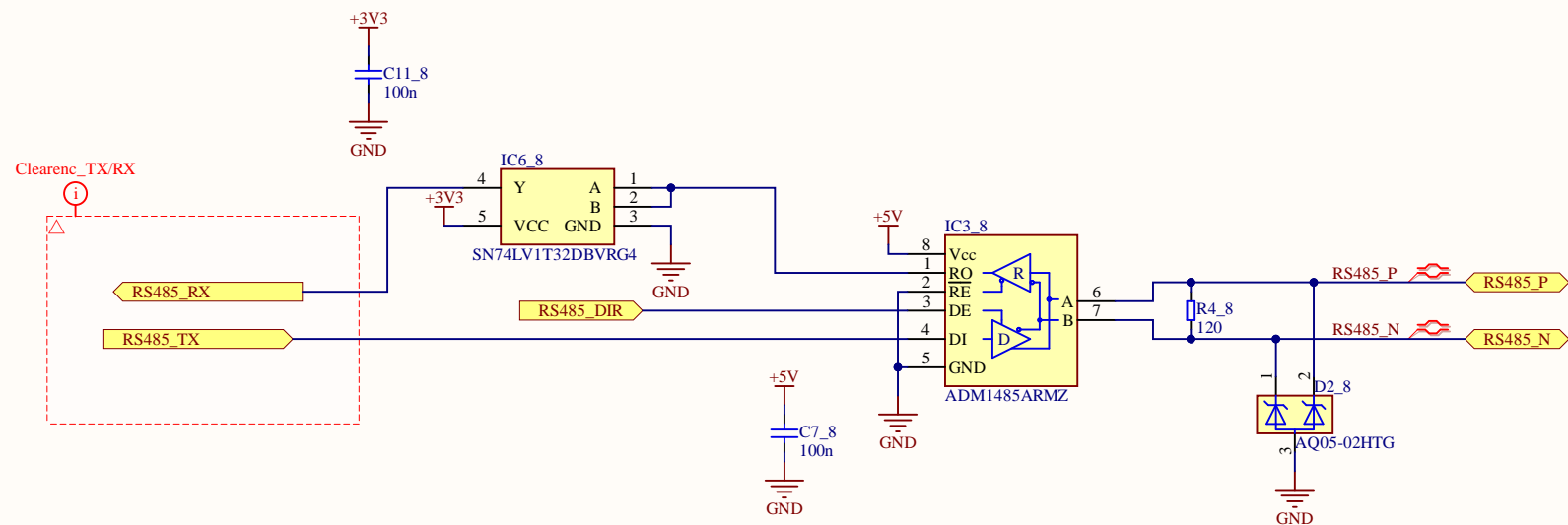
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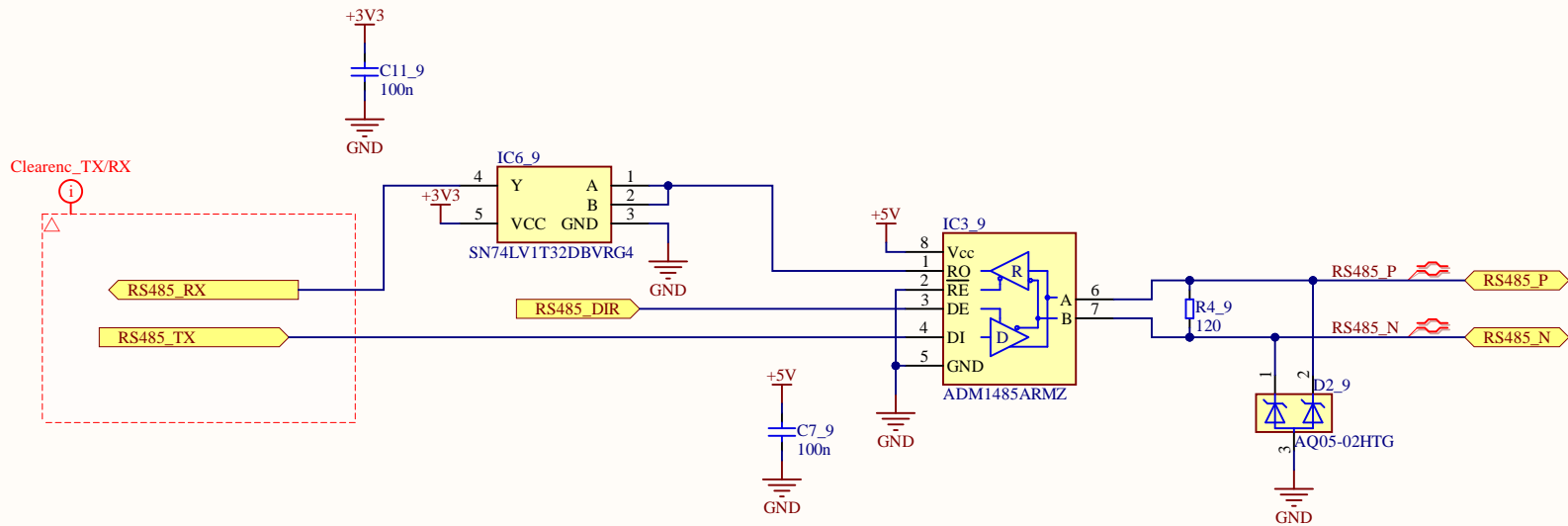
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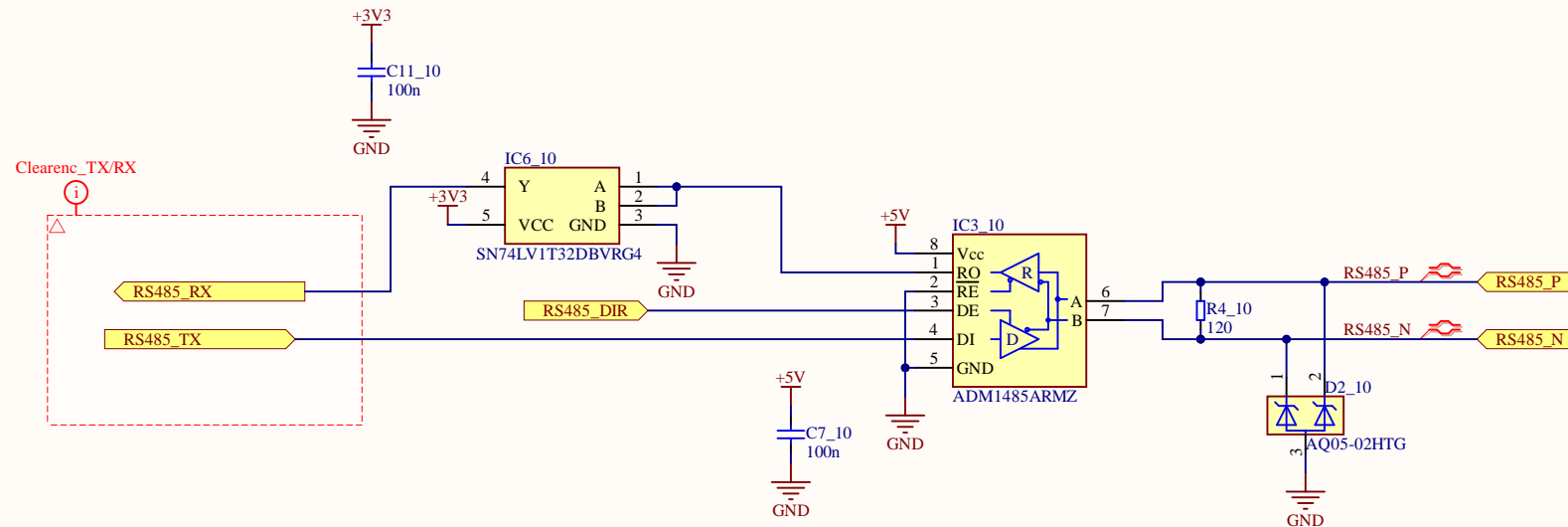
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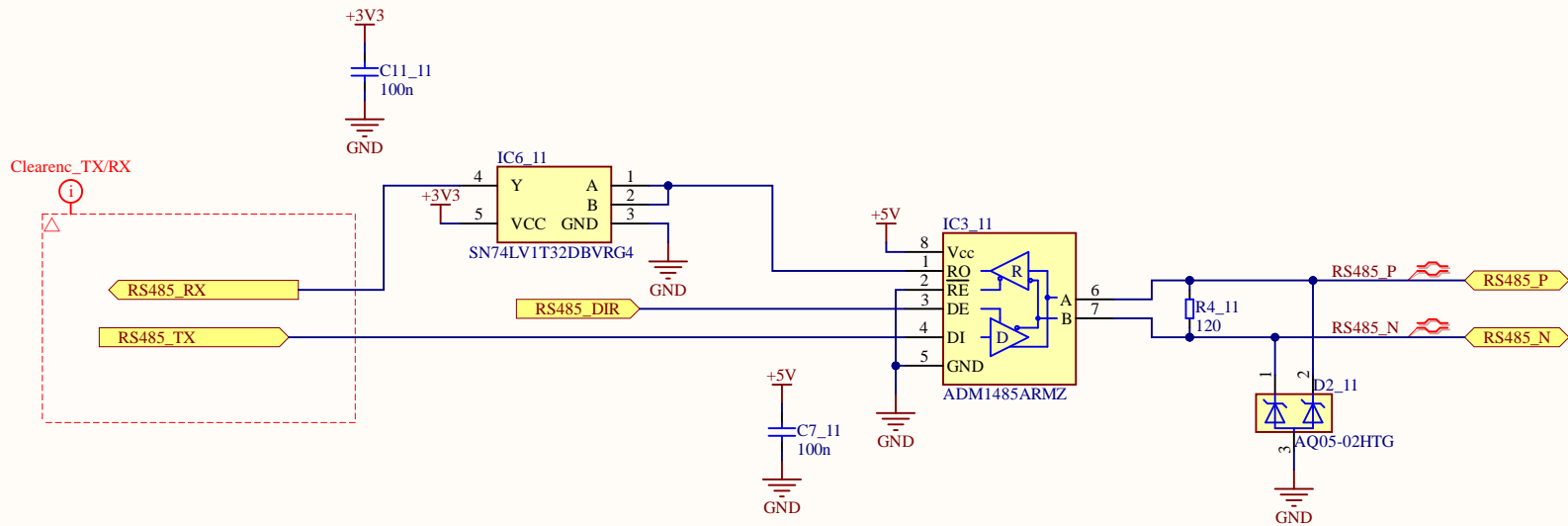
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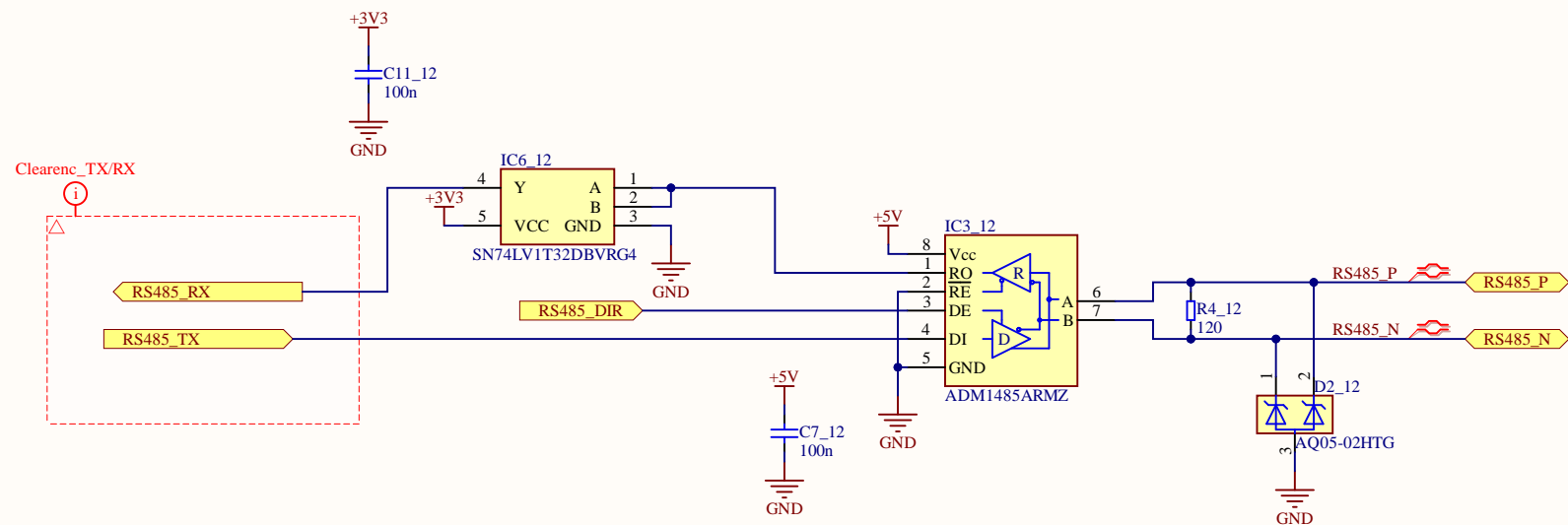
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Author: David Bartůněk	Subtitle: RS485/FPGA	Variant: [No Variations]	
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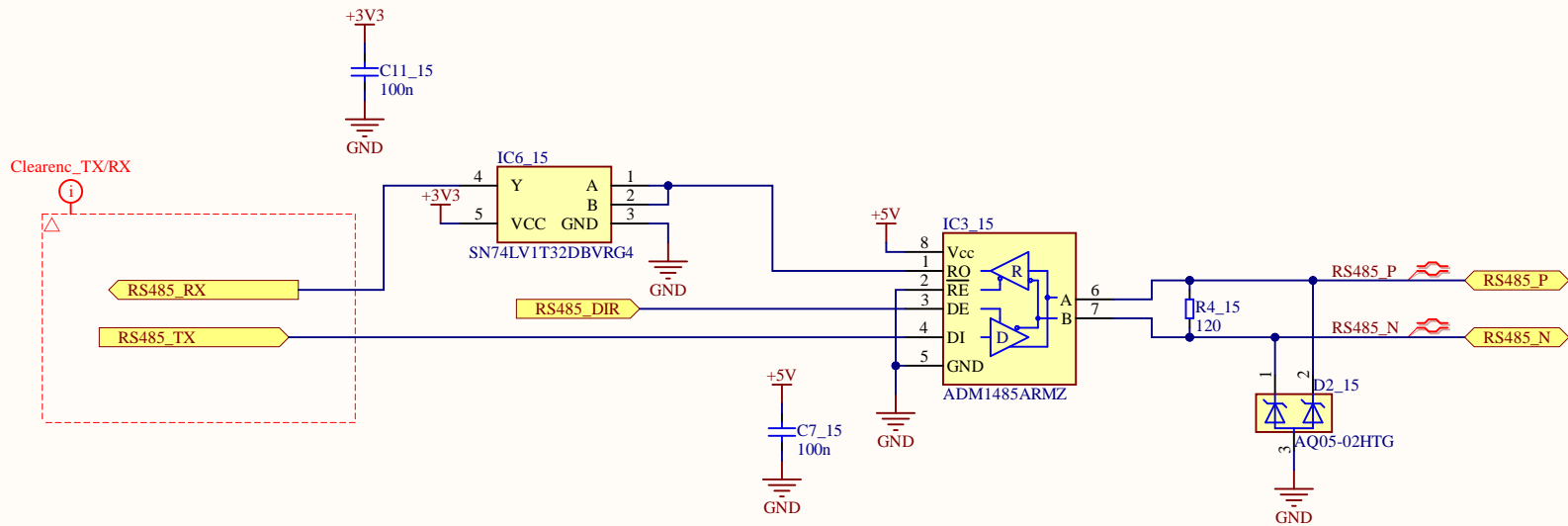


Diplomová práce

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Checked by: David Bartůněk	Nr.: 1	Revision:	
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