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Current Source for the Solid-state LASER Amplifier

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Annotation:
This paper focuses on design of a pulsed constant current source, which should be used for driving a laser diode module used in medicine or LASER spectroscopy. Essentially, it is a multiphase step-down converter with an output switch, driven by FPGA and high-speed current amplifier with A/D converter, which are providing the feedback.

Anotace:
Tato práce je zaměřena na návrh pulsního zdroje konstantního proudu, který lze použít k buzení diodového laserového modulu s účelem využití v medicíně nebo laserové spektroskopii. Jedná se o vícefázový snižující měnič a výstupní spínač, které jsou řízeny prostřednictvím FPGA, rychlého proudového zesilovače a A/D převodníku, tvořících zpětnou vazbu.

INTRODUCTION

The LASER amplifier is one of the most important parts of each LASER system. The amplifier is, easily said, composed of an active medium with semi-transparent mirrors and a source of light. As this source is often used a semiconductor diode. The system requires a high power pulses in very short time in pulse-mode operation.
Similar power sources manufactured by commercial suppliers cost thousands of USD and they have much other disadvantages like unsuitable installation dimensions, poorly adjustable output parameters, high supply voltage and low efficiency. This power source unit (PSU) is designed to enable driving a module with maximum power of 4500 W. Other important parameters are listed below:

- Supply voltage 24 V
- Output voltage 0 - 16 V
- Output current 0 - 550 A
- Output ripple < 1,5 %
- Rise/fall time less than 10 µs
- Maximum pulse frequency 120 Hz
- Pulse width 100 - 300 µs

DEVICE DESCRIPTION

The core of the PSU is a 1200 kHz 10-phase buck converter. The output pulse energy is stored in an input capacitor array. This array is constantly charged by a current source. Once a trigger pulse arrives, the input capacity begins to discharge into the load through the buck, which regulates the output voltage. The phase-shifted PWM is generated by Lattice LCMXO3 FPGA development kit, output parameters can be changed by the RS-485 bus or UART. Bus control is provided by microcontroller, which translates programmed bus commands to values sent via SPI into the FPGA. Next part of the design is a power switch at the output of the buck converter. This switch has to improve pulse edges and inhibit the output when needed.
Because the LASER diode is a non-linear component and its dynamic resistance varies with temperature, the current feedback is necessary. As a suitable solution has been chosen an analog to digital converter (ADC) with 48 MHz SPI bus and 3 Msps sample rate. An input 5th order low-pass filter is added to the ADC for eliminating possible parasitic oscillations.
There is no inductor current sensing in each single phase. Phase current at high loads is being balanced automatically, as described in literature [1]. It is not necessary to do that at smaller currents because all used components are over-rated. As described in [1], the largest source of errors is the PWM, which is precisely generated by FPGA.
The printed circuit board (PCB) is designed with respect to EMI. Next important issue is a parasitic resistance of all power wires, which leads to a voltage drop and power losses. PCB is made of the FR4 with 70 µm copper thickness. Components are cooled by heatsink on the PCB. Some of most current stressed copper areas are unmasked and strenghtened by solder and copper wires.

RESULTS

Assembled board is depicted in Fig. 2. There are visible three IDC headers determined for connecting the FPGA board in the picture.
Tab. 1 contains summary of computed, required and measured parameter values. This design is optimized for driving a nominal load 15 V/300 A [2]. Preliminary tests were carried out with a 150 mΩ

Tab. 1 - Comparsion of theoretical, measured and required parameters

Parameter	Symbol	Theoretical value	Measured value
Propagation delay	T_D	-	140 ns
Rise time	t_r	-	1 µs
Fall time	t_f	-	1 µs
Output current ripple	ΔI_{OUT}	0,01 A	2,05 A
Output voltage	U_{OUT}	6,00 V	5,95 V
Maximum output voltage	U_{OUTMAX}	< 20 V	> 17 V

resistive load at output current 100 A. Selected pulse width was 300 microseconds at 30 Hz. Fig. 1 illustrates a typical output pulse captured by oscilloscope Tektronix TDS2024C.
Results of the preliminary tests are various. Some parameters are met, some are not. Propagation delay is constantly about 140 ns, rise and fall time are about 1 µs. Output voltage has only 1,2 % deviation from the expected value (see full text [3]). Output ripple is greater than the required maximum limit. That is caused by non-zero ESR and ESL of output capacitors and can be corrected by their replacement. Assembled switching transistors (silicon MOSFETs) are not able to drive output at higher frequency than 30 Hz because they run at the edge of their safe operating area (SOA). PWM generator runs always the same phase at the desired duty when triggered, there is no soft-start, and this issue leads to a breakthrough of the most stressed transistor. The soft-start can be firmware-implemented to avoid the described problem.

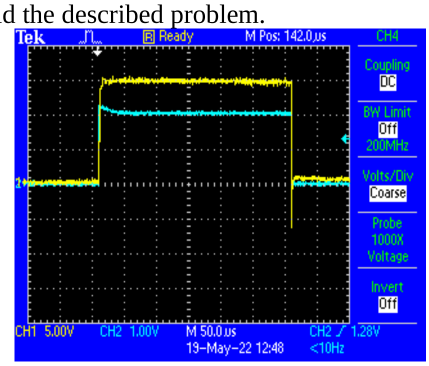

Fig. 1 - Oscillogram of the trigger (blue) and output (yellow) pulse

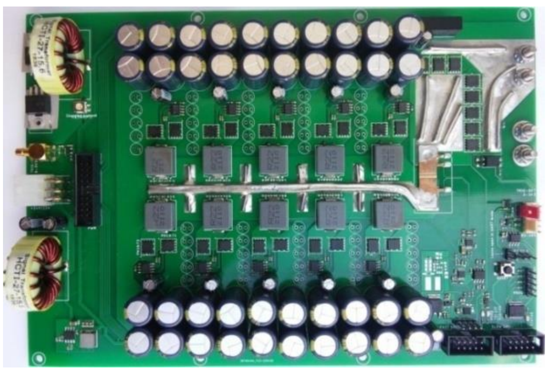
Fig. 2 - Assembled board

CONCLUSION

A high-current pulse current source for supplying a semiconductor diode array was designed. It has to be used in LASER amplifiers in medicine or LIBS. This device works with a 10-phase buck converter driven by FPGA with a current feedback provided by ADC.
Tab. 1 shows a comparsion of required, computed and measured parameters. Preliminary tests were carried out at 15 V/100 A and showed, that timing and output voltage requirements are met, but output pulse rate not. At frequencies higher than 30 Hz the switching transistors are burning.
Future work includes replacement of silicon switching FETs by GaN FETs with appropriate driving circuitry, device size reduction and testing at full load.

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