DESIGN OF THE 1.5 AND 2.5 BIT MDAC – APPLICATION OPPORTUNITIES

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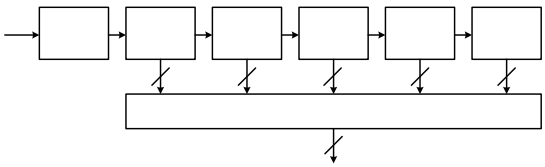
Abstract:
The paper presents design and simulation of the most important stage in pipelined analog-to-digital converter (ADC) so-called multiplying digital-to-analog converter (MDAC). The MDAC with 1,5 and 2,5 bit of resolution were designed using CMOS 0.7 µm technology. The both types of MDAC were compared and the results are also presented. All stages were proposed utilizing Cadence design software.
Příspěvek se zabývá návrhem a ověřením funkce simulací tzv. násobícího převodníku DA (MDAC). Tento převodník je základním blokem každého řetězového převodníku. Násobící převodník DA je obvykle realizován s využitím techniky spínaných kapacitou (SC). Rozlišení je nejběžněji 1,5 bitu, ale může být i vyšší. Tato práce popisuje návrh 1,5 a 2,5 bitové struktury MDAC a porovnává jejich výhody a nevýhody. Celý návrh byl proveden v návrhovém prostředí Cadence v technologii CMOS 0.7 µm.

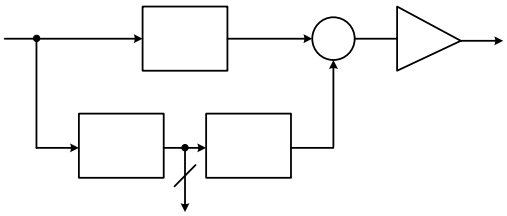
INTRODUCTION

The pipelined ADC became very popular in last few years because of its good parameters (sampling frequency up to tens of MS/s and resolution from 8 to 16 bits), which is widely utilized in many applications i.e. fast Ethernet, xDSL, digital video, CCD imaging, PDA etc [1,2,3].
The pipelined ADC block scheme is shown in Fig. 1 and consists of several stages. There are mainly sample-and-hold input stage (S/H), MDAC, paralel DAC at the end of the conversion chain and time aligning and calibration parts. These parts are usually designed as digital stages.



Obr. 1: The block diagram of the standard pipelined ADC

The MDACs are blocks called Stage 1-4. The MDAC integrates together function of the S/H stage, DA conversion, subtraction and amplifying in one block – Fig. 2. Usually this circuitry is designed using switched-capacitor approach (SC).
The input signal is sampled by S/H stage and concurrently converted by means of parallel subADC as partial output. These data are converted back into the analog representation using subDAC and subtracted from original input signal. The resulting residuum is amplified at the end and sent into the next stage. The resolution of the MDAC varies from 1,5 to 4,5 bits, which depends on application. The half of bit serves for correction purposes.



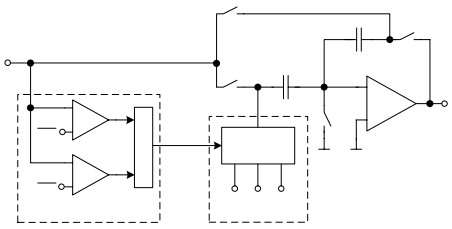
Obr. 2: The block diagram of the MDAC

1.5 AND 2.5 BIT MDAC DESIGN

There are several reasons to use 1,5 bit MDAC in most cases. First, by using the minimum possible stage gain for which the first stage dominates the error performance (A = 2), the bandwidth of the sample-and-hold amplifier is maximized. Second, the use of redundancy a digital correction provides a high immunity to decision errors, allowing the decision process to occur before the amplifier output is completely settled.
The paper compares this MDAC with 2,5 bit MDAC and concludes advantages and disadvantages of both structures.

1.5 bit MDAC

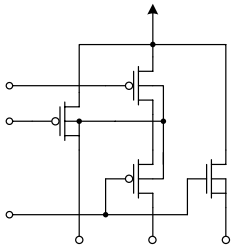
Fig. 3 shows 1.5 bit MDAC using SC technique. The MDAC produces 2 bits output signal, which is sent into the time aligning and calibration stage. One bit is a part of output digital signal and the second part is utilized for calibration. It means that for example 10 bit ADC needs 10 MDACs with 1,5 bit resolution.



Obr. 3: The switched-capacitors 1.5 bit MDAC

The MDAC consists of two comparators and latch – subADC, multiplexer with references – subDAC and amplification stage. The input signal is compared in subADC first. The reference voltage is 1.5 V. The ouput signal D(x-1) is sent into the calibration and time aligning block and it also controls the multiplexer in subDAC. The signals from comparators are directly connected on addressing inputs of the multiplexer and simultaneously decoded into 2 bit output signal.

Thanks to this design the multiplexer is realized as simple circuit and the stage is insensitive against hazards. The proposed multiplexer is depicted in Fig. 4 and the function of the subADC and subDAC describes Tab. 1.



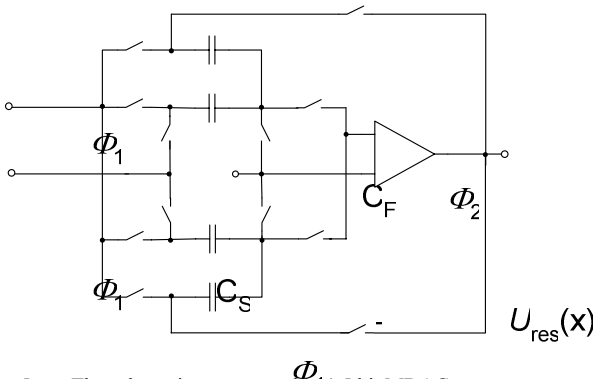
Obr. 4: The proposed multiplexer for 1.5 bit MDAC

Tab. 1: The function of the subADC and subDAC

input signal	comparators outputs				output code		sub-DAC output
$u_{res}(x\text{-}1)$	N1	N2	N3	N4	A_1	A_0	u_{DAC}
$u_{res}\,(x\text{-}1) > U_{ref}/4$	1	0	1	0	1	0	4 V
$U_{ref}/4 > u_{res}\,(x\text{-}1) > -U_{ref}/4$	0	1	1	0	0	1	2,5 V
$-U_{ref}/4 > u_{res}\,(x\text{-}1)$	0	1	0	1	0	0	1 V

The last stage in the MDAC is subtracting block using SC technique – Fig. 5. The output is

$$u_{res}(x) = u_{res}(x-1) - u_{DAC} \quad (1)$$



Obr. 5: The subtracting stage used in 1,5 bit MDAC

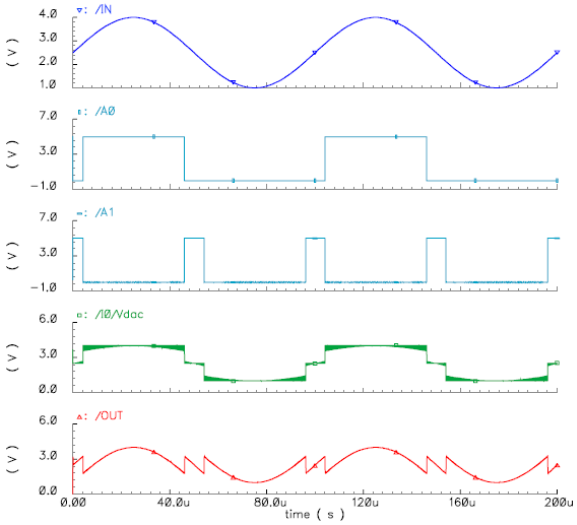
The output residuum of the stage is

$$\left(2+\frac{C_S}{C_F}\right)\cdot u_{res}(x-1) - U_{ref} \quad \text{if } u_{res}(x-1) > \frac{U_{ref}}{4}, \quad (2)$$

$$\left(1+\frac{C_S}{C_F}\right)\cdot u_{res}(x-1) \quad \text{if } -\frac{U_{ref}}{4} < u_{res}(x-1) < \frac{U_{ref}}{4}, \quad (3)$$

$$\left(2+\frac{C_S}{C_F}\right)\cdot u_{res}(x-1) + U_{ref} \quad \text{if } u_{res}(x-1) < -\frac{U_{ref}}{4}, \quad (4)$$

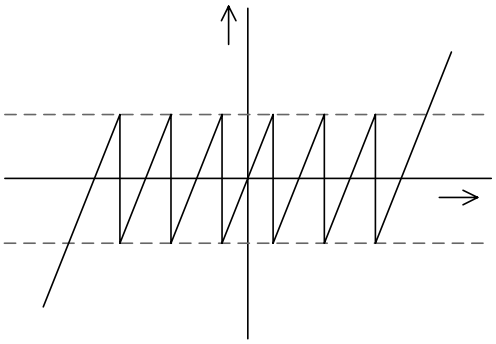
The results made for the 1,5 bit MDAC confirm the calculations and design. They are shown in Fig. 6. The power consumption is 2,5 mW.



Obr. 6: The simulated function of the 1,5 bit MDAC

2.5 bit MDAC

This MDAC is more complicated. It consists of six comparators, amplifier and SC block. The transfer characteristic is shown in Fig. 7.



Obr. 7: The transfer characteristic of the 2,5 bit MDAC

As can be seen, the input signal is compared on six comparators with reference voltages of ± 5/8 U_{ref}, ± 3/8 U_{ref}, ± 1/8 U_{ref}. The 3 bit output signal is sent into the calibration and time aligning block and it addresses three multiplexers. The function of the proposed subADC and subDAC is described in Tab. 2.

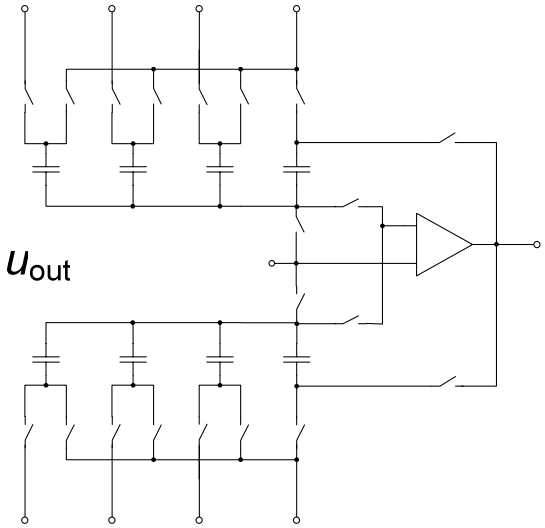
Tab. 2: The function of the subADC and sub DAC

input signal	output code			sub-DAC output		
u_{res} (x-1)	A_2	A_1	A_0	u_{DAC3}	u_{DAC2}	u_{DAC1}
u_{res} (x-1) > 5/8 U_{ref}	1	1	0	4 V	4 V	4 V
5/8 U_{ref} > u_{res} (x-1) > 3/8 U_{ref}	1	0	1	4 V	4V	2,5 V
3/8 U_{ref} > u_{res} (x-1) > 1/8 U_{ref}	1	0	0	4 V	2,5 V	2,5 V
1/8 U_{ref} > u_{res} (x-1) > -1/8 U_{ref}	0	1	1	2,5 V	2,5 V	2,5 V
-1/8 U_{ref} > u_{res} (x-1) > -3/8 U_{ref}	0	1	0	2,5 V	2,5 V	1 V
-3/8 V_{ref} > u_{res} (x-1) > -5/8 V_{ref}	0	0	1	2,5 V	1 V	1 V
-5/8 U_{ref} > u_{res} (x-1)	0	0	0	1 V	1 V	1 V

The last stage of the 2,5 bit MDAC realises the operation

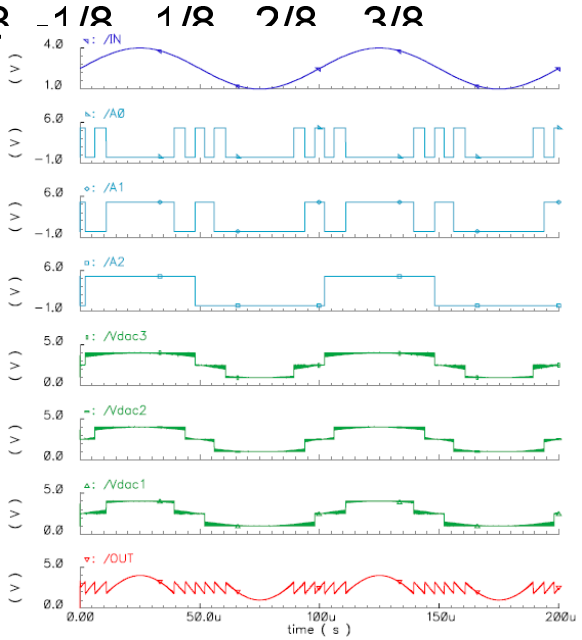
$$u_{res}(x) = u_{res}(x-1) - \frac{(u_{DAC3} + u_{DAC2} + u_{DAC1})}{4} \quad (5)$$

Fig. 8 shows the designed subtracting block.



Obr. 8: The subtracting stage used in 2,5 bit MDAC

The simulation of the MDAC also confirms the correctness of the design – Fig. 9. The power consumption of the 2,5 bit MDAC stage is 4 mW.



Obr. 9: The simulated function of the 2,5 bit MDAC

CONCLUSIONS

The paper shows pros and cons of usage of the 1,5 bit and 2,5 bit MDAC in pipelined ADC. It is clear, that 1,5 bit structure is very simple circuitry, but higher number of these stages have to be used to obtain the same resolution of ADC as 2,5 MDAC.

Let conclude the pros and cons of designed structures.

1,5 bit MDAC

+ only two comparators without correction necessity,
+ small chip die,
+ simple structure of the subADC and subDAC,
- more stages are needed in the ADC with the same resolution,

2,5 bit MDAC

+ half number of the stages in the ADC,
- more comparators with higher accuracy, the correction of the offset is needed,
- the operational amplifier with high bandwidth,
- more complexity of the subADC and subDAC.

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