



NanoLab System for NanoElectronics and Sensors

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Abstract:

Aim of this work is to study and to realize new structures for nanoelectronic devices and for sensor applications. The idea is to start from a basic nanostructure for electronic devices, nanogaps, to generalize its concept for the implementation of a general complete system, built starting from the nanostructures up to user interfaces and experiment management, for the realization of nanodevices. This solution wants to give to researchers the opportunity to work on their specific application and to have an already prepared working base, ready to be customized for the specific design needs.

INTRODUCTION

The idea of this project is to develop a novel system starting from the realization of nanogaps in which authors have a matured experience [1-4], and because they are a very interesting application, useful in several application areas as nanoelectronics or sensor devices. In fact, together with other solutions, they represent interesting approaches to find new technologies to solve the limitation of CMOS processes. They can be used in molecular electronics [5-7], but also in sensor devices, exploiting nanostructures to detect molecules having comparable dimensions ([8]-[11]). The presented approach for fabrication of nanogaps is based on the use of gold probes and Electromigration Induced Break Junction (EIBJ) technique [13-17].

In Fig1 is showed the idea of the complete system, composed of its different parts that can be summarized as:

1. The NanoLab, the core of the system, where are present areas devoted to host the realization of custom nanostructures (called NanoLab Elements - NLEs), in our case the gold probes in which will be built the nanogaps. In these areas will be present already pre-built interconnections and first electronic stages, mainly for pre-amplification of signals;
2. The Signal Conditioning and Interfaces, for input/output generation. This section is composed with a custom board developed for the specific experiment and for signal conditioning interfaces. This board is interconnected to a Linux Embedded system

useful for high level operations and for implementation of control algorithms. Embedded system is also used for interfacing the system to the Control Station;

3. The Control Station, on which user interfaces are present and that is interconnected via a wireless channel to the Embedded System, so the experiment can be remotely controlled.

With this system is possible to control in a first step the processes for construction of the nano/micro devices in the NanoLab, then to manage the experiments that will use them. In this way is obtained a solution that can be extremely compact. The chip with the NanoLab can be inserted in a controlled environment and then all the different steps can be realized without manipulations, avoiding risk of contaminations and improving processes yield. In presented work nanogaps structures were built, studying the processes of device fabrication and some different geometries to find the optimal possible solutions.

THE NANOLAB AND THE NLES

The NanoLab structure is based on a bidimensional array of elements designed to support a large number of experiments both for the nanoelectrodes fabrication and for the measurement of molecular devices.

The common technological process for the NLE fabrication is based on a silicon dioxide layer with a thickness of 230 nm, grown on the silicon wafer. After surface activation in an oxygen plasma and hydroxylation, the thermal silicon dioxide layer is

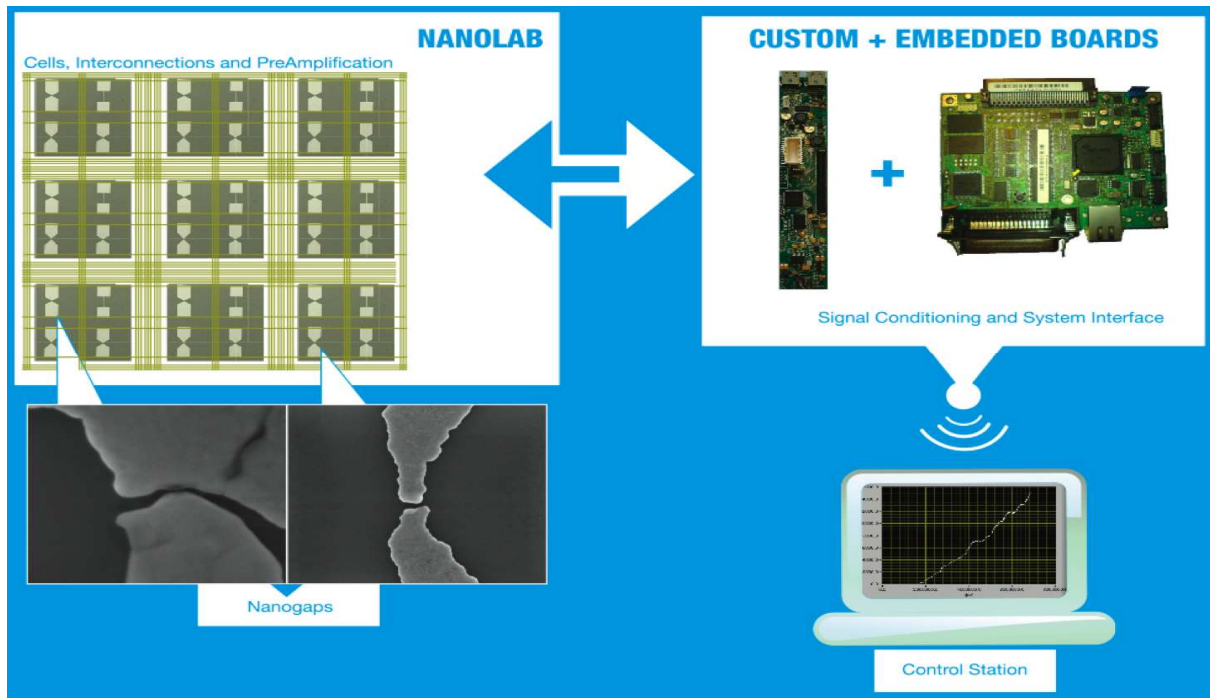


Fig.1: the Nanolab System

Then silanized with (3 – Mercaptopropyl) trimethoxysilane (MPTMS) working as self-assembly adhesion monolayer. MPTMS molecule solves the problem of using metallic promoters for gold deposition, as titanium or chromium. With this solution is so possible to have good adhesion, but not other metallic, and so conductive, parts, because for electromigration control it is important that the current flows only in the gold layer. Then, a gold thin film with a thickness of 25 nm is deposited by means of an electron beam evaporation.

The geometry of the gold electrodes (Fig. 2) is defined to support different fabrication techniques:

- Electromigration (EIBJ)
- Field Emission Electromigration (FEE)
- Electrodeposition with Crono-Potentiometry (ECP)
- Electrochemical Etching (EE).

Nanogap fabrication based Electromigration Induced Break Junction (EIBJ) technique had been largely experimented by authors ([1]-[4]). To obtain reproducible and stable devices it is very important to control the width of the generated nanogap. For this reason in EIBJ the currents used to stimulate the electro-migration effect must be controlled using a feedback algorithm, where the resistance measurement and a thermal estimation are used to avoid thermal runaway. So it is important to have a control system where it is possible to control the experiment and where to implement the necessary algorithms to, in this specific case, manage stimulus signals and to analyze signals received from the NLEs for obtaining nanogap creation.

When the gap dimensions become few nanometers, the tunnel current can be measured to estimate the final dimension. In fact, even if an accurate measure of the gap dimension can be obtained only by FESEM or AFM analysis, the tunnel current can be used to give a first evaluation of the yield of the fabrication process. Moreover, when the dimension of the gaps is larger than the expected value, increasing the applied voltage on the electrodes a Fowler-Nordheim Field Emission activation of the metal ions can be induced. This kind of electromigration (FEE) can be applied to the nanogaps to narrow the gap ([18]-[19]) with high accuracy since the tunnel resistance can be measured and used to control the process: the process is stopped when the tunnel resistance becomes some MΩ. Both EIBJ and FEE require a NLE structure like that shown in Fig. 2a) where the geometries are designed to control the temperature profile in the wire during EIBJ.

Besides the EIBJ and FEE techniques the use of a gold geometry as shown in Fig. 2b) can be used to electrochemically prepare electrodes. A solution of KAu(Cn)_2 with $\text{K}_3\text{C}_6\text{H}_5\text{O}_7$ and KH_2PO_4 is used as electroplating electrolyte.

In particular, the deposition is controlled by a feedback algorithm based both on the electrolyte conductance and the tunnel current measured while the gap is narrowing.

Since the initial gap in the NLE for this kind of technique is created by photolithography, the dimension is about 1 μm; to reduce the required electrodeposition time, the deposition rate at the beginning of the process must be higher than during the final part, where the rate must be reduced to increase the control on the final dimension of the Nanogap.

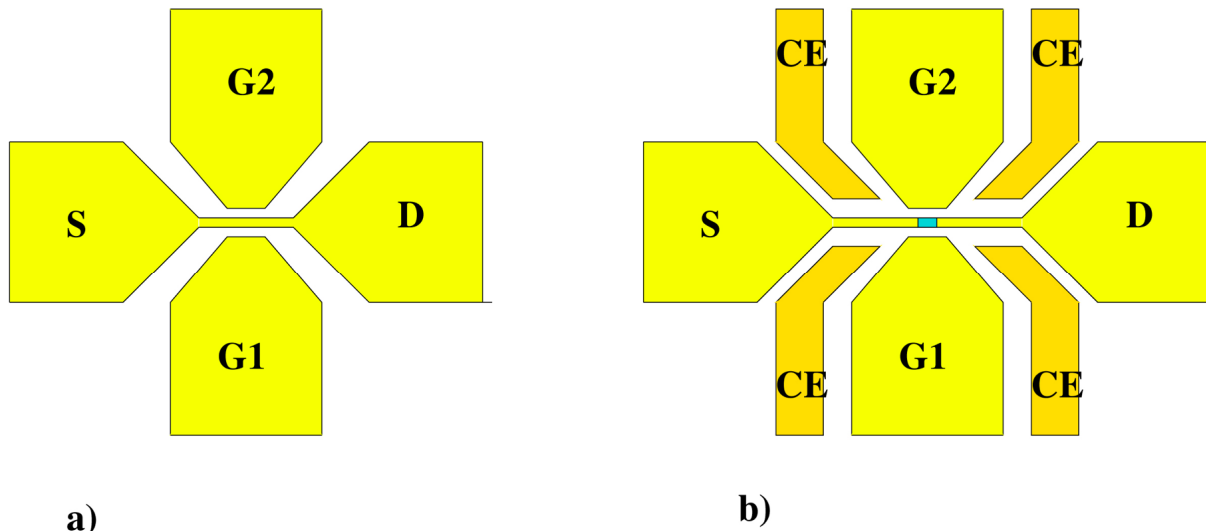


Fig. 2: the NanoLab Element structure.
a) Metal geometries used for EIBJ and for FEE
b) metal geometries used for ECP and for EE

This step is a classical technological process for new nanoelectronics approach, where a liquid phase is needed to produce the required devices. For this reason a microfluidic structure has to be realized for having a fluidic interconnection between NLEs and for allowing inlet and outlet channels for management of reaction liquids or, more generally, fluids. The layout of his fluidic structure has to be designed for having a correct access of fluids to the microchambers in terms of quantity, but also considering the fact that, for doing in parallel the construction of nano/micro devices, fluidic paths must be similar in length and characteristics for all NLEs.

During the fabrication process in the NLE the S terminal is used as working electrode, the D terminal as reference electrode and the four fingers designed around the microwire as counter electrode.

This technique, described in [20] and [21], can be realized by using the NanoLab standard experimental setup, where the potentiostat and the feedback algorithm are implemented by the Signal Conditioning and Interfaces block of the NanoLab System. The real time monitoring of the deposition process can be performed by using the conductance measurement of the gap and for the fine control of the final dimension the measurement of the tunnel current can be applied. This experimental setup can be also used in a reverse condition where the gold on the working electrode can be removed by electrochemical etching making possible a procedure where the nanogap dimension can be adjusted.

The possibility to implement electronic functions by mean of molecular FET had been demonstrated by some authors in [22] and [23]. The gate structures must be compatible with the fabrication of Metal-Molecule-Metal junction. In the planar gate structure showed in Fig. 2 it is possible to apply a potential between G1 and G2 terminals, so the resulting electric field will influence the Molecular Orbital

Energies and I-V characteristics of the molecular junctions. The main problem of this affordable technology is the low gate coupling with the molecule, and the weak control of the molecule conductivity; this is mainly due to the distance between the two gate electrodes. A possible solution that can be implemented is reducing the distance between G1 and G2 by electrodeposition, using alternatively these two electrodes as WE. Moreover the availability of a planar gate few nanometers from the M-M-M junction makes possible some relevant experiments for the development of new device architectures: if molecules with localized charge are bound on the gate electrodes, the interaction between conducting molecule inserted in the nanogap and the molecules bound to gate electrodes can be measured in terms of influence on I-V characteristics. In this case the G1 and G2 electrodes in Fig. 2 work just as support to the charged molecules and they are not used to apply an external voltage.

CONTROL STATION AND SIGNAL CONDITIONING

To control the experiment a micro structure is realized for management of the signals in and out of NLEs and, after a first interface directly realized on silicon surface, the device is connected to a custom electronic board then to a Linux Embedded system, in which are described the algorithms and the procedures for controlling the nanogap fabrication. The schematic of the custom board is showed in Fig. 3, where it is possible to see that the gold probe is driven by a circuit that receives the signal from the Embedded Linux (Analog Input) and generates the desired current for inducing electromigration. The current in the probe, and so the resistance, is measured and it is sent to the Embedded Linux in which are implemented the algorithms for controlling the injected current into the probe. In this way the

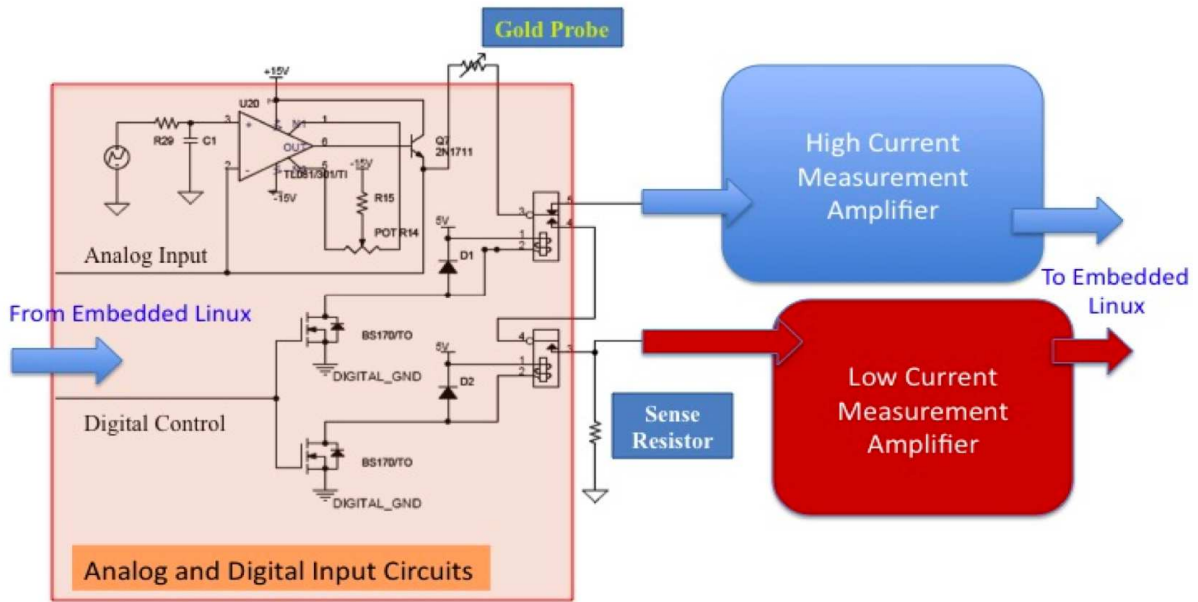


Fig. 3: schematic of control board for nanogap fabrication

fabrication of the nanogap is controlled, avoiding for example thermal runaway that can create breaks, but uncontrolled and too large, not useful for the desired applications.

Realised circuits have to drive the micro wire with a controlled bias voltage supplying a maximum current of hundreds of mA. The front-end must also be able to measure the real time current flowing in the wire to evaluate resistance variation: are schematically showed the two stages, automatically controlled, that are able to measure currents ranging from hundreds of mA (when the current is high and the break is not yet created) to some nA (for measuring the tunnel current inside the nanogap) with a good resolution.

Applying EIBJ technique, a software controlled voltage step-ramp was applied to the wire, monitoring the real-time resistance to implement an effective feedback algorithm. Control algorithm uses the information provided by the electrothermal model to control the temperature of the micro wire and to keep the conditions favourable to nanogap formation.

A first relevant result is related to control algorithm: if the feedback in the control is not used, generally thermal runaway destroys the wire and any calibration of the input waveform does not improve results.

Nanogap fabrication begins with a low voltage DC measurement, used to estimate the total resistance of the wire. Since probe and access pad resistances are well known, an initial bias voltage is evaluated to force a defined initial current density in the wire: in our case the standard cross section of wires is approximately $0.025 \mu\text{m}^2$ and a current of 25 mA

produces a current density of $108 \text{ A}\cdot\text{cm}^{-2}$. This

current density can be considered a threshold value for electromigration process.

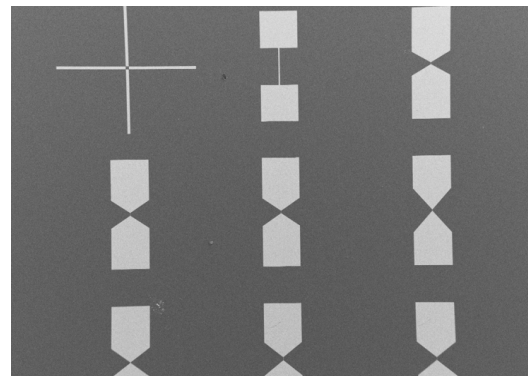


Fig. 4: test probe structures

RESULTS

Different structures have been produced (Fig. 5), while studying the behavior of nanogap generation in several geometries. Different shapes of the two terminals have been implemented to obtain two examples of thermal resistance profiles. The two most interesting are reported in Fig. 5: type 1 and type 2 probes. In the first (type 1), the metal wire directly interconnect pads, while in the second shape (type 2)

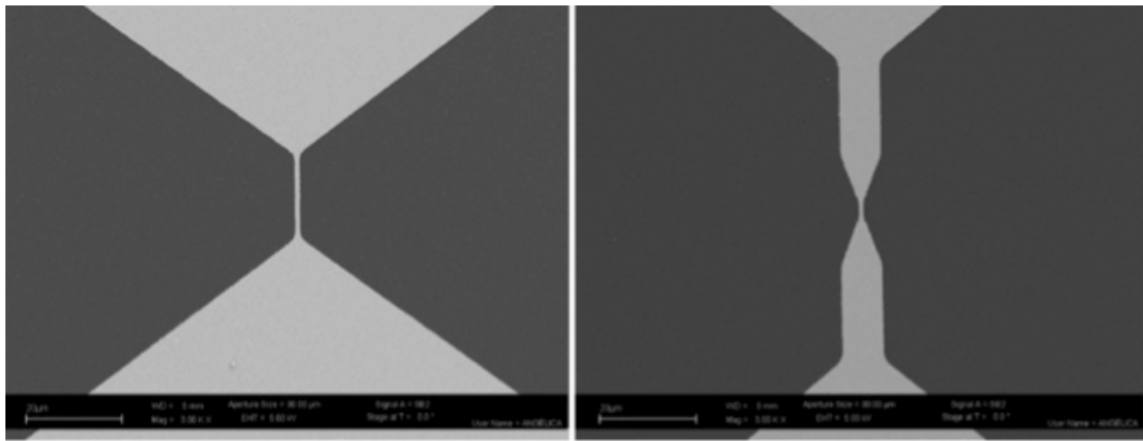


Fig. 5: type 1 and type 2 probes

the wire has two different widths, so thermal resistance is not constant in the interconnection. Structures with different dimensions have been produced for each of two terminal types.

In Fig. 5 are showed a type 1 structure with a width of $1\ \mu\text{m}$ and a length of $15\ \mu\text{m}$ and a type 2 structure with a larger connection of $8\ \mu\text{m} \times 25\ \mu\text{m}$, while thinner one is $1\ \mu\text{m} \times 4\ \mu\text{m}$. Type 1 structures demonstrated a more straightforward management of nanogap generation. The reason of this behavior is due to the temperature that in type 1 structures is more controllable and this fact is a confirmation of the tight interconnection between thermal and electromigration effects.

Several structures were obtained and one of the produced nanogaps is reported in Fig. 6 where are showed images obtained using or a FESEM or an AFM microscope for having all the possible information about nanogap structure.

As it can be observed in Fig. 6, the nanogap created between the two terminals has different widths, but the ones of interest are those with the desired dimensions, while are specific for the application or for the sensing technique. In this first work the control of the nanogap width was not very specific and so the control part has to be improved, including an electro-thermal model in control loop.

Very interesting results were obtained mapping the behavior of current and resistance in the probe.

An example of these results during nanogap creation is showed in Fig. 7. As can be seen, when the voltage increases, the current flowing through the two terminals decreases and resistance value increases.

The reason of this increase in resistance does not indicate that we are producing the nanogap, and so breaking the structure, but is generated by thermal effects.

For this reason it is important to control the stimulus sent to the probes, in fact controlling the behavior of the resistance gives the possibility to produce nanogaps with desired dimensions. In applied algorithm the control reads the current from the two terminals, calculates the resistance and continues to increase voltage if the resistance does not increase of a predefined percentage (a good value can be 5%). The reason of this type of management is that the voltage cannot be increased without control, in fact the wire can melt, making this technique not suitable for nanogap fabrication. In this case break dimensions would be unpredictable and generally much wider than requested ones. To avoid this thermal runaway the algorithm removes the bias voltage for ten seconds, and restarts the procedure from a reduced bias voltage to keep the estimated maximum current density to the predefined value. The process continues up to a point where is clear that the resistance increasing is due to electromigration breaking, and not to thermal effects.

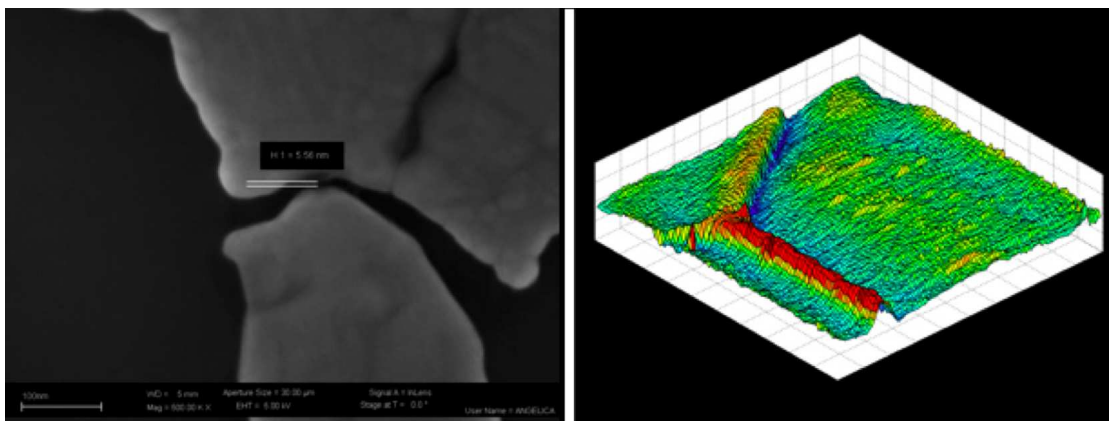


Fig. 6: FESEM and AFM image

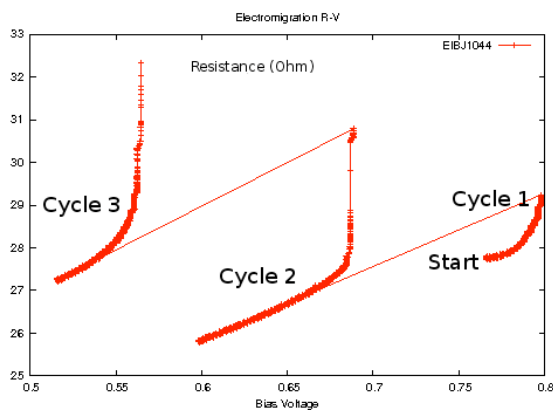


Fig. 7: Probe resistance plot during nanogap creation

CONCLUSIONS

A complete approach for management of nanostructures has been presented and future works will be done for building the final system, now realized in some parts. Starting from the fabrication of nanogaps, the control structure has been implemented and good results were obtained in creating some nanogap structures. In this case future activities will be the optimization of the control of nanogap fabrication and in the exploitation of these structures for building new devices and sensors.

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