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Global Simulation Model Design of Input-Serial, Output-Parallel Solid-State Transformer for Smart Grid Applications

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Abstract: This paper provides an overview of an early attempt at developing a simulation model on a solid-state transformer (SST) based on input-serial and output-parallel (ISOP) topology. The proposed SST is designed as a base for a smart grid (SG). The paper provides a theoretical review of the power converters under consideration, as well as their control techniques. Further, the paper presents a simulation model of the proposed concept with a PLECS circuit simulator. The proposed simulation model examines bidirectional energy flow control between the medium-voltage AC grid and DC smart grid, while evaluating power flow efficiency and qualitative indicators of the AC grid. After the completion of design verification and electrical properties analysis by the PLECS simulation models, the synthesis offers recommendations on the optimal layout of the proposed SST topology for smart grid application.

Keywords: smart grid; control strategy; power semiconductor converter; solid-state transformer; simulation; PLECS; hardware in the loop

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1. Introduction

The idea of solid-state transformers (SSTs) has evolved in recent years in a variety of disciplines, including smart grids. It is a promised crucial element for future smart grids [1]. SSTs are expected to replace conventional low-frequency transformers in the smart grid because they provide efficient and more controlled bidirectional power flow control options, as well as the ability to implement functions such as reactive power compensation, short-circuit current limitation, power factor correction, harmonics compensation, voltage drop compensation, and voltage drop compensation to the distribution network as input and output frequency variability [2]. Future smart grid design and research are focused on improving the reliability, efficiency (loss reduction in smart grids), and quality of distributed power, such as short outages or prevention of voltage fluctuations [1,2]. However, SST has several drawbacks that have not yet resulted in its replacement of conventional transformers. The expense of SST in comparison to a traditional low-frequency transformer is one of the most significant drawbacks. To manage the power flow in SG, the SST requires high-voltage, high-power semiconductor switching devices. When compared to a standard transformer, it has lower efficiency and increased complexity and produces more electromagnetic interference. The efficiency can further be balanced by lower losses in the superior network, thanks to the automatic compensation of reactive energy and an overall neutral power factor.

However, due to the drawbacks of commercial transformers and the inherent benefits of SST, research in this field is presently primarily focused on the implementation and usage of SST in smart grids [3].

The growing prevalence of renewable energy sources (such as solar panels and wind turbines), energy storage devices (such as batteries and electric vehicles), and high-current loads (such as electric vehicle chargers) make power distribution networks operational [4].

The residential smart grid concept proposed in this article is based on a three-tier SST topology. The three-level SST topology is the most commonly chosen topology in research due to the intelligent properties and control strategies offered [4]. This research also proposes the HIL simulation model of proposed SST architecture. The PLECS simulator is being used to model the circuit description of the planned SST's individual stages.

2. Materials and Methods

Currently, the most widespread is the use of a low-voltage AC supply (LVAC) for powering appliances in residential networks, although a large proportion of the devices currently in use does not require AC power to function. Most commercial and consumer devices today have a DC intermediate circuit (consumer and office electronics, switching power supplies and chargers) or can work directly on both AC and DC networks (lighting and heating technology, universal electric motors). From the point of view of energy within the microgrid, the use of a low-voltage DC supply (LVDC) to directly power consumer devices appears to be a beneficial solution. In the case of DC sources (photovoltaics, battery storage), working directly into the DC network, the min. one DC/AC transformation stage and the energy efficiency of the system as a whole increase.

The common block diagram of a SG is illustrated in Figure 1. In this paper, it is assumed that the proposed concept will supply a group of local smart homes that are connected to a micro-grid. The LVDC bus is a base for the micro-grid. In addition, the MVDC (medium-voltage DC) bus can be used to connect renewable energy sources, an energy storage system, or a DC high-voltage EV charger to the proposed concept of SG with SST [5]. This approach is attractive because it allows more precise and effective power flow control.

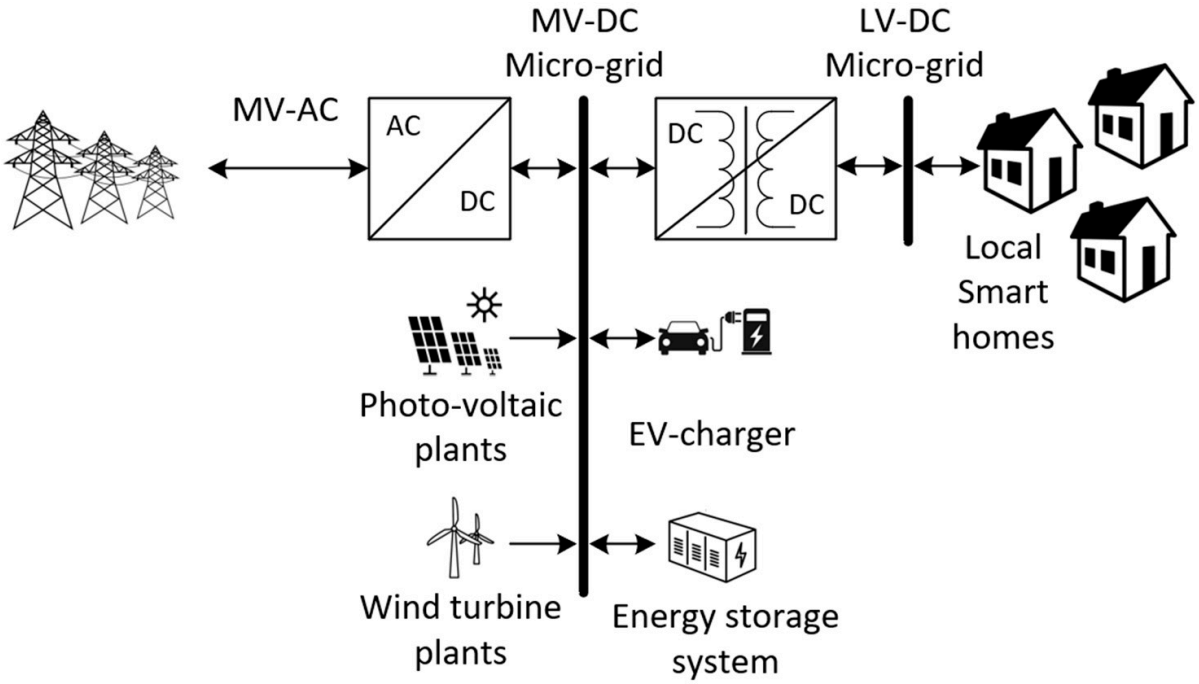

Figure 1. Illustrative block diagram of future SG for local residences.

There are several SST topologies classified as one-tier, two-tier, and three-tier. In many SST topologies, DC or AC inputs can be converted to DC or AC outputs by changing some or all of the switches [6].

The three-stage topology is the most popular in research compared to other topologies because it offers effective power control properties [7]. In addition to reducing volume and weight, this SST can also improve the performance of distribution and transmission grids [8]. Additionally, the three-layer SST design provides on-demand reactive power support for grid, power quality, current limiting, storage management, and dual DC buses [7].

2.1. Medium-Voltage (MV) Stage of SST

Generally, the medium-voltage (MV) distribution network is the main power source for SGs. Standardized voltages used in medium-voltage distribution networks are often 10 kV or higher [9], so a multi-level topology for the first stage (medium-voltage side) of the SST is preferred when using ordinary silicon-based semiconductors [10–12].

For SST applications, many multilevel converter topologies have been proposed. Furthermore, given the needed number of levels, even at the lowest voltages, the selected design must deal with several critical issues, such as capacitor voltage balance and sophisticated control techniques. Table 1 summarizes possible SST MV-stage topologies in SG [8].

Table 1. Potential medium-voltage-stage topologies and control algorithms for SST in SG [8,10–12].

Topology	Advantages	Disadvantages
Cascade H-Bridge	Simple control strategy and simple voltage balance control Modularity	Unachievable MVDC link
H-bridge NPC	Lower number of semiconductor switches	Complex control strategy with voltage balance control Limited modularity
Multilevel Active NPC	Modularity	Complex control strategy with voltage balance control High amount of clamping diodes
Modular Multilevel Converter	Modularity	Complex control strategy with voltage balance control
Control algorithms		
Phase-Shifted PWM	Simple control: carrier pairs are assigned to individual cell	Higher losses
Level-Shifted PWM	Improved harmonic cancellation	

2.2. Isolated Stage of Solid-State Transformer

The low-voltage DC link is the base of a local residence's microgrid. The microgrid voltage is set to 600 V [13]. For stepping down the MVDC bus voltage to a reliable voltage level, an isolation stage is implemented [7]. Table 2 summarize the possible topologies for the isolation stage of SST in SG applications [8].

This stage is considered one of the most difficult because it requires a lot of power to balance the high current on the low-voltage side and the high voltage on the medium-voltage side. There are two ways to meet the requirements. One is the use of HV-rated semiconductor devices, and the other is a modular approach, in which many modules are cascaded together to share all power, voltage, and current [14,15].

The modular approach has an advantage over the first option in that it emits less electromagnetic interference and allows for the use of LV-rating power devices, which increases the fault tolerance in this stage [14].

Table 2. Potential second-stage topologies and control algorithms for SST in SG [8,14,15].

Topology	Advantages	Disadvantages
Cascade H-Bridge	Simple control strategy and simple voltage balance control Modularity	Unachievable MVDC link
Single-phase Dual Active Bridge Converter	Smaller number of passive components Higher efficiency	High RMS DC capacitor currents
Three-phase Dual Active Bridge Converter	Lower RMS current Lower ratings of component	Multiple switches and inductors High losses
Bidirectional Isolated Current Doubler Topology	Higher currents Small conduction losses Smaller number of switches	Requires more inductors
Bidirectional Isolated Push–Pull Topology	High currents Smaller inductor Smaller number of switches	Complex HF transformer
Control algorithms		
Phase-Shift Modulation	Simple algorithm	High losses at low power
Trapezoidal Modulation	Higher-voltage spectrum	Discontinued operation without load
Triangular Modulation	Lower switching losses	Higher RMS currents

2.3. SST System Control Strategy

The control strategy of SST in SG is a complex task. The main task for the control strategy is to maintain a power balance within the SG [16]. Additionally, the control strategy should maintain MVDC, LVDC buss voltages and currents, battery management, power factor correction for MVAC and LVAC grids, control of renewable energy generators (photovoltaic panels, wind turbines, hydro turbines, etc.), operating the microgrid in the islanding mode, optimum battery management and the seamless transfer between the two operational modes, etc. [7,8,14–16].

There are three categories: centralized, decentralized, and hierarchical control. In centralized control strategy, the control circuit controls the three-stage SST as one converter. This central controller is connected to the microgrid via a communication link; thus, the controller relies on the data flow from the communication channel, which reduces the overall system reliability. This control approach is rarely implemented for SST-based SGs [7].

In decentralized control strategy, the converter control circuits are separated from each other, thus increasing the system reliability. To fulfill the control needs of microgrids, centralized and decentralized techniques have been used. However, given the difficult control requirements imposed on microgrids, more advanced regulating must be used [17]. Hierarchical control combines the benefits of centralized and decentralized control, allowing for more complex control objectives to be realized. Table 3 summarizes the control strategies for SST-based microgrids. In this paper, a decentralized control strategy was selected with a global power flow control.

Table 3. SST's system control strategies for microgrids [16].

Control Strategy Type	Control Purpose	Control Algorithms
Decentralized	Voltage regulation of MVDC bus	Voltage and current dq controller with PWM
	Bidirectional power flow and power factor correction at MVAC grid	
	Voltage regulation of LVDC bus	PSM

Table 3. *Cont.*

Control Strategy Type	Control Purpose	Control Algorithms
Decentralized	Voltage regulation of LVAC grid	D-q controller with SPWM
	Capacitor voltage balancing	PI controllers
Centralized	Complex power management	Predictive control algorithm
	Regulation of DC voltages	Phase-shift method, PWM
	Bidirectional power flow	
	Voltage regulation on isolation stage	Fuzzy logic
Hierarchical	Primary control layer: decentralized control of each stage of SST	Droop control
	Secondary control layer: voltage control and management of DC links	Voltage compensation with PI controller
	Tertiary control layer: BMS (battery management system), microgrid's power and fault management	Higher-level control

3. Design of Proposed SST Concept

According to research in the previous section, the proposed design is based on a bidirectional input-serial output-parallel (ISOP) topology. Figure 1 represents the proposed approach of a SG based on a ISOP SST.

This paper focus on the SST part of the SG. The SST is connected to a MVAC distribution grid with a voltage level of 22 kV (Figure 2). The LVDC voltage is set to 600 V [13] for the micro-grid. The proposed concept is designed to the power level of 1 MW. This power level was determined for inspecting the highest power demand in a local group of smart residences. The control strategy is based on the hierarchical control. Each stage of the SST is controlled individually (primary layer), and the power flow is set by a higher control layer.

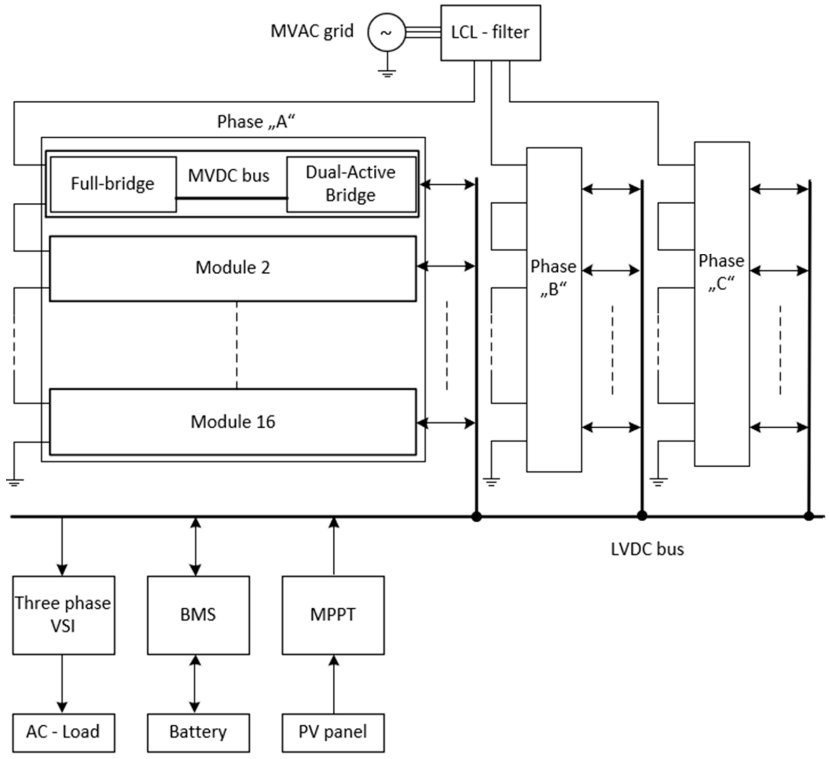

Figure 2. Block diagram of proposed SST concept.

3.1. Design of Medium-Voltage Stage

According to previous research, a three-phase, modular, multilevel cascaded full-bridge (MMCHB) topology was selected as a MV stage of the proposed SST. This section focuses on the design of one module of this converter. Figure 3 illustrates the schematic of the MV stage. The most significant advantages of a MMCHB are modularity and simple control. The disadvantage of this converter is the additional voltage balancing control for each filter capacitor on the DC side. Yet, in comparison with a modular multilevel converter (MMC), the MMCHB divides the MVDC voltage among each module, so the topology does not require high-voltage capacitors on the MVDC side. In addition, MMCHB topologies provide lower voltage requirements for the isolation stage on the MVDC side, thus lower voltage requirements for semiconductor switches.

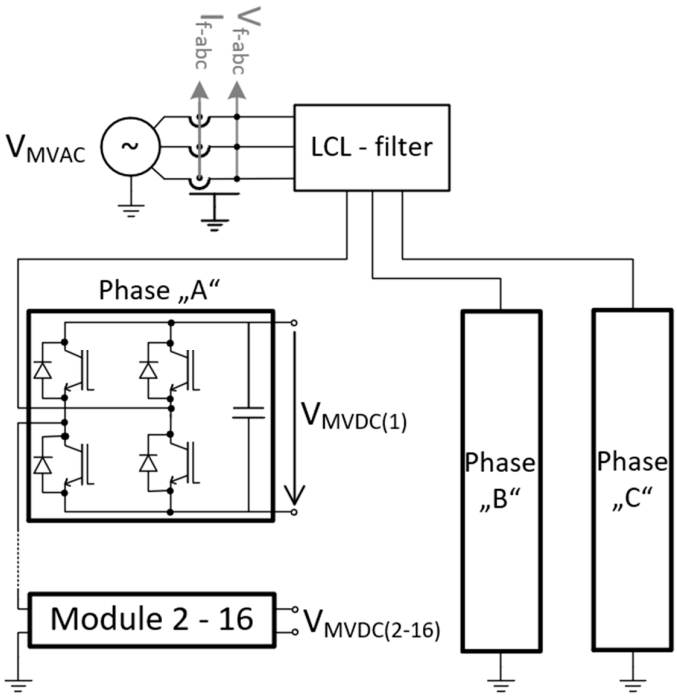

Figure 3. Medium-voltage stage of proposed SST.

The required number of modules in a MMCHB depends on the total output DC voltage (Vmvdc) and the non-destructive rate of the blocking voltage of the selected semiconductor switches. The minimum value of the output DC voltage of a MMCHB can by calculated by (1).

$$V_{mvdc\_min} = V_{mvac(l-l)} \cdot \sqrt{2} \quad (1)$$

It is necessary to compensate the voltage drops across filters to ensure the proper operation of the MMCHB converter [18]. This can be achieved by calculating the DC output voltage (V_{mvdc}) with an added tolerance. In this paper, a 10% voltage tolerance is selected, and Equation (2) calculates with this voltage tolerance the minimum output DC voltage of the MMCVHB.

$$V_{mvdc} = V_{mvdc\_min} \cdot 1.1 \quad (2)$$

A high-voltage Silicon (SI)-based IGBT transistor with a blocking voltage (V_{BR_max}) of 4.5 kV is used as the semiconductor switches for the proposed MMCHB converter.

The minimal number of modules for the converter is determined with the following Equation (3).

$$N\_sm \geq \frac{V_{mvdc} \cdot y}{V_{BR\_max}} \quad (3)$$

where y refers to a safety factor that assumes the additional voltage across the IGBT impacted by leakage inductances [19]. In this paper, a safety factor of 1.2 is selected. Equation (4) determines an output DC voltage in one module of the converter.

$$V_{mvdc\_sm\_max} = \frac{V_{mvdc}}{N_{sm}} \tag{4}$$

For analysis of the current behavior, assume a connection of two full-bridge modules, creating a five-level MMCHB converter; see Figure 4. The current through semiconductor switches in any module of MMCBH can be described as a time-dependent binary switching function, $s(t) \in \{1, 0\}$, assuming that the switches are ideal, and the input AC current describes a sinusoidal time waveform due to filter circuits. Under these assumptions and this analysis of the MMCHB converter, it is possible to identify the conductivity of each switching transistor.

$$i_{C1} = [s_1(t) - s_2(t)] \cdot i_0(t) \tag{5}$$

$$i_{C2} = [s_3(t) - s_4(t)] \cdot i_0(t) \tag{6}$$

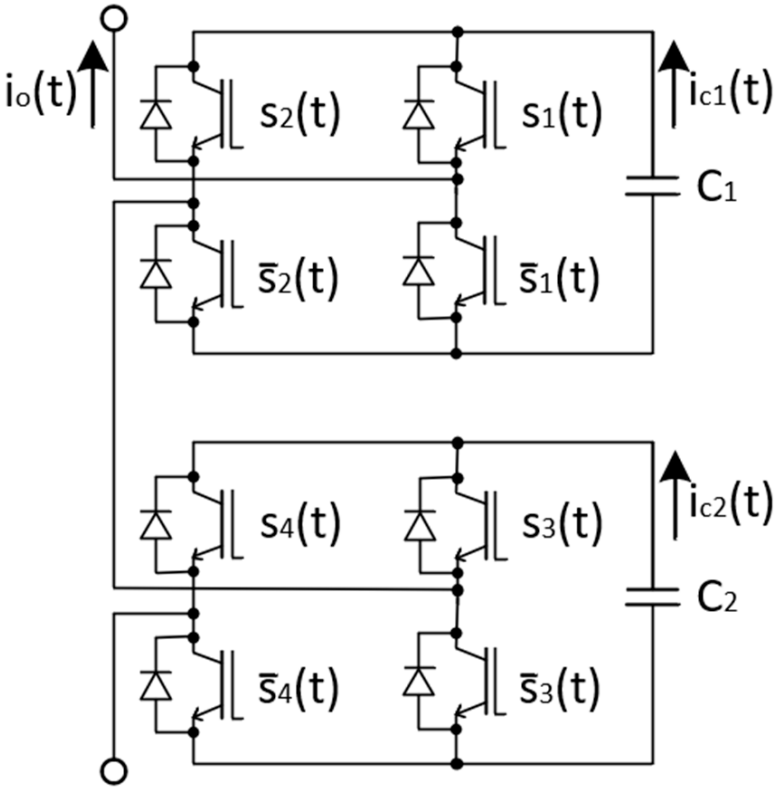

Figure 4. One leg of five-level MMCHB converter.

The output DC currents (i_{C1} and i_{C2}) are described in (5) and (6). The total current $i_0(t)$ is obtained by the superposition of the time-varying partial switching currents $ic_{1\text{-}2}$ (t) from each module of the MMCHB converter [20].

In order to control the two-way power flow of a MMCHB converter, a direct vector control strategy was selected and proposed in this paper. The task of the control circuit is to generate the required amount of active power into the MVAC grid, as well as the DC bus, depending on the direction of the energy flow [21].

At the same time, the control circuit maintains the average value of the MVDC voltage of the DC filter capacitors at a defined constant level. Figure 5 shows the control circuit, which consists of an outer and an inner loop. The outer loop consists of a voltage regulator

that compares the reference value with the measured average value of the voltage on the capacitors and provides a reference value for the inner current loop through a discrete PI regulator with an anti-wind-up. The inner current loops are implemented in separate current i_d and i_q controllers. The transformation functions from "abc" to "α-β", "q-d", and vice versa are synchronized with the AC network via a three-phase, decoupled, double synchronous reference frame (DSRF)-type phase-locked loop (PLL) [21].

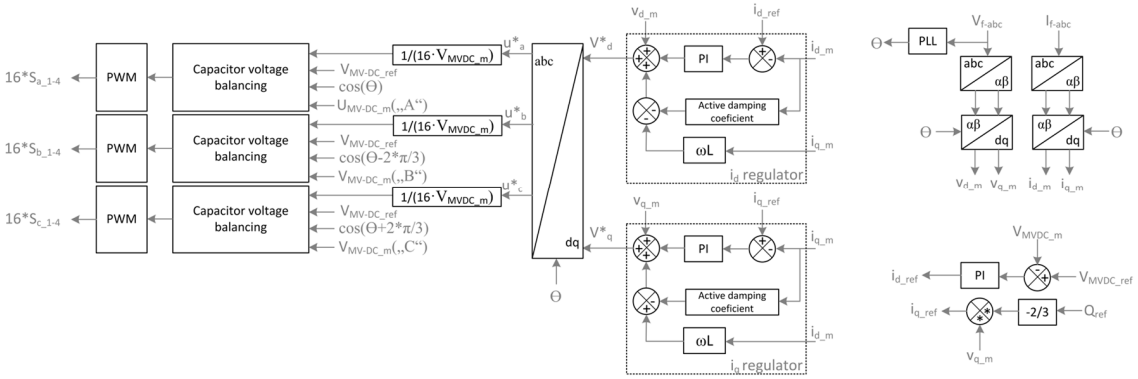

Figure 5. Block diagram of controller circuit for MV stage of proposed SST.

The decoupled double synchronous reference frame PLL makes use of two synchronous reference frames that rotate at positive and negative synchronous velocities. This permits the influence of the negative sequence component on the dq-signals to be decoupled. This is especially important when synchronizing to non-ideal grids, such as those with unbalanced voltage characteristics. Because the double-frequency ripple induced by the unbalanced grid situation is avoided, a greater control bandwidth may be set in comparison to the basic PLL, such as the synchronously rotating reference (SFR) PLL.

The reference value of the d-axis component comes from the voltage regulator, while the reference value of the q-axis component is directly calculated from the required reactive power. The outputs of the discrete current regulators in the d-q system are back-transformed into the α-β system and further transformed into the three-phase system. Subsequently, the back-transformed quantities are divided by the sum of the voltages of the capacitors of one phase. The resulting values are further used as reference indexes for the voltage balance block on the output capacitors.

To guarantee a homogeneous distribution of the required power from the MVAC grid among all the capacitors of the MMCHB converter, it is necessary to adjust the modulation indexes of individual modules so that they differ from the preset value provided by the external control loop. The voltage balancing of the DC filter capacitors is implemented in two steps [20]. In the first step, the controller individually maintains the voltage value on the 16 cells (modules) in each branch at average value, while in the next step, the controller ensures that the mean voltage value on all capacitors in 1 branch is equal to the mean voltage value of all legs.

The switching signals of full-bridge converters in each module are generated as a result of comparing the modulation index with a triangular reference signal with a frequency of 10 kHz. For each leg, the triangular carrier signal, for modules 1 to 16, is phase-shifted by 22.5°. In this way, a 17-level output voltage can be achieved, which significantly reduces the amount of harmonic distortion generated by the MMCHB converter to the MVAC distribution grid.

3.2. Design of Isolated Stage

According to previous research on isolated stages, the dual active bridge (DAB) converter was selected. The advantages of DAB are high efficiency, high power density, the possibility of bidirectional power flow control, soft switching at zero voltage (ZVS), and

lower stress on semiconductor switches [22,23]. Figure 6 shows the DAB topology, which consists of two bridge converters and a high-frequency transformer (HFT).

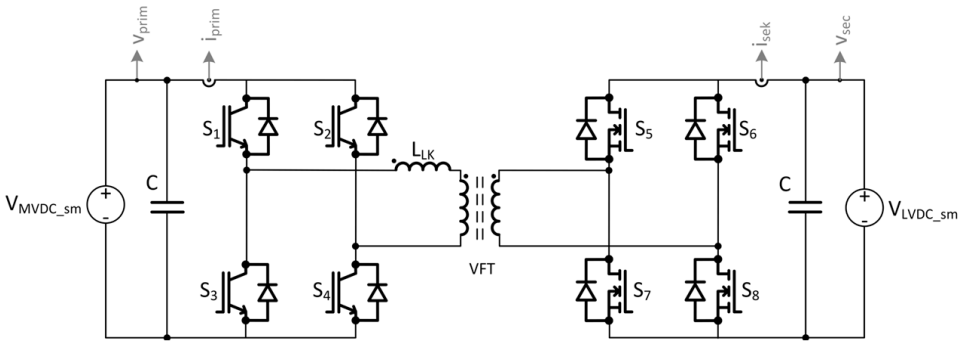

Figure 6. Dual active bridge converter.

The input of the isolated stage is connected to the output of MVDC busses of the MMCHB converter. The output of the isolated stage forms a common LVDC bus with a required value of 600 V. The LVDC bus represents the base for the microgrid for local smart residences. Output inverters (1 or 3 phase), electric energy storage (BSS, EV), or renewable sources (PV, WG) can then be connected to this network as needed.

The HFT serves to accumulate the energy in the leakage inductances, and the air gap of the DAB primary side is connected to the MVDC bus of one module of the MMCHB converter. The DAB secondary sides are connected in parallel between all modules and phases.

The transmitted power can be defined by (13), where d is the ratio of the phase shift of the primary and secondary parts, n is the turns ratio of the HFT, T is the period, and L_{LK} is the stray inductance of the HFT.

$$P = V_{out} \cdot I_{out} = \frac{(1 - |d|) \cdot d \cdot T \cdot V_{in} \cdot V_{out}}{n \cdot L_{Lk}} \tag{7}$$

Equation (7) represents the dependence of the transmitted power as a function of the phase shift between the primary and secondary sides, a function of the switching frequency, and the leakage inductance. According to (7), it is possible to derive the desired value of the leakage inductance as follows:

$$L_{Lk} = \frac{(1 - |d|) d V_{in} V_{out}}{2 f_s n P_{max}} \tag{8}$$

The phase-shift method was chosen to generate the control PWM signal. The value of the phase-shift ratio "d" between the primary and secondary sides will not only determine the magnitude, but also the direction of the power flow.

Changing the control pulses of the secondary side by a positive value of "d" will ensure the power flow from the primary to the secondary side, while in this mode, the control pulses for the switches of the primary side S1,4 and the secondary side S5,8 are taken into account [24,25].

Similarly, with a negative value of 'd', the power flow is supplied from the secondary to the primary side. The control system is shown in Figure 7 and consists of an outer and an inner loop for both power flow directions. The outer loop consists of a voltage discrete PI type regulator and the inner loop consists of a current discrete PI regulator. The output of the current regulators represents the modulation index for the phase-shift PWM generator. Subsequently, for the control of the modular DAB, the PWM signals are interleaved with each other.

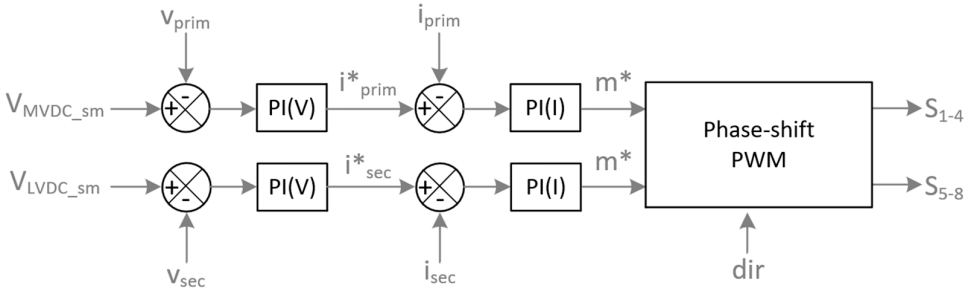

Figure 7. Block diagram of control circuit for DAB converter (one module).

3.3. Filter Design

Higher harmonics, which are generated by the switching of high-power semiconductor converters, are a major factor causing negative issues for connected sensitive loads within the common grid. A suitably designed filter reduces the higher harmonics of the current flow while power semiconductor switches operate in high-frequency switching mode. For higher-power applications, in addition to the appropriate choice of filter type, the price and overall total harmonic distortion (THD) are also important factors during the design [26,27]. For these facts, L, LC, or LCL filters are usually connected between the AC grid and the power semiconductor converters; see Figure 8. The LCL-type filter has a higher damping quality of higher harmonics and better dynamic characteristics compared to the LC-type filter [27].

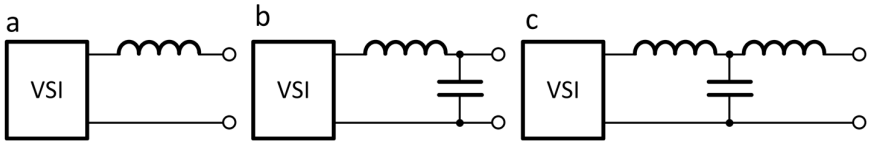

Figure 8. Filter schematics (**a**) L, (**b**) LC, (**c**) LCL.

However, the LCL filter type causes stability problems due to its unwanted natural resonance behavior, which is caused by the impedance of the grid and the impedance of the filter capacitor at certain frequencies (natural resonance of the LC elements). Further, reactive power requirements can cause unwanted resonance between the capacitor and the AC grid.

For this reason, it is necessary to minimize the resonance. This can be achieved with active or passive damping techniques. In this paper, a passive damping was selected. The passive damping is achieved by connecting a series resistance to the filter capacitor [27].

The first step in the design of the LCL-type filter is to determine the values of the inductances of coil L_1 on the AC grid side and L_2 on the converter side. These coils serve to dampen the ripple of the output current. According to the standard IEEE Std 1515-2000, the ripple of the output current is specified to a value of 20% of the nominal value of the output current (see relation (9)) [28].

$$\Delta I_{L_{max}} = \frac{0.02 \cdot P}{3 \cdot V_{mvac\_RMS}} \tag{9}$$

where P represents the active power of the converter, and V_{mvac_RMS} represents the RMS value of the input voltage of the AC grid. The total inductance L_{tot} of the LCL filter is determined by Equation (10), where N is the number of modules per leg, and f_{sw} represents the switching frequency.

$$L_{tot} = \frac{V_{mvdc}}{N \cdot f_{sw} \cdot \Delta I_{L_{max}}} \tag{10}$$

The determination of L_1 and L_2 is shown in Equations (11) and (12), where L_g represents the inductance of the MVAC grid.

$$L_{1f\_mvac} = \frac{L_{tot}}{2} \tag{11}$$

$$L_{2f\_mvac} = L_{1f\_mvac} - L_{g\_mvac} \tag{12}$$

The design of the filter capacitor for one phase depends on the reactive power attenuation requirement. It is common practice that the value of the reactive power (Q) absorbed by the filter capacitor is limited to 5% of the nominal power. The value of the filter capacitance C_{f_mvac} can be determined by Equation (13).

$$C_{f\_mvac} = \frac{0.05 \cdot Q}{3 \cdot U^2_{mvac\_ef} \cdot 2 \cdot \pi \cdot f_g} \tag{13}$$

The resonant frequency of the LCL-type filter must be higher than the grid frequency (f_g) and, at the same time, must have at least half the value of the switching frequency f_{sw}. The resonant frequency (f_{res}) of the LCL-type filter is determined by (14). This equation is derived from Thomson's relation of the LCL circuit.

$$f_{res} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{L_1 + L_2}{L_g \cdot L_2 \cdot C_f}} \tag{14}$$

$$\omega_{res} = 2 \cdot \pi \cdot f_{res} \tag{15}$$

The value of the damping resistor can be determined by (16), where ω_{res} represents the angular resonant frequency of the LCL filter (15). The disadvantage of the passive damping technique is the increase in the losses by the added damping resistor, which reduces the overall efficiency of the converter [27].

$$R_{sd} = \frac{1}{3 \cdot \omega_{res} \cdot C_f} \tag{16}$$

When designing a filter capacitor for DC busses, the nominal power (P), the grid frequency (f_g), the DC voltage ripple (Δu), and the DC voltage per module (V_{mvdc_sm}) are considered [27]. The minimum capacitance of the DC filter is determined in (17), while we considered the value of a voltage ripple of 10% of V_{mvdc_sm}.

$$C_{f-min} = \frac{\frac{P}{3 \cdot N\_sm}}{2 \cdot \pi \cdot f_g \cdot \Delta u \cdot V^2_{mvdc\_sm}} \tag{17}$$

4. Global Simulation Model Design for HIL Analyses

In this part of the paper, the simulation model implementation of the proposed SST concept as a base for smart grids is described. Next, the simulation analysis of two possible operational scenarios are performed.

Figure 9 shows the principal block diagram of the SST concept and the circuit schematic of one SST module. The simulation model is designed in the PLECS circuit simulation environment. Figure 10 shows one module of the proposed concept in the PLECS circuit simulator. From Equation (3), the number of modules per phase is 16, thus the total number of modules is 48.

The model of the one SST module from Figure 9 or Figure 10 consists of three full-bridge connections. The first full-bridge (FB) with switches $S_{1–4}$ represents one module of the MMCHB converter and also the MV-side input of one SST module. The second FB with switches $S_{5–8}$ represents the high-voltage primary side of a DAB converter. Between

the first and second full-bridges, an intermediate MVDC bus is located per every module. This MVDC bus is design to a maximum voltage level ($V_{MVDC\_sm\_max}$) of 3.7 kV, according to Equation (4). The third FB with switches $S_{9–12}$ represents the low-voltage secondary side of the DAB converter and also the LV-side output of one SST module. The inputs (MV-side connections) of all modules are connected in series within one phase. The outputs (LV-side connections) are connected in parallel within the three phases, thus creating a LVDC-bus as a base for smart grids. The specifications of the simulation model are recorded in Tables 4 and 5.

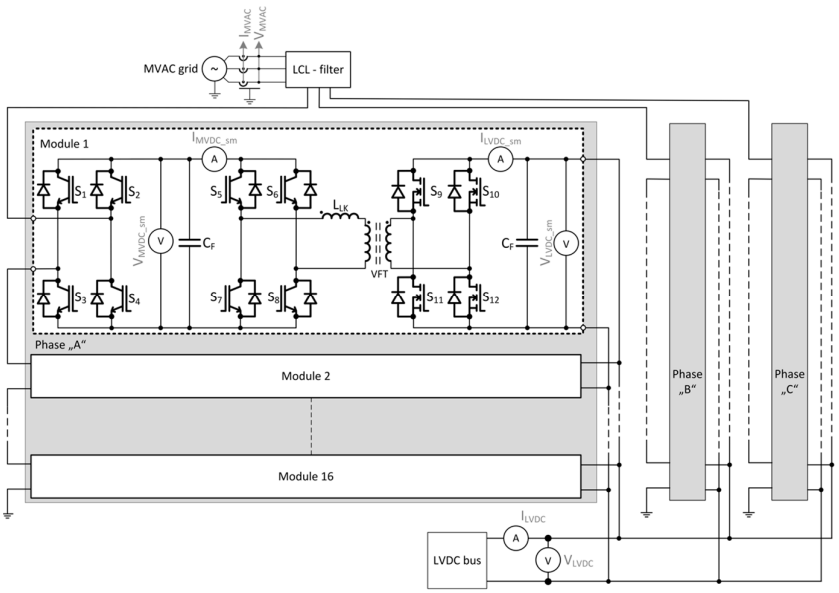

Figure 9. Block diagram of the SST simulation model for smart grids.

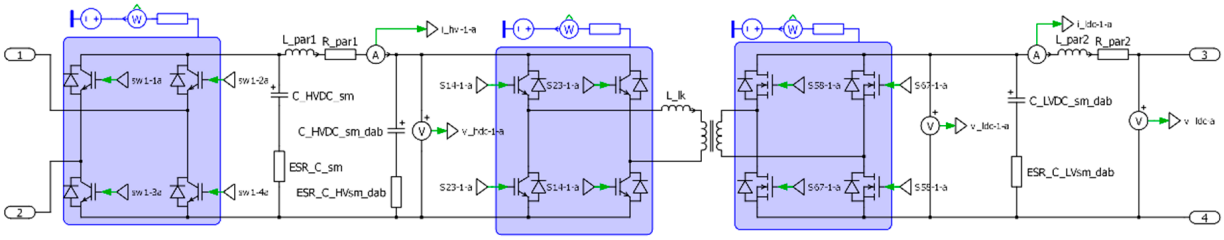

Figure 10. One module of simulation model.

Table 4. Specifications for MV stage of proposed SST.

Parameter	Value
P_{nom}	1 MW
$V_{MVAC(RMS)}$	22 kV
$V_{MVAC(l-l)}$	38.105 kV
$I_{total(RMS)}$	45.45 A
$f_{sw(MMCHB)}$	10 kHz
$V_{MVAC(p-p)}$	53,889 kV
V_{MVDC_max}	59,278 kV
$V_{MVDC\_sm\_max}$	3.7 kV
L_{g_AC}	5 µH
L_{1f_AC}	55,578 mH
L_{2f_AC}	55,578 mH
C_{f_AC}	109,611 pF
C_{MVDC_sm}	24,207 µF

Table 5. Specifications for isolated stage of proposed SST.

Parameter	Value
P_{nom_sm}	20,833 kW
I_{sm_max}	5.63 A
$V_{MVDC\_sm\_max}$	3.7 kV
$f_{sw(MMCH)}$	25 kHz
L_{LK}	86.4 µH
$C_{DAB\_MVDC\_sm}$	94.5 pF
$C_{DAB\_LVDC\_sm}$	35,957 µF

Figure 11 shows the control circuit for the DAB converter, and Figure 12 shows the control circuit for the one-phase, five-level MMCHB converter. The control circuits were designed according to the previous research described within this paper. As a merit of the performance evaluation, the power factor (PF), system efficiency, and total harmonic distortion (THDi) have been analyzed during various operational scenarios.

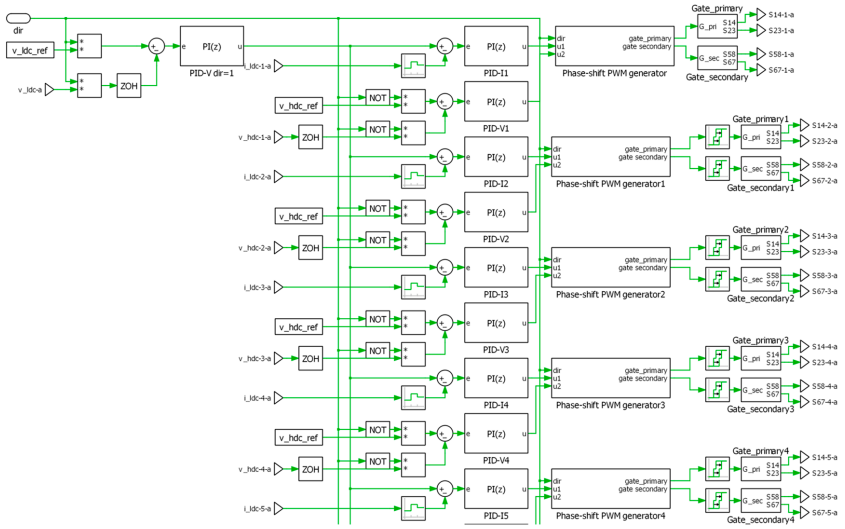

Figure 11. Control circuit for DAB converter model considering four modules in one phase.

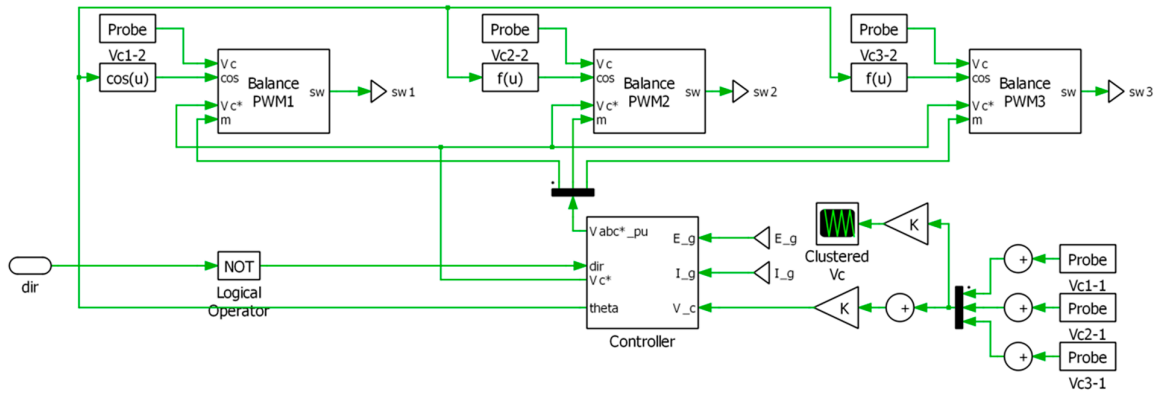

Figure 12. Control circuit for MMCHB converter.

During development of the simulation model, the focus of the control strategy and the implementation of the proposed SST concept described earlier in this paper are considered. Therefore, linearized IGBT and MOSFET models and a magnetic model of a high-frequency transformer were utilized within the simulation model [13]. This approach reduces the requirements for the computation time, while it enables HIL tests, as well. The proposed concept consists of 384 IGBT and 192 MOSFET transistor switches.

5. Results

This section deals with the evaluation of the simulation results. The simulation model was evaluated for two operational scenarios. In the first scenario, which is shown in Figure 13, the maximum limit of the transmitted power is set to 1 MW, and the power flow direction is set from the MVAC grid to the LVDC bus.

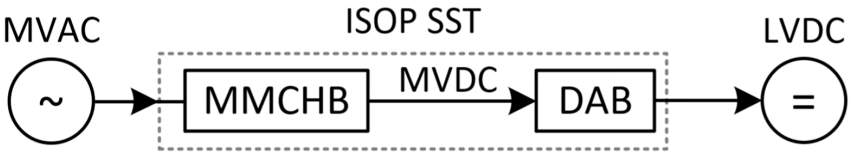

Figure 13. Illustration of power flow for first operational scenario.

Figures 14–16 show the main parameters of the investigated ET concept, i.e., Figure 14 shows the voltages, currents and the active and reactive power of the MVAC grid (U_{MVAC}, I_{MVAC}, P_{MVAC}, Q_{MVAC}). Figure 15 shows the voltages and currents of the MVDC and buss in all modules (U_{MVDC}, I_{MVDC}), and Figure 16 shows the voltage, current, and power of the common LVDC bus (U_{LVDC}, I_{LVDC}, P_{LVDC}). Furthermore, an evaluation of the power factor (PF), total system efficiency (η_{total}), and total harmonic distortion of current (THD_i) was taken into account in this paper; see (18–20).

$$PF = \frac{P_{out}}{U_{out} \cdot I_{out}} \tag{18}$$

$$\eta_{total} = \frac{P_{out}}{P_{in}} \cdot 100\% \tag{19}$$

$$THD_i = \frac{\sum_{i=n}^{\infty} I_{out\ i}}{I_{out\ 1}} \tag{20}$$

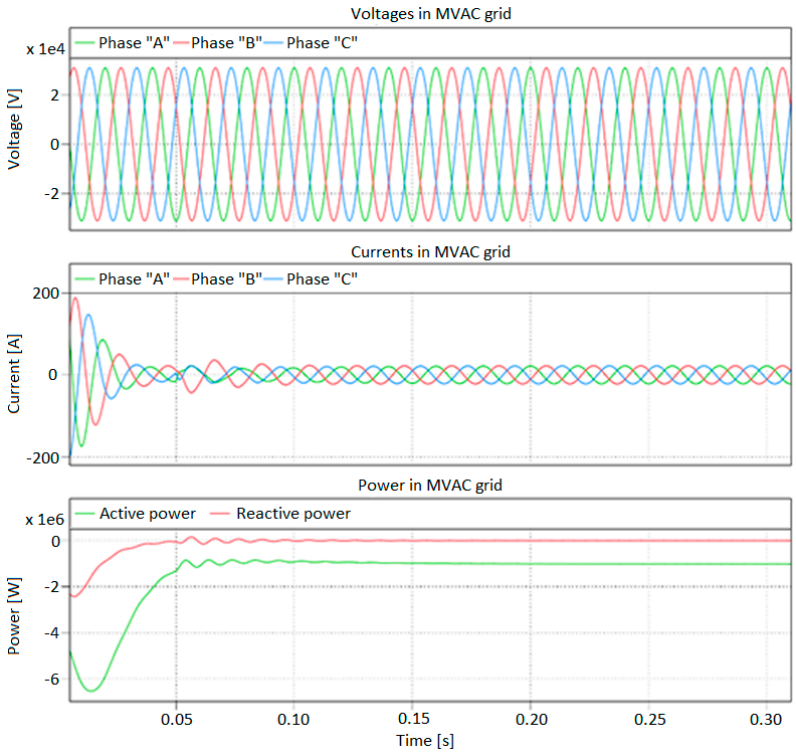

Figure 14. Time-waveforms of the main parameter of MVAC grid for first operational scenario.

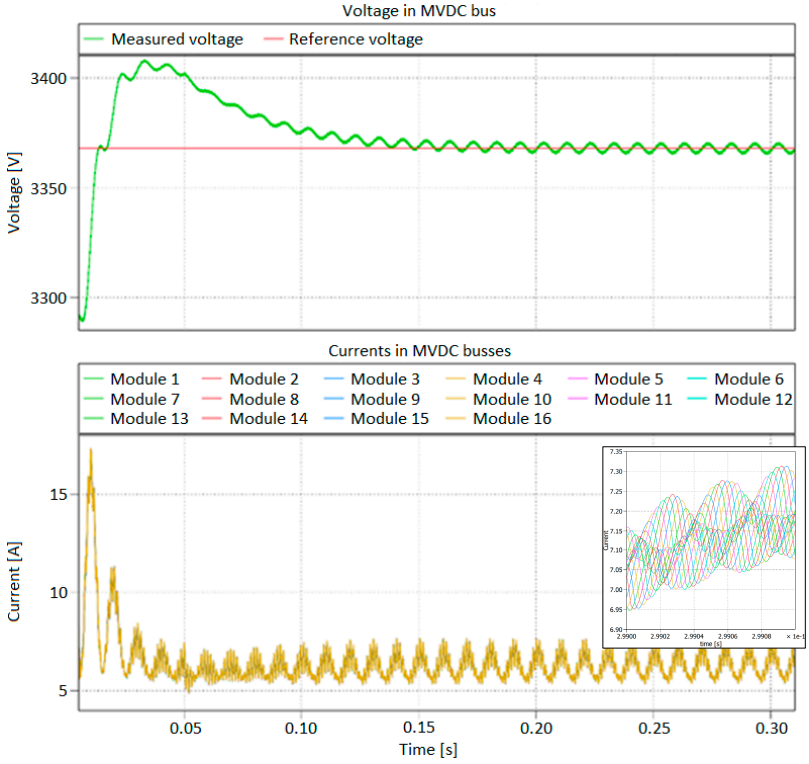

Figure 15. Time-waveforms of the voltages and currents of MVDC bus for first operational scenario.

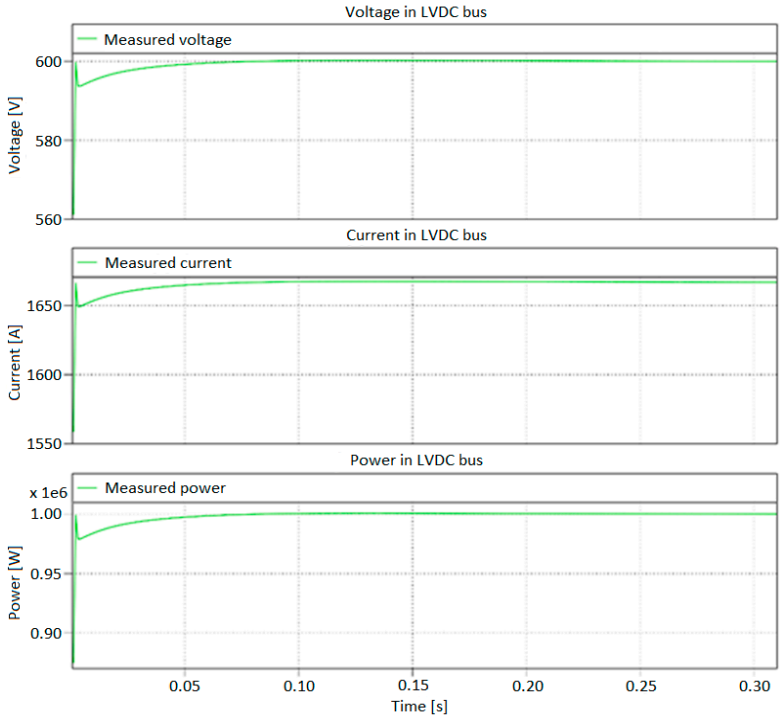

Figure 16. Time-waveforms of the voltages and currents of LVDC bus for first operational scenario.

Table 6 lists a summary of the qualitative parameters of the proposed concept in the steady state for the first operational scenario. Based on this simulation result, the concept shows a total efficiency of 91.68% and the THD_i of 1.779%. The voltage ripple on the LVDC side reached a level of 0.38 V and a current ripple of 0.105 A. The low voltage and current ripple at the LVDC bus are achieved from the ISOP topology of SST.

Table 6. Qualitative parameters of proposed concept for first operational scenario.

Parameter	Value
V_{LVDC}	600.12 V
ΔV_{LVDC}	0.38 V
I_{LVDC_sm}	1667.09 A
ΔI_{LVDC_sm}	0.105 A
V_{MVDC_sm}	3367.92 V
ΔV_{MVDC_sm}	0.782 V
I_{MVDC_sm}	5.631 A
ΔI_{MVDC_sm}	0.612 A
$V_{MVAC(RMS)}$	22 kV
PF	0.999
η_{celk}	91.68%
THD_i	1.779%

For the second scenario, which is shown in Figure 17, the maximum limit of the transmitted power is set to 1 MW, and the power flow direction is set from the LVDC bus to the MVAC grid. Figures 18–20 show time-waveforms of the main parameters of the investigated SST concept.

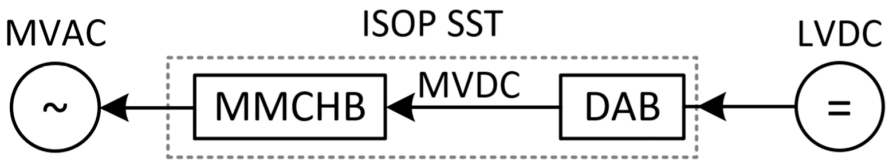

Figure 17. Illustration of power flow for the second operational scenario.

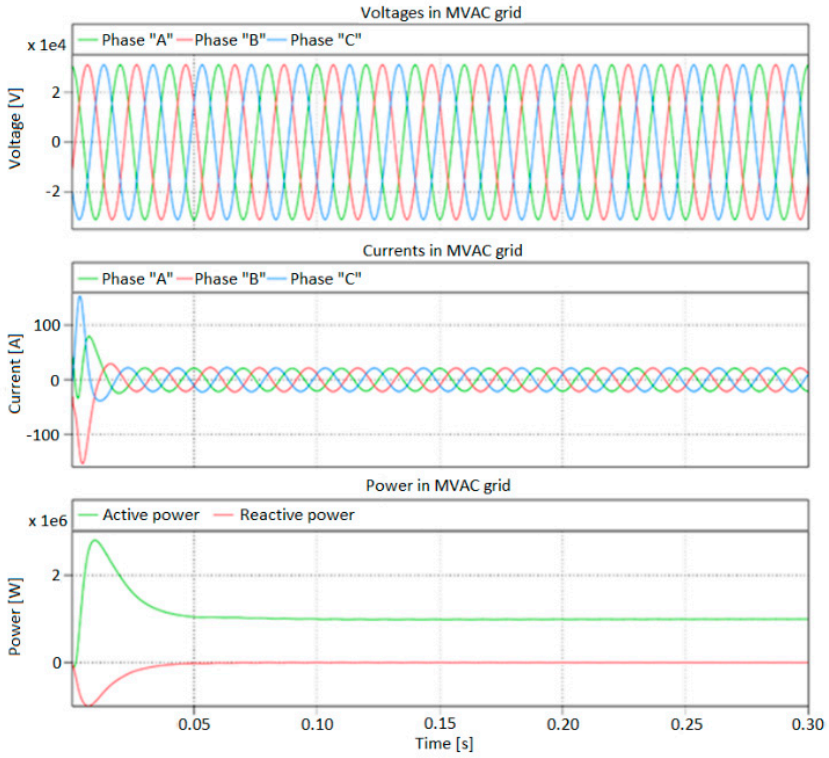

Figure 18. Time-waveforms of the main parameter of MVAC grid for second operational scenario.

Table 7 lists a summary of the qualitative parameters of the proposed concept in the steady state for the second scenario. In this paper, the LVDC bus model was represented as a voltage source. Based on this simulation result, the concept shows a total efficiency

of 92.351% and a THD_i of 1.869%. The voltage ripple on the LVDC side reached a level of 0.43 V and a current ripple of 0.755 A. The low voltage and current ripple at the LVDC bus are achieved from the ISOP topology of SST.

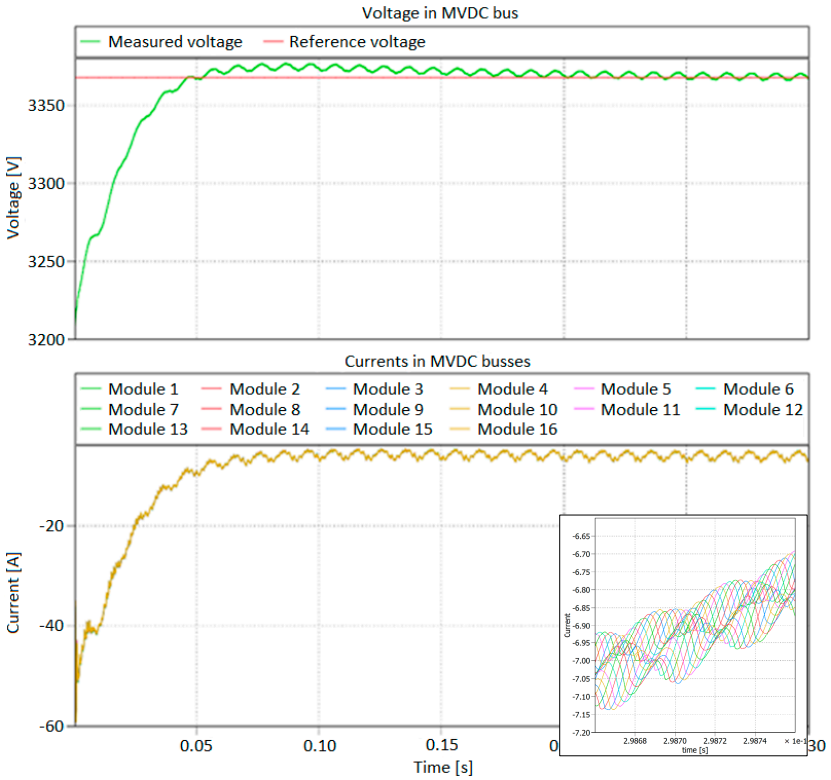

Figure 19. Time-waveforms of the voltages and currents of MVDC bus for second operational scenario.

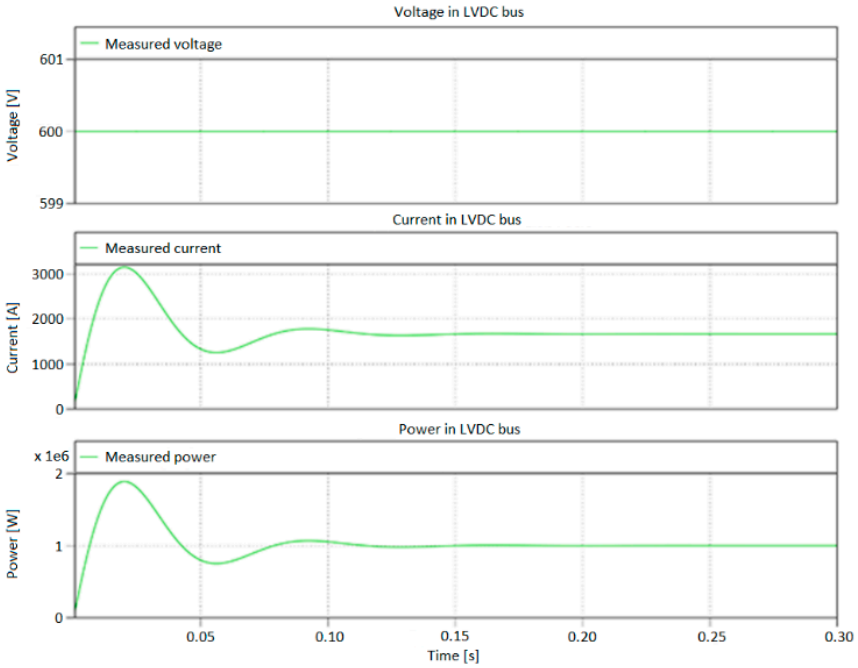

Figure 20. Time-waveforms of the voltages and currents of LVDC bus for second operational scenario.

The total system efficiency of the presented model reached an average value of 92.02% in the steady state, the average THDi value is 1.82%, and the power factor value is close to 1 in both operational scenarios. The $V_{MVDC\_sm\_max}$ value is 3368.64 V on average for

both operational scenarios, which is below the calculated value from (4). This 10% safety tolerance is implemented to ensure the unwanted high-voltage fluctuations that can destroy the semiconductor switches.

Table 7. Qualitative parameters of proposed concept for second operational scenario.

Parameter	Value
V_{LVDC}	600 V
ΔV_{LVDC}	0.43 V
I_{LVDC_sm}	1633.7 A
ΔI_{LVDC_sm}	0.755 A
V_{MVDC_sm}	3369.68 V
ΔV_{MVDC_sm}	4.026 V
I_{MVDC_sm}	6.626 A
ΔI_{MVDC_sm}	1.461 A
$V_{MVAC(RMS)}$	22 kV
PF	0.999
η_{tot}	92.351%
THD_i	1.869%

6. Conclusions

In this paper, a review of possible topologies and control algorithms of SST in SG was described. Based on previous research, a possible concept of SST for SG application was determined, designed, and verified with a simulation model. The proposed concept is based on ISOP topology. The concept consists of two stages. The MV stage is based on an MMCHB converter, and the isolation stage consists of modular DAB converters. The MVDC busses of the MMCHB converter are connected to the HV sides of each DAB module. The LV sides of DAB modules are connected in parrel, forming the base of the micro-grid for a local group of smart residences. For verification of the designed concept, a simulation model was implemented in the PLECS circuit simulator. During the verification, both power flow directions of the proposed concept were evaluated. The advantage of utilizing a piecewise linear simulator (such as the PLECS circuit simulator) is the capability to simulate and study the behavior of complex converter systems (such as SSTs) as a real-time system within a reasonable simulation time. The possible disadvantage of the proposed solution in comparison with the listed topological solutions is a higher number of semiconductor switches, HVTs, and filter capacitors in MVDC buses, which leads to additional complex balancing algorithms. Another disadvantage of ISOP topology lies in cases when a short-circuit failure of one module occurs. This scenario leads to higher stress levels in the other modules and could be analyzed in the future to improve the design of the proposed SST solution.

This work presented an implementation of a decentralized control strategy with a global power flow control. In future work, this approach can be used as a base for a more complex and reliable hierarchical control strategy. Although the proposed concept of an SST-based smart grid gained low voltage and current ripples and good efficiency in simulation results, there is room for further development and additional improvements. One of the areas of investigation is the known relevant behavior of the SST-based smart grid and its control strategies in various operating situations, or the investigation of critical operating condition occurrences.

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Abbreviations

Symbol	Definition
AC	Alternating current
BMS	Battery management system
BSS	Battery storage system
DAB	Dual active bridge
DC	Direct current
DSRF	Decoupled double synchronous reference frame
EV	Electric vehicle
FB	Full bridge
HFT	High-frequency transformer
HIL	Hardware-in-the-loop
IGBT	Insulated-gate bipolar transistor
ISOP	Input-serial output-parallel
LVAC	Low-voltage alternating current
LVDC	Low-voltage direct current
MMC	Modular multilevel converter
MMCHB	Modular multilevel cascaded full-bridge
MOSFET	Metal–oxide–semiconductor field-effect transistor
MPPT	Maximum power point tracking
MV	Medium voltage
MVAC	Medium-voltage alternating current
MVDC	Medium-voltage direct current
NPC	Neutral-point-clamped
PI	Proportional-integral
PLECS	Piecewise linear electrical circuit simulation
PLL	Phase-locked loop
PSM	Phase-shifted modulation
PV	Photo-voltaic
PWM	Pulse width modulation
RMS	Root mean square
SG	Smart grid
SPWM	Sine pulse width modulation
SRF	Synchronously rotating reference
SST	Solid-state transformer
THD	Total harmonic distortion
VSI	Voltage source inverter
WG	Wind generator
ZVS	Zero voltage switching

References

1. Hadjsaïd, N.; Sabonnadière, J.C. (Eds.) *Smart Grids*; John Wiley and Sons: Hoboken, NJ, USA; ISTE: London, UK, 2012.
2. Momoh, J. *Smart Grid. Fundamentals of Design and Analysis*; John Wiley and Sons; IEEE Press: Hoboken, NJ, USA, 2012.
3. Heinemann, L.; Mauthe, G. The universal power electronics based distribution transformer, a unified approach. In Proceedings of the 32nd IEEE Annual Power Electronics Specialists Conference, Vancouver, BC, Canada, 17–21 June 2001; pp. 504–509.
4. Liu, Y.; Escobar-Mejia, A.; Farnell, C.; Zhang, Y.; Balda, J.C.; Mantooth, H.A. Modular multilevel converter with high-frequency transformers for interfacing hybrid DC and AC microgrid systems. In Proceedings of the 5th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Galway, Ireland, 24–27 June 2014.
5. Alnawafah, H.; Harb, A. Modeling and Control for Hybrid Renewable Energy System in Smart Grid Scenario—A Case Study Part of Jordan Grid. In Proceedings of the 2021 12th International Renewable Energy Congress (IREC), Amman, Jordan, 14–15 April 2021; pp. 1–6. [CrossRef]
6. Falcones, S.; Mao, X.; Ayyanar, R. Topology comparison for solid state transformer implementation. In Proceedings of the IEEE 2010 PES General Meeting, Minneapolis, MN, USA, 25–29 July 2010; pp. 1–8.
7. Tan, K.; Yu, R.; Guo, S.; Huang, A.Q. Optimal design methodology of bidirectional LLC resonant DC/DC converter for solid state transformer application. In Proceedings of the IECON 2014—40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014; pp. 1657–1664. [CrossRef]
8. Firouzjaee, M.E.A. *Advanced Modeling of Solid State Transformer*; Departament d'Enginyeria Elèctrica, Universitat Politècnica de Catalunya: Barcelona, Spain, 2018.

9. *IEC Std 60038*; IEC Standard Voltages, Edition 7.0. IEC: Geneva, Switzerland, 2009.
10. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Pérez, M.A.; Leon, J.I. Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.* **2010**, *7*, 2553–2580.
11. Abu-Rub, H.; Holtz, J.; Rodriguez, J.; Baoming, G. Medium-voltage multilevel converters-State of the art, challenges, and requirements in industrial applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2581–2596.
12. Rodríguez, J.; Bernet, S.; Wu, B.; Pontt, J.O.; Kouro, S. Multilevel voltagesource-converter topologies for industrial medium-voltage drives. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2930–2945.
13. Frivaldsky, M.; Morgos, J.; Prazenica, M.; Takacs, K. System Level Simulation of Microgrid Power Electronic Systems. *Electronics* **2021**, *10*, 644. [CrossRef]
14. Liserre, M.; Buticchi, G.; Andresen, M.; De Carne, G.; Costa, L.F.; Zou, Z.-X. The smart transformer: Impact on the electric grid and technology challenges. *IEEE Ind. Electron. Mag.* **2016**, *10*, 46–58.
15. Hannan, M.A.; Ker, P.J.; Lipu, M.S.H.; Choi, Z.H.; Rahman, M.S.A.; Muttaqi, K.M.; Blaabjerg, F. State of the Art of Solid-State Transformers: Advanced Topologies, Implementation Issues, Recent Progress and Improvements. *IEEE Access* **2020**, *8*, 19113–19132. [CrossRef]
16. De Silva, H.H.H.; Jayamaha, D.; Lidula, W.A. Review on design and control of solid state transformer based microgrids. *AIMS Energy* **2019**, *7*, 901–923. [CrossRef]
17. Yu, X.; She, X.; Ni, X.; Huang, A.Q. System integration and hierarchical power management strategy for a solid-state transformer interfaced microgrid system. *IEEE Trans. Power Electron.* **2013**, *29*, 4415–4425. [CrossRef]
18. Adabi, M.E.; Martinez-Velasco, J.A.; Alepuz, S. Modeling and simulation of a MMC-based solid-state transformer. *Electr. Eng.* **2018**, *100*, 375–387. [CrossRef]
19. Islam, M.R.; Guo, Y.; Zhu, J. A High-Frequency Link Multilevel Cascaded Medium-Voltage Converter for Direct Grid Integration of Renewable Energy Systems. *IEEE Trans. Power Electron.* **2014**, *29*, 4167–4182. [CrossRef]
20. Marzoughi, A.; Burgos, R.; Boroyevich, D.; Xue, Y. Investigation and comparison of cascaded H-bridge and modular multilevel converter topologies for medium-voltage drive application. In Proceedings of the IECON 2014 40th Annual Conference of the IEEE Industrial Electronics Society, Dallas, TX, USA, 29 October–1 November 2014; pp. 1562–1568. [CrossRef]
21. Behrouzian, E. *Operation and Control of Cascaded H-Bridge Converter for STATCOM Application*; Chalmers University of Technology: Gothenburg, Sweden, 2016. Available online: https://www.researchgate.net/publication/301349487_Operation_and_control_of_cascaded_H-bridge_converter_for_STATCOM_application (accessed on 26 May 2022).
22. De Doncker, R.; Divan, D.; Kheraluwala, M. A three-phase softswitched high-power-density dc/dc converter for high-power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73.
23. Qin, H. Dual Active Bridge Converters in Solid State Transformer. Ph.D. Dissertation, Missouri University of Science and Technology, Rolla, MO, USA, 2012. Available online: https://scholarsmine.mst.edu/doctoral_dissertations/1914 (accessed on 26 May 2023).
24. Zumel, P.; Ortega, L.; Lazaro, A.; Fernandez, C.; Barrado, A. Control strategy for modular Dual Active Bridge input series output parallel. In Proceedings of the 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), Salt Lake City, UT, USA, 23–26 June 2013; pp. 1–7. [CrossRef]
25. Behrouzian, E.; Bongiorno, M.; De La Parra, H.Z. Investigation of negative sequence injection capability in H-bridge multilevel STATCOM. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, 26–28 August 2014; pp. 1–10. [CrossRef]
26. Rachev, E.; Petrov, V. DC link capacitor selection for DC-DC converters. In Proceedings of the 2020 12th Electrical Engineering Faculty Conference (BulEF), Varna Town, Bulgaria, 9–12 September 2020; pp. 1–5. [CrossRef]
27. El Wahid Hamza, K.A.; Linda, H.; Cherif, L. LCL filter design with passive damping for photovoltaic grid connected systems. In Proceedings of the IREC2015 The Sixth International Renewable Energy Congress, Sousse, Tunisia, 24–26 March 2015; pp. 1–4. [CrossRef]
28. Ahmed, K.H.; Finney, S.J.; Williams, B.W. Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation. In Proceedings of the Compatibility in Power Electronics (CPE), Gdansk, Poland, 29 May–1 June 2007; pp. 1–9. [CrossRef]