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Advanced Design and Optimization of Current Mode Blocks

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Abstract:
This article deals with the topology modifications and the optimization of the current mode building blocks for an analog part of the video signal (HDTV) preprocessing unit. The blocks of our interest are the Current Conveyor (CCII) as the basic functional block for current mode filters and the Caprio structure translated to CMOS for an implementation of low input impedance differential current input. The topology of the current conveyor was modified to enlarge output impedance and bandwidth. The Caprio structure was, in the first step, modified to operate as a current follower in the CMOS process. After the hand setting of the circuit parameters of both structures, they were optimized to improve their operation via Differential Evolution (DE) algorithm. The proposed blocks were simulated in 0.25 um CMOS process and they operate from under 1.8 V of symmetrical supply voltage. Along with the transconductance amplifiers, the investigated structures will be utilized in current mode anti-aliasing filter for the video applications.

INTRODUCTION

Recently, the usage of current mode blocks in analog signal preprocessing has arisen. Although a big amount of processes is transferred to a digital domain, an amplification and filtering before A/D conversion is still a challenging problem mainly for wide bandwidth signals. In this article, we are about to discuss the current mode building blocks for an implementation in the analog part of the mixed-signal CMOS integrated circuit – the video signal preprocessing unit – with respect to ITU-R BT.709-5 [7]. The final one-chip block will consists of analog filtering and amplification part and A/D converter part. The enhanced applicability of the proposed block will be provided by the low supply voltage and low current consumption that help to further usage in the mobile applications.

For the application in the HDTV we need the broadband analog functional blocks (FB). This implies directly an exploitation of the above mentioned current mode operation, because of its well known advantages in wide band and mainly in low voltage applications [4]. After the analysis of different current mode building blocks, we selected the 2nd generation Current Conveyor (CCII) as a current follower and the Caprio structure as a differential input current follower. These basic blocks together with the transconductance amplifier (OTA) allow us to realize the future top level blocks (anti-aliasing filter, true current operational amplifier [3, 4] e.g.). In the following text we will concern just about CCII and Caprio structures.

The content of the article is divided in three paragraphs. In the first paragraph we will focus our attention to the topology of both proposed circuits. The next paragraph deals with the optimization employing the DE algorithm and the last paragraph summarizes the simulation results. At the end of the paper there is a brief conclusion

CCII AND CAPRIO STRUCTURE DESIGN

Proposed topologies of the above mentioned functional blocks were designed with respect to the requirements of our application, which were mainly to maintain the existing wide bandwidth together with the drop of current consumption in the case of the CCII and an ideal current transfer function with the highest possible bandwidth in case of the second mentioned building block.. It is worth to note, that this features of Caprio topology were traded off with the supply voltage and current consumption growth. Following improvements prevent the discussed circuits from some of their earlier drawbacks (nonlinearity, narrow bandwidth, low output impedance).

Modifications of the Current Conveyor

In the design of CCII we started from classical rail-to rail conveyor with the feedback transistors that reduce the input impedance of the node X [5]. To improve the output impedance and current consumption it was necessary to lower the current together with preserving low input impedance on port X. The additional resistors implemented as an active load were introduced in series to the current mirrors. That helps to increase an output impedance. This modification lowers the voltage on gates of the transistors in output mirrors and does not change the signal path. The output impedance is larger with still reasonable power consumption [1]. Another improvement is the placement of regulated cascode [2] in place of simple or cascode current mirror (Figure 1).

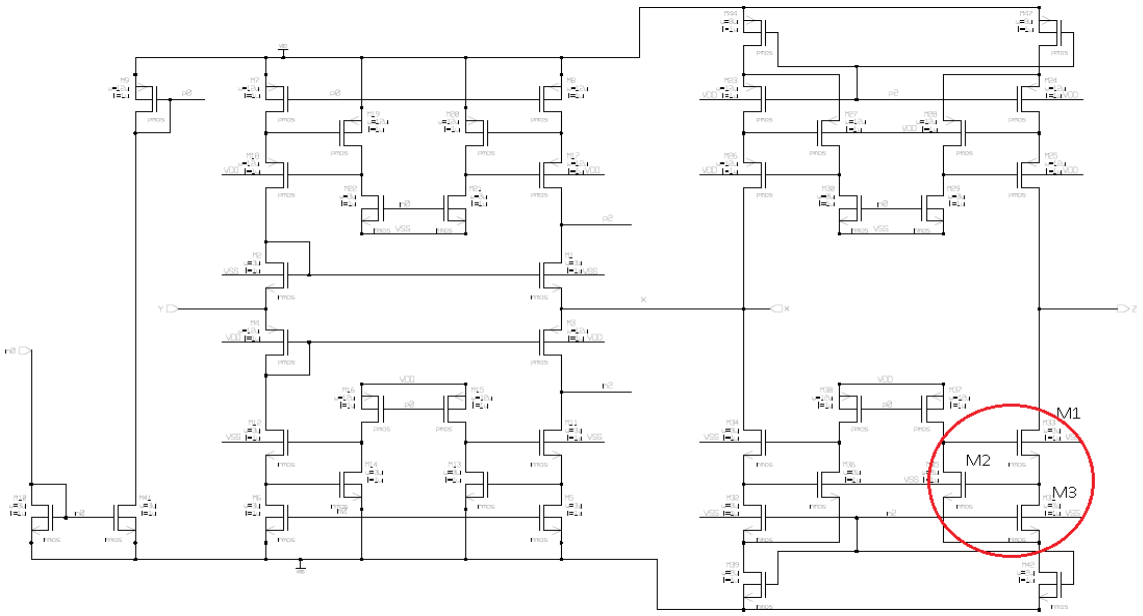

Fig. 1: Proposed Current Conveyor CCII+

That further improves the output impedance, since it is approximately

$$R_{out} \approx gm_1\, gm_2\, r_{o1}\, r_{o3}\, r_{o2} \qquad (1)$$

where the usual notation is used and indices correspond to the denoted transistors.

Caprio structure

When transferring the Caprio structure on Figure 2 based on translinear principle to CMOS, we used classical approach for differential input, single output devices. This simple current block has one advantage in its low input impedance. Nevertheless, there are also the drawbacks caused mainly by the folded cascode principle. They are mainly the narrower bandwidth incurred by the additional pole brought by the folded cascode and low output impedance. Anyhow, this block will be further investigated mainly for fully differential designs [4]. We assume, that the output structure will need large modifications to provide differential output (e.g. CMFB, advanced current mirrors, etc).

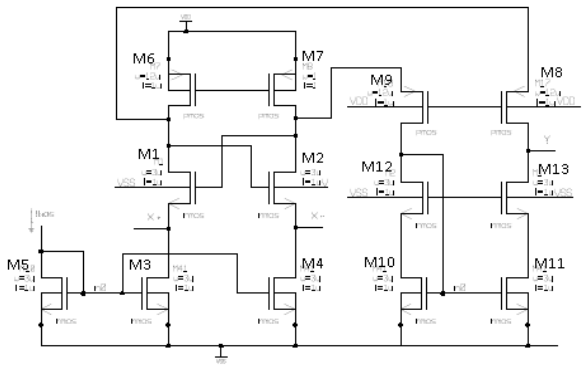

Fig. 2: CMOS Caprio structure

OPTIMIZATION VIA DIFFERENTIAL EVOLUTION

The optimization part is typical sizing problem in CMOS design. It is usually started up after the suitable topology of each circuit is proposed. Some of the useful methods of automated transistor sizing were published in several papers [5, 6]. The task is a proper selection of the variable input parameters of given topology with respect to fulfill all required output parameters of the optimized circuit. The input parameters are primarily sizes of the transistors; output parameters are for example bandwidth or gain.
We have recently implemented an efficient subset of the evolutionary algorithms – the differential evolution (DE) – into the optimization loop with the ngspice simulator that assures the objective function evaluation [5]. For later professional simulation (Eldo) and layout generation (Calibre) in Mentor Graphics package, the technology parameters of academic models for ngspice were converted to match the 0.25um CMOS design kit.

Objective function, parameters to be optimized

The objective function is typical error function defined as a sum of weighted squared deviations from desired parameter values over the set of observed circuit parameters:

$$f_{err}(\vec{x}) = \sum_i w_i \cdot \left(g_i(\vec{x}) - g_{i\,req}\right)^2 \quad \forall i \in \{p_i\}, \qquad (2)$$

where w_i is the i-th component of the weight vector, representing the importance of the i-th objective parameter g_i. The $g_{i\,req}$ is the required value of the i-th parameter and $\{p_i\}$ is the set of observed parameters - characteristics of the circuit - to be optimized.
Since both circuits operate as the current followers between certain terminals and the CCII implements also the voltage follower, the observed output

characteristics/parameters (p_i) are very similar. Ideally all transfers should equal one, current input terminals should have zero input resistance and output current terminals should have limitless output impedance. These specifications should have been met under the global requirement of wide bandwidth and low power consumption. The notation of desired values in figure (2) is $g_{i\,req}$. The optimization process so as the input variables and observed output characteristics are described in detail in the paper [5].

Optimization results

Before an advanced optimization, both blocks were set "by hand". This setting was quite successful and mainly for the CCII we found only a partial improvement when using the advanced methods. In the mentioned case it was caused by the high number of variables – transistor lengths and widths. Hence we only used several different transistor geometries (as in the first hand approach) to experience the results in the feasible time. In the case of Caprio structure, after several optimization runs, we found 3 different minimum peaks of the objective function and the lowest one was simulated for this article.

The results of the optimization flow of the Current Conveyor is as follows: all PMOS/NMOS devices except those, that implement the active load described in the paragraph denoted to CCII modifications are sized 12/1, 3/1 respectively, the active load transistors have sizing 8/1, 2/1 respectively. The optimal sizing of Caprio structure in selected design technology is: M1, M2, M10, M11 – 6.2/1, M3, M4, M5, M12, M13 – 10.3/1, M6, M7 – 31.1/1, M8, M9 – 17.2/1. All values obtained by the optimization were rounded to the process grid and matched together

The optimized design of proposed blocks meets the criteria given by the ITU norm (namely the cut off frequencies). Anyhow, it is worth to mention, that the optimization of CCII was not even noticeable due to the fact of the search only in a close neighborhood of selected by the "rule of thumb" optimized point.

SIMULATION RESULTS

The main results for proposed blocks are summarized in the below and Figures 3 and 4 under the comments.

Simulation results

	$f_{cut\text{-}off}$ [MHz]	R_{in} [Ω]	R_{out} [MΩ]	Linearity region [uA]	Supply [V]
CCII	459	47	260.1	-150÷150	±1.8
Caprio	263	23	0.16	-50÷50	±1

CCII

The proposed circuit has in compare to [2] higher output impedance and a little lower supply voltage when the comparable bandwidth, input impedance and linearity of the forgoing design are maintained.

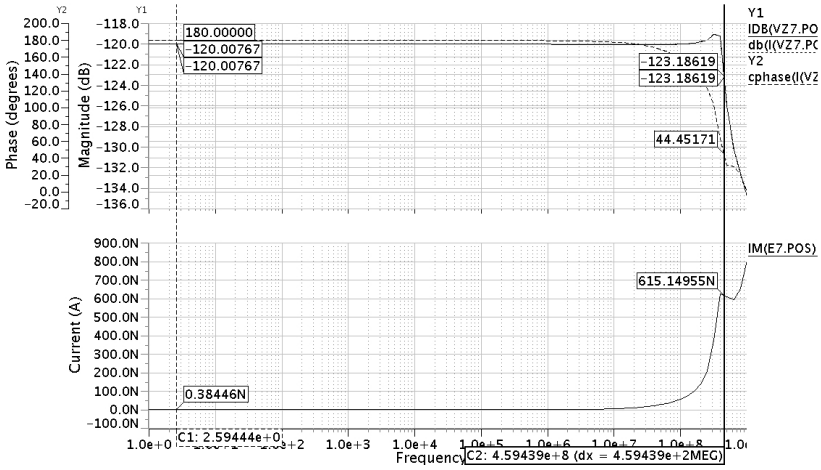

Fig. 3: AC characteristics of CCII – output current (Iin=1uA), current through the output node for Vout=100mV

Caprio topology

Caprio structure appears as a perspective current mode, differential input topology with very low input impedance and wide bandwidth. We do not suppose to use the output topology as it is due to its low output impedance.

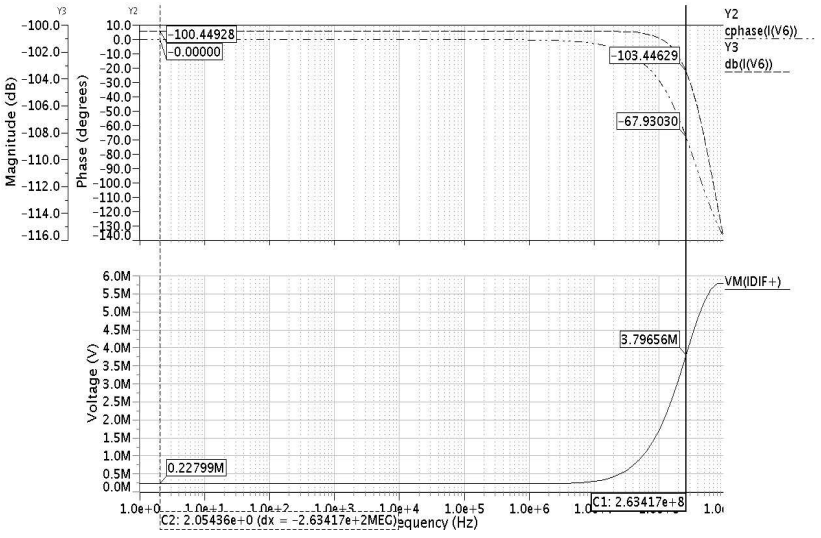

Fig. 4: AC characteristics of CCII – output current (Iin=1uA), current through the output node for Vout=100mV

CONCLUSION

The current mode building blocks for video signal applications were proposed. The first proposed circuit could be directly applied in the filter design. The second one was designed as a differential input stage for X node of future fully differential current mode block . That will lead to an enhanced fully differential structure.

Specifically, the proposed circuits are applicable for CM and VM ARC filter implementations using Bruton's transformed LC prototype. The can easily implement the structures of lossy FDNRs correspond to the basic nullor model [3]

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