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Optimization of Printed Circuit Board Design Assembly based on DPMO Metrics

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Abstract:
The paper deals with optimization of printed circuit board assembly (PCBA) design based on defects per million opportunities (DPMO) metric. Due to DPMO data predictions for a given new PCBA design is possible to optimize its layout in terms of yield and quality even before the PCBA pilot production. The DPMO data are obtained from the below presented yield-DPMO model. The model is based on a combination of elements from DPMO calculation according to the IPC 7912 standard and two most used yield prediction methodologies, namely: process yield and board design yield. The model provides not only DPMO data, but also assembly process yield prediction that can assist the manufacturers in determining reliable estimates of production capabilities.

INTRODUCTION

The electronics manufacturing industry producing PCBAs faces continuously stronger competitive environment. The producers have to optimize their processes, shorten product cycle times, reduce cost of test and repair and increase yield in order to stay competitive.

But on the other hand, the trend in Printed Circuit Board Assembly technology is towards higher complexity. Many boards have significantly more components and solder joints today than just a few years ago. More components and more solder joints means more defect opportunities and lower yields. A higher number of components typically means higher cost for each PCBA, resulting in higher work in process (WIP) cost and scrap costs. The higher WIP costs and scrap costs are also because higher complexity typically means lower yields and more difficulty in diagnosing when failures occur. The decrease in electrical and visual access makes it more difficult for effective test and inspection techniques.

When we focus on first pass yield, it is possible to define three things that control FPY: design processes, quality of incoming materials, manufacturing processes and equipment. In other words, we need to have a good "recipe" (design processes), good "ingredients" (incoming material) and a good "chef" (manufacturing).

Nowadays the outsourcing trend dominates where the contract manufacturer ("chef") does not have total control on quality, as the original equipment manufacturer (customer) also controls the design ("recipe") and incoming material ("ingredients"). But often the contract manufacturer takes the blame. That is not only a wrong approach, but this thinking will never lead to higher yield and lower cost. To solve yield problems, it is necessary to understand the interdependency of design and manufacturing [1].

The FPY metric is one of the well-known methods how to measure the quality of the assembling process. The limitation of this method consists in the fact that it is just a ratio between good and wrong PCBAs, there is no link with the number of defects on the bad boards. This is becoming more important in a high mix – low volume production, where is more complex to make the PCBA without any defects, since there is not possible to fine-tune the manufacturing process, as could be done in a high volume environment. The another limitation comes from very close connection between measured yield and test coverage.

On the other hand, Defects per Million Opportunities (DPMO) metric is an easy method of measuring process performance often used in Six Sigma initiatives. DPMO also serves as a basis for calculating process sigma values, another performance measure. Unlike Defects per Unit (DPU), which provides the number of defective products, DPMO takes into account the reality that multiple defects can exist in a single product. DPMO is fully comparable metric in contrast to FPY.

Due to a PCB assembly process DPMO and yield prediction is possible not only to assist the manufacturers in determining reliable estimates of production capabilities, but also to optimize the PCB design process.

Through the use of sensitivity analysis can be determined an effect that each component package has on the manufacturing yield and process

performance. The component packages, having the biggest influence on the manufacturing yield loss or on the decline of process performance, represent potential failure areas. Due to this information is possible to optimize PCB design before the start of mass production in order to minimize or even to eliminate these "problematic" component packages. The result of this procedure is an increase in the manufacturing yield and a process performance improvement.

DPMO

DPMO (Defects per Million Opportunities) according to the standard **IPC-7912** entitled Calculation of DPMO and Manufacturing Indices for Printed Board Assemblies is defined as the total number of defects divided by the total number of opportunities for a defect multiplied by 1,000,000 [3]. It is not strictly equivalent to "PPM" as the definition of "opportunities" has special meaning when considering electronic assembly processes.

$$DPMO = \left(\frac{\sum d_x}{\sum o_x} \right) \times 10^6 \qquad (1)$$

d_x… number of defects
o_x … number of opportunities

$$DPMO = \left(\frac{\sum d + \sum d_p + \sum d_t}{\sum o_c + \sum o_t + \sum o_p} \right) \times 10^6 \qquad (2)$$

Component Opportunities (o_c) is defined as each device or piece of hardware that may be assembled onto a PCB.
Component Defect (d) is damage to a component exceeding the limits of the component specification.
Placement Defect (d_p) is any component presence and/or positioning error that has occurred during an assembly operation.
Termination Opportunity (o_t) is defined as any hole, land or other surface (such as component to component attachment) to which a component may be electrically terminated.
Termination Defect (d_t) is any electrically joined termination that violates the requirements specified in J-STD-001 or IPC-A-610.
Placement Opportunity (o_p) - The term "placement" refers to the presence and/or positioning of any component on a PCB [3].

YIELD, FIRST PASS YIELD

The metric yield is defined as the number of good units produced divided by the number of total units going into the process. But mostly in the industry is used the metric First Pass Yield (FPY) which is calculated as following: the number of PCBAs which passed through the entire assembly process without any defect, any rework, any retest divided by the total number of produced boards.

It is necessary to understand properly what a defect is. The defect is defined as an unacceptable deviation from a norm at the end of manufacturing process [4]. Faults are a subset of defects. A fault is manifestation of a defect.

Thus a defect may or may not turn out as a fault. Defects are detected by testing and inspection systems. In our case we will consider all defect that were detected by downstream testing system no matter if they turn out as a fault or not. First pass yield can be downgraded by one more phenomenon so-called false calls when the good items are detected as failure ones. False calls are mostly generated by automated optical inspection systems (AOI).

YIELD-DPMO MODEL

The yield-DPMO model is based on the yield prediction tool which was created in my dissertation. The inputs for the model are either historic yields or DPMO data with their bill of materials (BOM) from the manufacturing lines, where DPMO and yield to be predicted, the BOM of new PCBA design, test coverage of the tests used at the manufacturing line and it is necessary to calculate opportunities to failure.

The outputs of the model are DPMO data and yield prediction of the new designed PCBA and results from the sensitivity analysis, which show the component packages having the biggest influence on the manufacturing yield loss or on the decline of process performance.

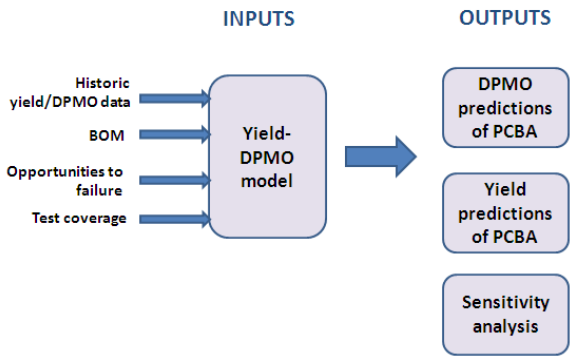

Fig. 1: The Inputs and outputs of Yield-DPMO model

Due to the yield prediction tool is possible to compute defect probabilities for component packages using the first pass yield history for previous board

designs. The yield prediction model combines elements from two most used yield prediction methodologies, namely: process yield and board design yield, and it is based on minimizing the difference between actual and predicted yields.

Tab. 1: The model for yield prediction for individual component packages [2]

Given values :	
ND	total number of different PCBs
j	number of PCB, j=1,….., ND
y_j	actual first pass yield for board j
N	total number of component package types
k_j	logarithm of the actual first pass yieldu, -ln(yj)
$n_{j,i}$	number of components of package type i for board j
Finding values:	
p_i	fault probability for components of package type i [ppm/1000h]
Objective function	**(minimize)**
$\min z = \sum_{i=1}^{ND}\left(k_j - \sum_{i=1}^{N} p_i n_{j,i}\right)^2$	
Conditions:	
$0 \le p_i \le 1$	

Yield prediction is then possible to calculate in two steps:

1) Group components of a new designed board according to package types and then use optimization model.

2) Determine first pass yield prediction according to the equation 4.

$$Y = \prod_{i=1}^{N} e^{-\lambda_i} = e^{-\sum_{i=1}^{N}\lambda_i} = e^{-\sum_{i=1}^{N} n_i * p_i} \quad [-] \qquad (4)$$

The yield model was tested on 20 real projects from the automotive electronics industry. The model performs well for various projects with 1,81% average difference with respect to the actual yield and with maximum difference 7,23% with respect to the actual yield.

The DPMO is calculated from yield predictions based on the following formula:

$$DPMO_n = -\frac{\ln(Y_n)}{o_n \times C_T} 10^6 \qquad (5)$$

C_T… test coverage
o_n … number of opportunities to failure at the point n
Y_n … Yield at the point n

It is possible to calculated DPMO for individual package types and then to determine which package type downgrades the process performance the most. Number of opportunities to failure at the point n could be automatically calculated from the BOM of the new PCBA design. Test coverage data can be obtained from the historic delivery quality data.

BOARD DESIGN OPTIMIZATION

When a PCBA is designed, quality planners need to know not only first pass yield and DPMO prediction, but also they want to know means how is possible to maximize the predicted yield and process performance. Information which can help during process yield optimization can come from several sources. One of the most important one is so-called sensitivity analysis.

Tab. 2: FPY and DPMO predictions for different PCBA designs

Packages	Design Versions			
	Version 1	Version 2	Version 3	Version 4
0603	33	43	28	26
0603 _06	69	45	83	43
0603 _13	29	34	32	29
0805	10	8	9	11
0805_075	17	22	17	18
do214aa	6	8	5	8
do214 ac	2	4	3	5
double coil	6	5	3	4
erc16	9	8	4	3
gfp112	2	1	1	1
quartz 11x10	1	1	1	1
rx4 array	4	3	5	3
SO8	9	6	6	6
SOP12	5	5	2	5
SOT23	9	15	7	16
SOT323_3	13	17	8	20
SOT363	7	10	5	10
conector 40-pin	2	1	1	2
tacab	4	3	4	4
FPY [-]	0,9023	0,8752	0,939	0,8542
No. of opportunities to failure	1313	1163	997	1062
DPMO	120,46	176,34	97,12	228,29

Process optimization demands a thorough analysis of the entire system, finding of relationships among elements and last but not least an evaluation, how the output is sensitive to inputs (in our case - component packages). The sensitivity analysis is suitable for this

purpose. It is used from following three primary reasons [5]:

a) understanding of results reliability

b) recognition of the best controllability of the system

c) specification of prospective experiments

In this paper we will deal with the field of recognition of the best system controllability, where it is investigated how the value of first pass yield or DPMO can be changed depending on various design variants and which component packages decrease the first pass yield the most or downgrade process performance.

The graph presented bellow shows an increment of 1 to 15 components for each component package assuming that all other components remain constant. Each increment consists of adding a component of a given package while the rest of the components in the board remain the same. The purpose of considering individual increments is to measure the effect that adding one component has on first pass yield.

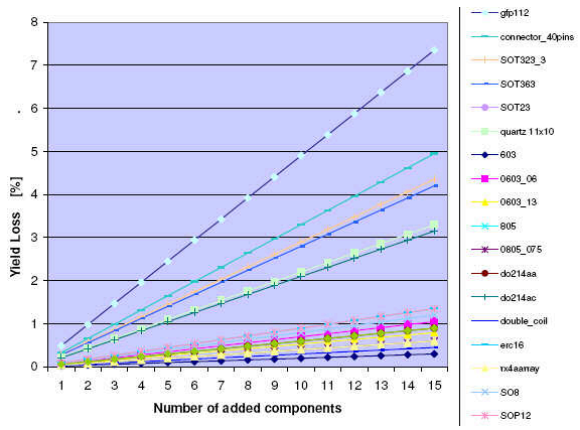

Fig. 2: Sensitivity analysis of component packages based on FPY

From the results presented in Figure 2 six component packages (gfp112, connector_40pins, SOT323_3, SOT363, quartz11x10, do214ac) clearly appear to be affecting manufacturing yield loss considerably. Therefore the designers should try to minimize the number of these packages as much as possible.

Tree PCB designs were optimized by using the sensitivity analysis of component packages. The result of the optimization were 4,5% average increase of the manufacturing yield with respect to the manufacturing yield before the optimization.

Mostly it is created more variants of PCBA (with different components, different layout – see table 2) during a design process. The sensitivity analysis can help during a decision process which designed variant is the best.

It says which variant is the best in terms of first pass yield or process performance - DPMO. In other words, it reports which design contains as few as possible of "problematic" component packages which decrease the first pass yield and process performance the most. In the presented example the best version in terms of FPY is the version 3 with the FPY = 93,9% and DPMO of 97,12 (see the table 2).

CONCLUSION

Due to the Yield-DPMO model is possible to obtain predictions of manufacturing yield and DPMO, which are critical to the business success of products. Understanding the mechanism behind the yield loss and process performance downgrade, thus enabling the rapid identification and fix of problems, is crucial for success. Predictability is also important, for production control, material management and timely product delivery. Yield and DPMO models are a principal operation planning tool. Accurate models mean a predictable business. The advantage of DPMO is the fact that it is fully comparable metric and it is not associated only with the certain manufacturing line.

The sensitivity analysis of component packages represents sort of feedback for PCB design process. Engineers can utilize this information to determine which board design best suits the performance characteristics of their given production lines.

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