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Capacitor-less Linear Regulator with NMOS Power Transistor

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Abstract:
A 3.6 (4.3) V 50 mA capacitor-less linear voltage regulator for system on chip (SoC) is introduced. It does not require any external component and is stable in a wide range of load current. This regulator uses an NMOS transistor as the power element. In order to increase the gate voltage of the power element switched floating capacitor is used. The proposed linear regulator has been designed in a commercial 0.13 μm CMOS technology. The variation of output voltage is less than 100 mV even if a full load step is applied and current consumption of this regulator is 150 μA regardless of the load current.

INTRODUCTION

With the increasing effort to integrate all circuits into a single chip, thereby establishing a SoC solution, the demands for power management unit (PMU) and its integration are growing [1]. Ideally, each block in the SoC should be supplied by independent regulated voltage. This can be achieved by using a dedicated on-chip linear voltage regulator for each circuit in the SoC. The main assumptions that are made on regulators in the SoC are small silicon area, low power dissipation, and last but not least the absence of external components that must be connected to the chip, and thus increase the price of the whole system and occupy pins of chip itself.

Linear regulators can be divided into two basic groups [2]:

- Conventional linear regulators
- LDO (low drop-out) regulators

The only difference between these two topologies, is in orientation of a power transistor. Conventional linear regulator utilizes a transistor which is connected in common drain, or this one transistor is replaced by a bipolar transistor (BJT), or two transistors in Darlington configuration. In the contrary LDO regulator uses configuration with common source. Both these basic configurations are depicted in the Fig. 1. The single orientation of a power transistor has a general influence on both working mode and stability of the linear regulator.

The most significant element which has the greatest influence on transient response of the regulator is the power transistor. This transistor delivers required current into the load impedance which in turn results in required output voltage. A delay which is caused by the power transistor in the control loop is caused by the fact that gate capacitance of this power transistor represents current voltage converter. The greater gate capacitance, the greater is the delay. This delay has dominant role in the entire delay of the control loop.

In LDO regulators a PMOS transistor (Fig. 1) is used in common source configuration as a power element. However with this configuration several disadvantages occur. The first drawback of using PMOS transistor is its lower mobility when compared to NMOS transistor. It means that PMOS transistor needs larger silicon area than NMOS transistor for comparable properties [3]. This larger power transistor reduces rate of charging common source. This configuration has higher output impedance than the source follower configuration in the NMOS

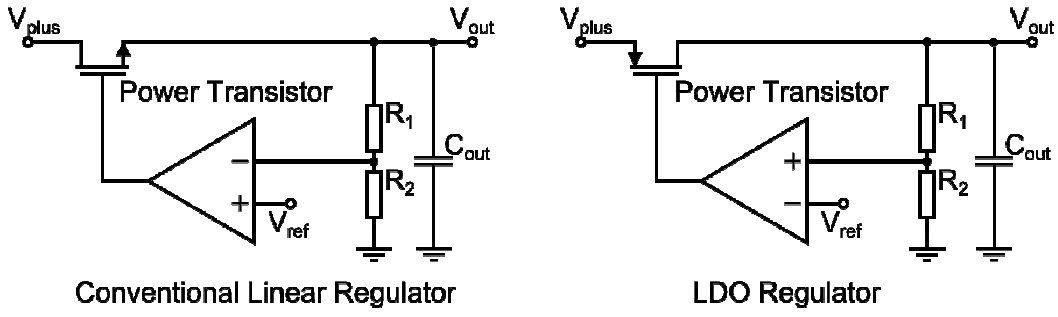

Fig. 1: Topologies of linear regulators.

regulator (Fig. 1). For LDO regulators this adds an additional low-frequency pole whose frequency is dependent both on load resistance and output capacitance. To ensure stability a large external capacitor and other compensation circuit is needed. Another drawbacks associated with the low frequency dominant pole are bandwidth limitation and the slow load regulation response. This can be enhanced by fast loops that increase regulator bandwidth [4].

All these disadvantages associated with the PMOS transistor can be eliminated by using the NMOS transistor. This power transistor is connected in a configuration known as source follower. An important characteristic of this circuit is low output impedance, which means the output pole is placed at a high frequency. With this in mind we do not use the output pole as dominant pole and thus we do not need external capacitor. Moreover, because the NMOS transistor has greater mobility, for the same output current a significantly smaller area of silicon is required.

On the other hand, even with NMOS power transistor several disadvantages are associated. One of the main drawbacks is that the gate voltage of power transistor must be at least by V_{gssat} greater than the output voltage. This itself is not a problem, but in addition with the ever decreasing supply voltage, this leads to the fact that the supply voltage gets below possible level of gate voltage. The result is that the power transistor requires charge pump. An alternative to raise the gate voltage is approach known as gate overdrive [5], which uses a floating voltage supply to elevate the control voltage into a range high enough to keep the NMOS pass element operating in saturation region.

CAPACITOR-LESS LINEAR/LDO REGULATORS

Conventional linear/LDO regulators are in common use and they are still being developed [6] and [7]. However a considerable part of current research of regulators aims at capacitor-less linear/LDO regulators [8], [9] and [10]. By removing an external capacitor of the regulator we introduce new

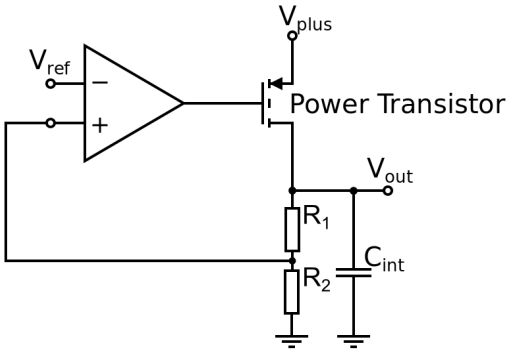

Fig. 2: Simplified circuit diagram for capacitor-less LDO regulator.

possibilities in power management like reduction of chip area, fewer pins are necessary and this leads to decrease of the price of the whole system.

On the Fig. 2 one can see that there is still a capacitor present at the output of a capacitor-less LDO regulator. But contrary to linear regulators (Fig. 1) (where the output capacitor is in the range of several microfarads) the value of this internal capacitor for capacitor-less LDO regulators is much smaller (in the range of several hundreds picofarads) and consequently its transient properties are much worse. For this reason it is necessary to implement enhancement structure to improve transient response.

Properties of Transient Responses

Presence of a large external capacitor at conventional linear/LDO regulators generally improves properties of the regulator during transient responses. It is due to the fact that the output capacitor stores energy which is proportional to the output voltage. This energy is transformed into current during changes. If we had an ideal capacitor with infinite bandwidth and zero internal resistance, then, such a capacitor would react immediately. During transfer of the charge from capacitor to the load a drop of output voltage is created. Equation 1 roughly describes relation between drop of voltage ΔV_{out}, charge ΔQ and value of the capacitor C_{out}.

As can be seen from the equation 1, change of output voltage is inversely proportional to the value of the external capacitor. Transient properties of

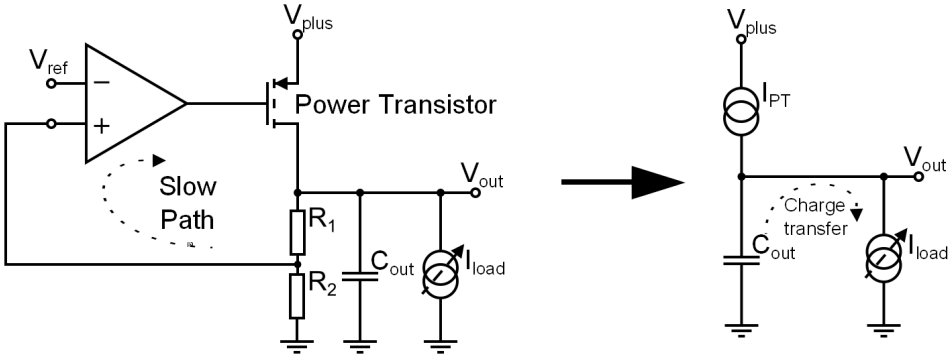

Fig. 3: Conventional LDO regulator with reduced loop bandwidth and its equivalent circuit diagram for fast load transients [10].

$$\Delta V_{\text{out}} \cong \frac{\Delta Q}{C_{\text{out}}} \qquad (1)$$

a regulator can be improved by increasing the value of this external capacitor. If the load transients are much faster than time response of the regulator, which is common with increasing clock frequency of IC, then meaning of the equation 1 is much more evident. Fig. 3 depicts this situation for conventional LDO regulator.

If the time response of the regulator is much smaller than load transients we can suppose constant gate voltage and the power transistor as such can be replaced by constant current source. With this on mind the change of the output voltage is described directly by equation 1. Contrary to conventional linear/LDO regulators, capacitor-less linear/LDO regulator misses large external capacitor and consequently its transient properties are much worse. To improve these properties it is necessary to replace constant current source from Fig. 3, where the power transistor is shown, by an adaptive source of current, which can react on fast changes of loading current.

Design of a Capacitor-less Linear Regulator

The aim of this work is to design a capacitor-less linear regulator for SoC applications. It is important for the circuit to be stable at all loading currents, mainly during small loading currents. Also, it is necessary that the circuit has acceptable reactions on fast change of load.

From this reason it is necessary to extend the circuit by fast loops, which will be responsible for fast response of the circuit and which will have greater bandwidth than the slow regulating loop. It is necessary to add these circuits due to absence of an external loading capacitor.

The basic concept of the designed circuit is depicted in the Fig. 4. In the concept one can see a fast loop, that improves transient parameters of the circuit, and also slow loop is shown. This slow loop sets the required output voltage during the steady state or during slow change of a loading current.

On the other hand, the fast loop should react on the fast transient changes of loading current and as such to control changes in output voltage. Also, low

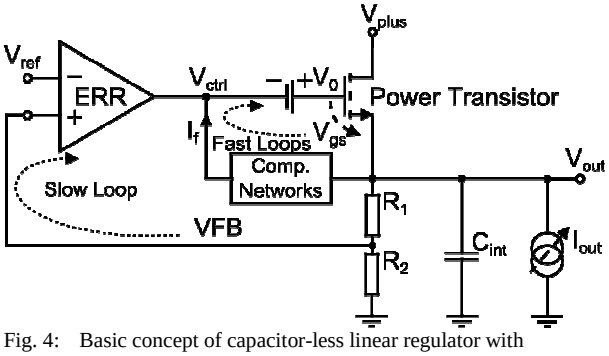

Fig. 4: Basic concept of capacitor-less linear regulator with NMOS power transistor.

consumption of the whole regulator belongs into aims of this work. It is from the reason that more and more emphasis is laid on efficiency in power management.

CONCEPT OF NMOS CAPACITOR-LESS LINEAR REGULATOR

In the following part we will describe core of the circuit (Fig. 5) and implementation of enhancement structure (Fig. 6), which is used for realization of the NMOS capacitor-less linear regulator. Basis of the circuit is the power transistor (M_{PT}) similarly as the topology of classic linear regulator. This type of regulator is like a voltage source which keeps output voltage constant and independent of change in load or change of battery voltage. Current I_{PT}, which is controlled by gate voltage on the M_{PT}, is divided between the load of the regulator and the transistor M_5, as depicted in the Fig. 5.

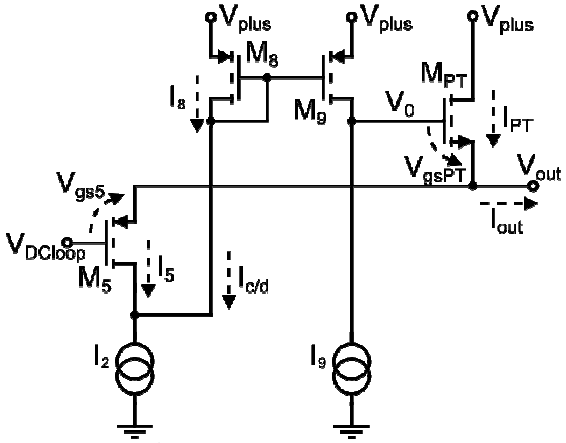

Fig. 5: The core of the NMOS capacitor-less linear regulator.

Current source I_8 delivers constant current, charging the gate capacitance of the power transistor. Transistor M_5 similarly like the power transistor M_{PT}, works in saturating mode and a control voltage from slow loop (V_{DCloop}) is applied to its gate. The current I_5, flowing through this transistor is dependent on the voltage V_{gs5} ($V_{gs5} = V_{DCloop} - V_{out}$) and so we can say that it works as a comparator. Magnitude of the current, which flows from current source I_2, is constant and in steady state given by a sum of currents I_5 and I_8, as depicted in the Fig. 5.

After general introduction of basic elements in the circuit we can describe the principle which this linear regulator works on. In the same way as it is at basic topology of regulator, even here a loop of feedback closes via comparator. The feedback is used to set the output voltage. Adjustment is based on the fact that current from source I_2 is constant, and the change of the current I_5 causes change of the current $I_{c/d}$, which has an influence on amount of charge on the gate of power transistor and related gate voltage on the power transistor. As it was stated earlier,

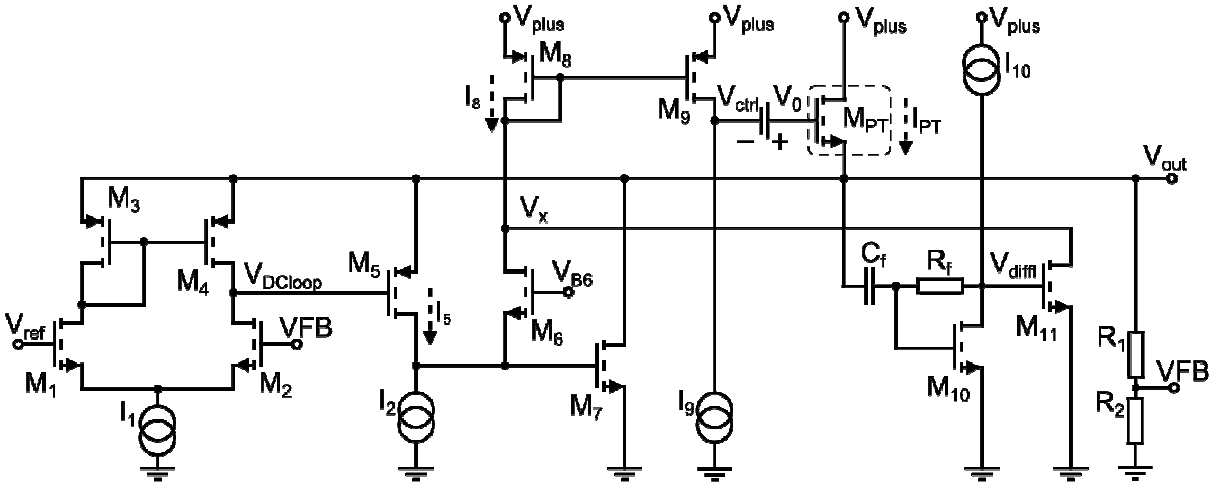

Fig. 6: Circuit implementation of the capacitor-less linear regulator with NMOS power transistor.

transistor M_5 regulates the amount of current I_5 which depends on the change of load. As it is apparent from the equation 2, output voltage of the regulator, V_{out}, depends only on constants and on the current I_5.

$$V_{out} = (V_{ref} - V_t) - \sqrt{\frac{2I_5}{\frac{W_5}{L_5}\mu C_{ox}}} \qquad (2)$$

Even during the change of load, the current source I_8 still delivers constant current, which means, that gate voltage of the power transistor V_0 is controlled by change of current $I_{c/d}$. Thus the current which flows through the power transistor is controlled by the current I_2, resp. by the current I_5 thereby closing feedback.

The great advantage of this circuit is its speed due to the fact that the circuit works in a current mode. Simultaneously the circuit has one dominant disadvantage – great stand-by current consumption for acceptable transient response. Maximum charging speed of the input gate capacitance of the power transistor is limited by current source I_8. The magnitude of the current, which is delivered by this source, is usually half of the I_2 current. The reason is that charging/discharging of the power transistor gate need to have the same maximum speed.

As shown in Fig. 4, NMOS capacitor-less linear regulator consists of error amplifier, floating voltage source, power transistor, compensation networks and the feedback network. The output voltage of the error amplifier (V_{ctrl}) is raised above the supply level by a constant floating voltage source. In theory the floating voltage source could be implemented as a charged floating capacitor. However, the voltage across the capacitor would drop due to its leakage current. This problem is solved by using two switched floating capacitors.

Implementation of Capacitor-less Linear Regulator

Concept of linear regulator, which was introduced in the previous part, needs to be rearranged in other to be realized in integrated form and also to improve its parameters like current consumption.

To the most fundamental changes belongs adding differential amplifier, which maintains required operation point of the whole regulator. What more, we added cascade transistor M_6. Furthermore, we added capacitive differentiator (C_f, R_f, M_{10}, M_{11}) [9] and [10], which compensates transient response, and finally a discharge transistor M_7 [5]. Fig. 6 depicts the elementary parts which are mentioned.

By adding differential amplifier into the concept of regulator is created series connection of two feedback loops. The previous loop, depicted in the Fig. 5, represents series fast loop while the differential amplifier creates slow loop. For improvement of *PSRR* (Power Supply Rejection Ratio) of the circuits is used a possibility to supply differential amplifier directly from the output of regulator.

Subliminal mode of the power transistor significantly slows down the response of the circuit. This can cause degradation in voltage regulation for applications where loading currents drop to very low levels in a very short time. This degradation in transient response of regulator can be eliminated by adding a discharge circuit. This is another arrangement of circuits of the regulator which should improve transient response of the regulator during fast decrease of loading current. Fig. 6 depicts principal connection of the regulator together with discharge transistor. This discharge circuit works only if regulating loop does not work in common mode but it is in saturation (during very fast changes of loading currents).

RESULTS AND COMPARISON

The proposed linear regulator was designed in a 0.13 µm CMOS technology. It provides a regulated output of 3.6 V or 4.3 V. The regulator was designed for delivering a maximum output current of 50 mA with a minimum drop-out of 100 mV. The power transistor has a *W*/*L* (width/length) ratio equal to 4000 µm/0.5 µm. The maximum quiescent current of the regulator is 150 µA, which corresponds to less than 0.5% of the maximum load current.

The load regulation response of the regulator is tested by switching the load current from 100 µA to 10 mA and vice versa with t_{rise}/t_{fall} edge 1 µs (Fig. 7) resp. 10 ns (Fig. 8).

Maximum output voltage variation for typical conditions which was obtained from the simulation for NMOS capacitor-less linear regulator is about 76 mV (Fig. 7(a)) and for PMOS capacitor-less LDO regulator is about 41 mV (Fig. 7(b)). One can see that for edge 1 µs PMOS capacitor-less LDO regulator has better results (variation of output voltage is almost twice smaller than NMOS capacitor-less linear regulator). Opposite case occurs in the situation when t_{rise}/t_{fall} edge is very fast (10 ns). Variation of output voltage for PMOS capacitor-less LDO regulator (Fig. 8(b)) is about 210 mV higher than for NMOS capacitor-less linear regulator (Fig. 8(a)).

Table 1 summarizes the performance of the proposed NMOS capacitor-less linear regulator compared to PMOS capacitor-less LDO previously reported [11].

As can be seen, the present work presents higher maximum output current (50 mA), with an improved dynamic performance for fast variation of load current, this means a faster setting time and a small variation of the output voltage.

CONCLUSIONS

New NMOS capacitor-less linear voltage regulator was introduced, which is capable of delivering 3.6 V or 4.3 V at loading currents up to 50 mA. PMOS capacitor-less LDO regulator [11] has two times lower current consumption than the proposed regulator but on the other hand maximum current load increased five times more than PMOS capacitor-less LDO regulator [11].

NMOS capacitor-less linear voltage regulator does not require any external component and is stable in a wide load current range with capacitive load up to 2 nF. Extensive simulation results demonstrate the feasibility of the design.

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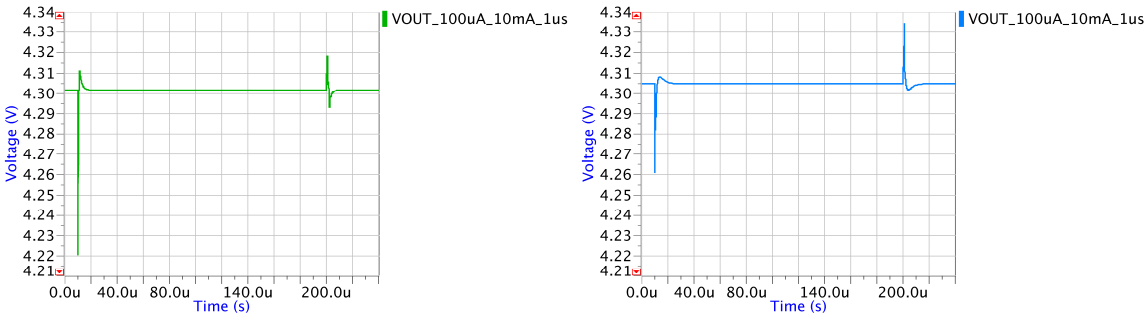
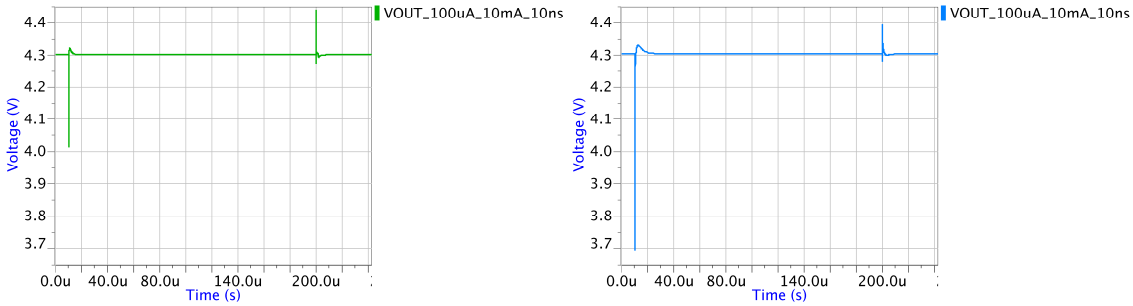


(a) NMOS capacitor-less linear regulator (b) PMOS capacitor-less LDO regulator [11]

Fig. 7: Comparison of transient response on the load step from 100 µA to 10mA with t_{rise} resp. t_{fall} 1 µs.



(a) NMOS capacitor-less linear regulator (b) PMOS capacitor-less LDO regulator [11]

Fig. 8: Comparison of transient response on the load step from 100 µA to 10mA with t_{rise} resp. t_{fall} 1 µs.

Table 1: Comparison of results between proposed NMOS capacitor-less linear regulator and PMOS capacitor-less LDO regulator [11].

			Proposed NMOS linear regulator Simulation			PMOS LDO Simulation			
Parameter	Name	Test conditions	Min	Typ	Max	Min	Typ	Max	Unit
Input supply voltage	V_{plus}	$(V_{plus}) - (V_{gnd})$	3.77	4.8	5.5	3.77	4.8	5.5	V
Output current	I_{load}		0		50	0		10	mA
Output voltage	V_{out}	VSEL = `0` VSEL = `1`	3.587 4.283	3.6 4.3	3.621 4.324	3.583 4.276	3.6 4.3	3.626 4.334	V
Expected parasitic load	C_{out} ESR		0.1 0		2 250	0.1 0		5 250	nF mΩ
Current consumption	I_{dd}	I_{load} = 10 mA I_{load} = 100 µA		100 100	135 142		65 58	72 67	µA
Load transient	Ldtr	I_{load} @ t_{rise} (t_{fall}) = 1 µs from 100 µA to 10 mA from 10 mA to 100 µA −30°C to 125°C		76 16	97 27		41 27	72 47	mV
		I_{load} @ t_{rise} (t_{fall}) = 10 ns from 100 µA to 10 mA from 10 mA to 100 µA −30°C to 125°C		280 107	547 297		591 71	890 186	

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